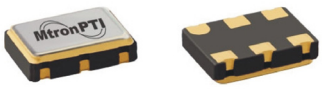
# M210x Series

## 5x7 mm, 3.3/2.5/1.8 Volt, LVPECL/LVDS/CML, Clock Oscillator

## Product Features

- Featuring *QiK Chip™* Technology
- From order to ship in 2 weeks
- Superior Jitter Performance (less than 0.25 ps RMS, 12 kHz - 20 MHz)
- SAW replacement - better performance
- Frequencies from 150 MHz to 1.4 GHz

QiK Chip™



## Product Description

The 210x series of oscillators are 5x7 mm oscillators designed with the QiK Chip™ technology. The QiK Chip™ technology was specifically designed for crystal based oscillators to provide low jitter performance (as low as 0.25 ps RMS) and a wide range of frequency support (150.00 MHz to 1.4 GHz) and provides a breakthrough in lean manufacturing enabling product to be provided in less than 2 weeks. The M210x provides design engineers with the stability needed in their advanced applications and supports the need for parts to be supplied quickly so that the rest of their circuit design can be solidified.

## Product Applications

- Telecommunications such as SONET / SDH / DWDM / FEC / SERDES / OC-3 thru OC-192
- 1-2-4-10 Gigabit Fibre Channel
- Wireless Base Stations / WLAN / Gigabit Ethernet
- Avionic Flight Controls
- Military Communications
- Clock and Data Recovery
- SD/HD Video
- FPGA/ASIC Clock Generation
- Test and Measurement Equipment

## Product Ordering Information

**Ordering Information**

**M210 0 6 8 B P C 00.0000 MHz**

**Product Series**

**Supply Voltage**
**0:** 3.3 V **1:** 2.5 V
**2:** 1.8 V

**Temperature Range**
**2:** -40°C to +85°C
**6:** -20°C to +70°C

**Stability**
**4:** ±50 ppm **3:** 100 ppm
**8:** ±20 ppm

**Enable/Disable**
**B:** Enable High (pin 1) **G:** Enable High (pin 2)
**S:** Enable Low (pin 1) **M:** Enable Low (pin 2)
**U:** No Enable/Disable

**Logic Type**
**P:** LVPECL **L:** LVDS
**M:** CML

**Package/Lead Configuration**
**C:** 5x7 mm Leadless (6 Pin)
**N:** 5x7 mm Leadless (9 Pin - Contact Factory for availability)

**Frequency (customer specified)**

M2100Sxxx, M2101Sxxx, M2102Sxxx & M2103Sxxx - Contact factory for datasheets.



Revision: 8-22-08

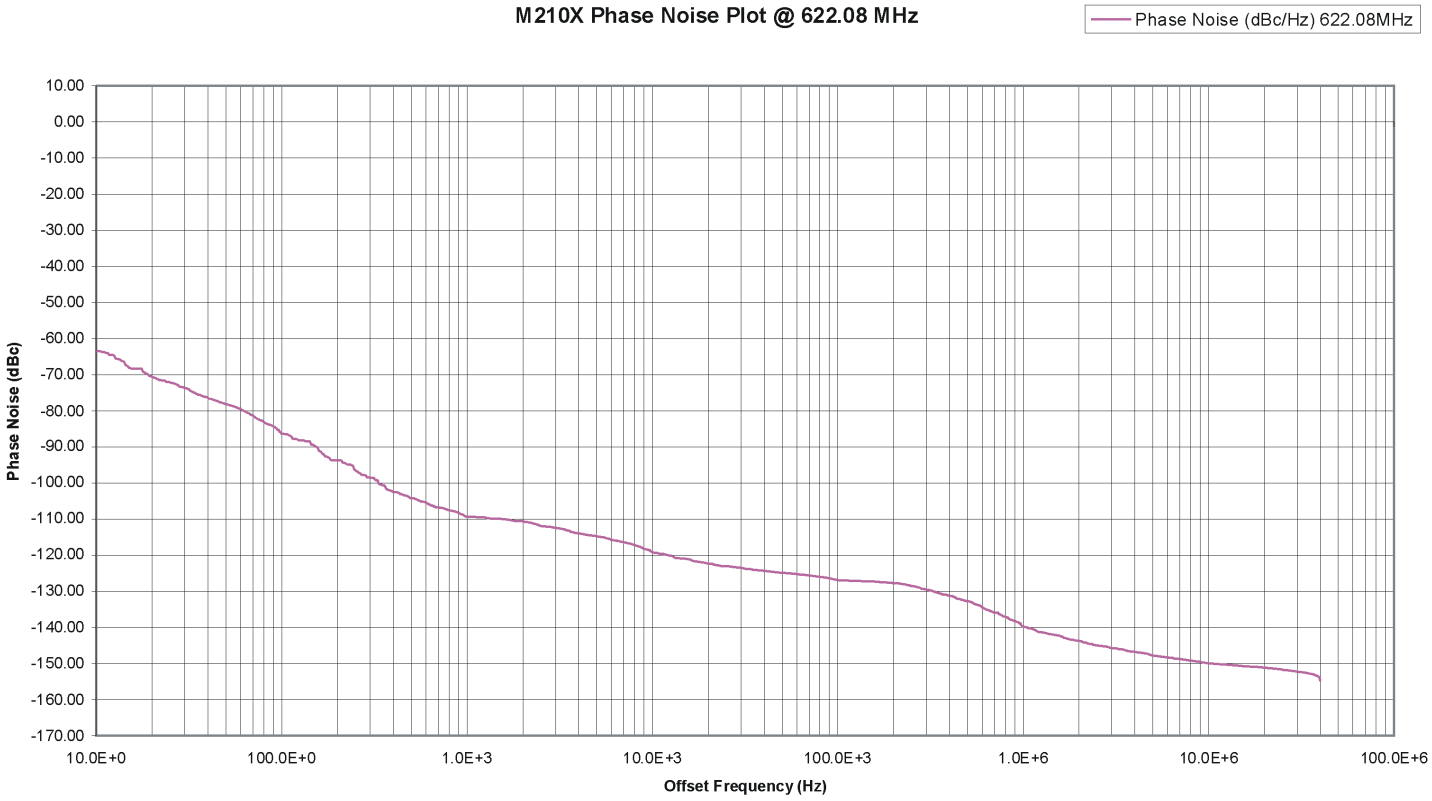
## Performance Characteristics

| | PARAMETER | Symbol | Min. | Typ. | Max. | Units | Condition/Notes |
|---|---|---|---|---|---|---|---|
| Electrical Specifications | Frequency Range | F | 150 | | 1400 | MHz | See Note 1 |
| | Operating Temperature | $T_A$ | (See ordering information) | | | | |
| | Storage Temperature | $T_S$ | -55 | | +125 | °C | |
| | Frequency Stability | ΔF/F | (See ordering information) | | | | See Note 2 |
| | Aging<br>1st Year<br>Thereafter (per year) | | <br>-3<br>-1 | | <br>+3<br>+1 | <br>ppm<br>ppm | |
| | Supply Voltage | Vcc | 1.71<br>2.375<br>3.135 | 1.8<br>2.5<br>3.3 | 1.89<br>2.625<br>3.465 | V<br>V<br>V | LVDS/CML |
| | Input Current | Icc | | | 125 | mA | LVPECL/LVDS/CML |
| | Load | | 50 Ohms to (Vcc -2) Vdc<br>100 Ohm differential load | | | | See Note 3<br>LVPECL Waveform<br>LVDS/CML Waveform |
| | Symmetry (Duty Cycle) | | 45 | | 55 | % | LVPECL – Vdd-1.3 V<br>LVDS – 1.25 V |
| | Output Skew | | | 20<br>15<br>20 | | ps<br>ps<br>ps | LVPECL<br>CML<br>LVDS |
| | Differential Voltage | Vod | 250 | 350 | 450 | mV | LVDS |
| | | Vod | 0.7 | .095 | 1.20 | Vpp | CML |
| | Common Mode Output Voltage | Vcm | | 1.2 | | V | LVDS |
| | Logic "1" Level | Voh | Vcc -1.02 | | | V | LVPECL |
| | Logic "0" Level | Vol | | | Vcc -1.63 | V | LVPECL |
| | Rise/Fall Time | Tr/Tf | | 0.23 | 0.50 | ns | @ 20/80% LVPECL |
| | Enable Function | | 80% Vcc min or N/C: Output active<br>0.5V max: Output disables to high-Z | | | | Output Option B or G |
| | | | 0.5V max or N/C: Output active<br>80% Vcc min: Output disables to high-Z | | | | Output Option S or M |
| | Start up Time | | | | 10 | ms | |
| | Phase Jitter<br>@ 622.08 MHz | <br>ϕJ | | <br>0.25 | | <br>ps RMS | <br>Integrated 12 kHz – 20 MHz |
| | Phase Noise<br>10 Hz<br>100 Hz<br>1 KHz<br>10 KHz<br>100 KHz<br>1 MHz<br>10 MHz<br>100 MHz | | | <br>-60<br>-97<br>-107<br>-116<br>-121<br>-134<br>-146<br>-148 | | | @ 622.08 MHz<br>dBc/Hz<br>dBc/Hz<br>dBc/Hz<br>dBc/Hz<br>dBc/Hz<br>dBc/Hz<br>dBc/Hz<br>dBc/Hz |

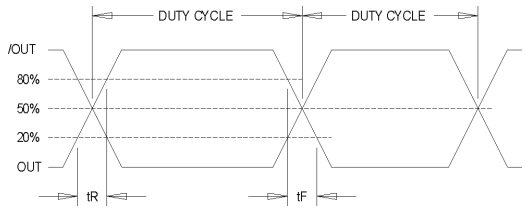
| | | |
|---|---|---|
| Environmental | Mechanical Shock | Per MIL-STD-202, Method 213, Condition C (100 g's, 6 mS duration, ½ sinewave) |
| | Vibration | Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz) |
| | Hermeticity | Per MIL-STD-202, Method 112, ($1x10^{-8}$ atm. cc/s of Helium) |
| | Thermal Cycle | Per MIL-STD-883, Method 1010, Condition B (-55°C to +125°C, 15 min. dwell, 10 cycles) |
| | Solderability | Per EIAJ-STD-002 |
| | Max Soldering Conditions | See solder profile, Figure 1 |

Note 1: Contact factory for standard frequency availability over 945 MHz
Note 2: Stability is inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging for one year at 50°C mean ambient temperature.
Note 3: See Load Circuit Diagram in this Datasheet. Consult factory with nonstandard output load requirements.

## Phase Noise Plot




## Output Waveform




**Output Waveform: LVDS/CML/PECL**

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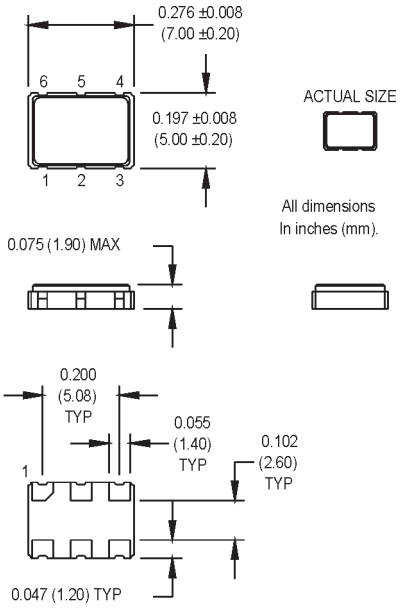
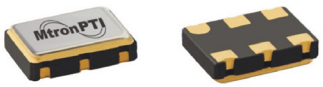
## Product Dimension & Pinout Information

### 6 Pad Standard Option

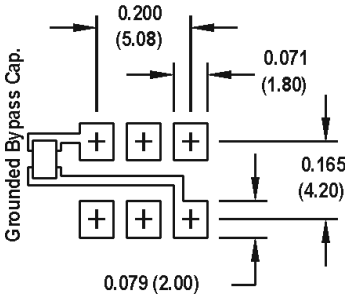



**PIN 1 ENABLE**
Pad1: Enable/Disable
Pad2: N/C
Pad3: Ground
Pad4: Output Q (LVPECL,LVDS,CML)
Pad5: Output $\bar{Q}$ (LVPECL,LVDS,CML)
Pad6: Vcc

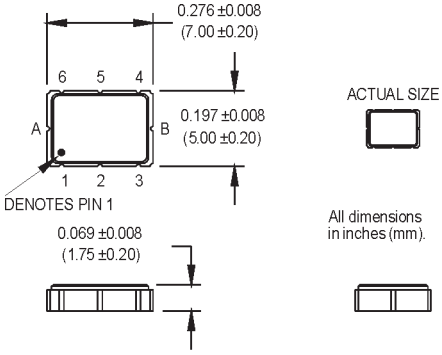
**PIN 2 ENABLE**
Pad1: N/C
Pad2: Enable/Disable
Pad3: Ground
Pad4: Output Q (LVPECL,LVDS,CML)
Pad5: Output $\bar{Q}$ (LVPECL,LVDS,CML)
Pad6: Vcc



SUGGESTED SOLDER PAD LAYOUT

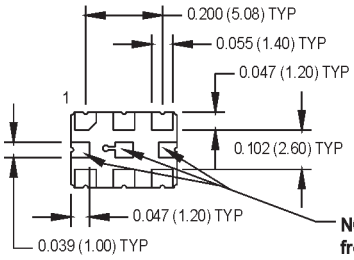



### 9 Pad Option



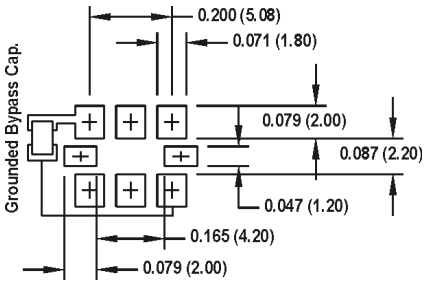

**PIN 1 ENABLE**
Pad1: Enable/Disable
Pad2: N/C
Pad3: Ground
Pad4: Output Q (LVPECL,LVDS,CML)
Pad5: Output $\bar{Q}$ (LVPECL,LVDS,CML)
Pad6: Vcc
PadA: Do not connect!
PadB: Do not connect!
PadC: Do not connect!

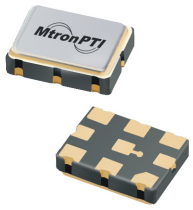
**PIN 2 ENABLE**
Pad1: N/C
Pad2: Enable/Disable
Pad3: Ground
Pad4: Output Q (LVPECL,LVDS,CML)
Pad5: Output $\bar{Q}$ (LVPECL,LVDS,CML)
Pad6: Vcc
PadA: Do not connect!
PadB: Do not connect!
PadC: Do not connect!




**NOTE: These 3 pads must be isolated from any traces or vias appearing beneath this port.**

SUGGESTED SOLDER PAD LAYOUT



## Handling Information

Although protection circuitry has been designed into the M210x oscillator, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. MtronPTI utilizes a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the mode. Although no industry-wide standard has been adopted for the CDM, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained using these circuit parameters.

| Model | ESD Threshold, Minimum | Unit |
|---|---|---|
| Human Body | 1500* | V |
| Charged Device | 1500* | V |

* MIL-STD-833D, Method 3015, Class 1


## Quality Parameters

**Environmental Specifications/Qualification Testing Performed on the M210 Clock Oscillator**

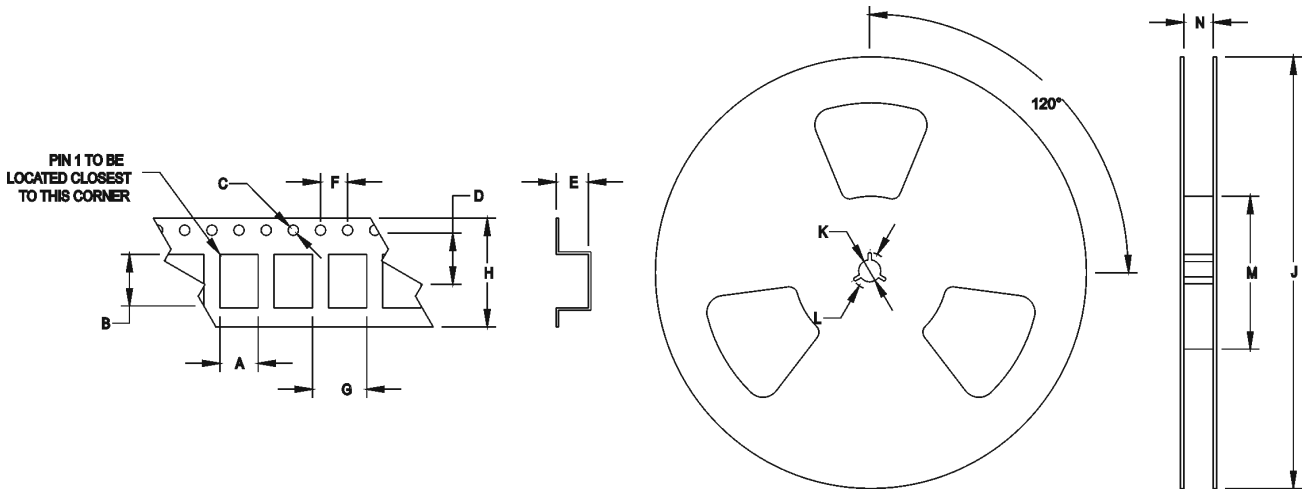
| Test | Test Method | Test Condition |
|---|---|---|
| Electrical Characteristics | Internal Specification | Per Specification |
| Frequency vs. Temperature | Internal Specification | Per Specification |
| Mechanical Shock | MIL-STD-202, Method 213, C | 100 g's |
| Vibration | MIL-STD-202, Method 201-204 | 10 g's from 10-2000 Hz |
| Thermal Cycle | MIL-STD-883, Method 1010, B | -55 Deg. C to +125 Deg. C, 15 minute Dwell, 10 cycles |
| Aging | Internal Specification | 168 Hours at 105 Degrees C |
| Gross Leak | MIL-STD-202, Method 112 | 30 Second Immersion |
| Fine Leak | MIL-STD-202, Method 112 | Must meet $1x10^{-8}$ |
| Solderability | MIL-STD-883, Method 2003 | 8 Hour Steam Age – Must Exhibit 95% coverage |
| Resistance to Solvents | MIL-STD-883, Method 2015 | Three 1 minute soaks |
| Terminal Pull | MIL-STD-883, Method 2004, A | 2 Pounds |
| Lead Bend | MIL-STD-883, Method 2004, B1 | 1 Bending Cycle |
| Physical Dimensions | MIL-STD-883, Method 2016 | Per Specification |
| Internal Visual | Internal Specification | Per Internal Specification |

## Part Marking Guide

Line 1: Model Number
Line 2: Frequency
Line 3: Date Code
Line 4: Pin 1 Indicator / MtronPTI

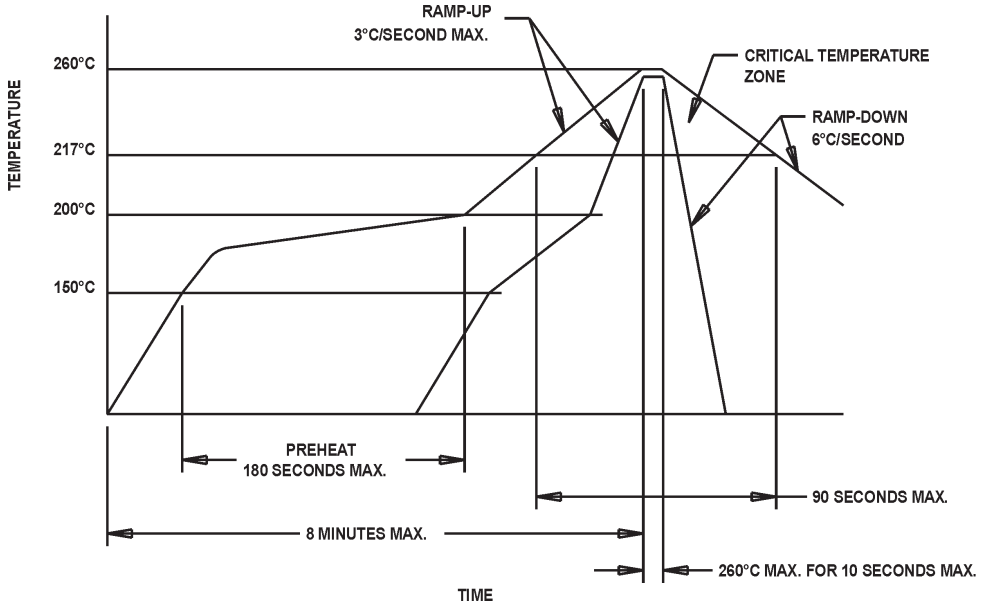
## Tape & Reel Specifications

| (all measurements are in mm) | A | B | C | D | E | F | G | H | I | J | K | L |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| M210x | 6.51 | 9.29 | 1.5 | 7.5 | 2.8 | 4 | 8/12 | 16 | 180-330 | 13 | 21 | 60-100 |




**Standard Tape and Reel:** 1000 parts per reel

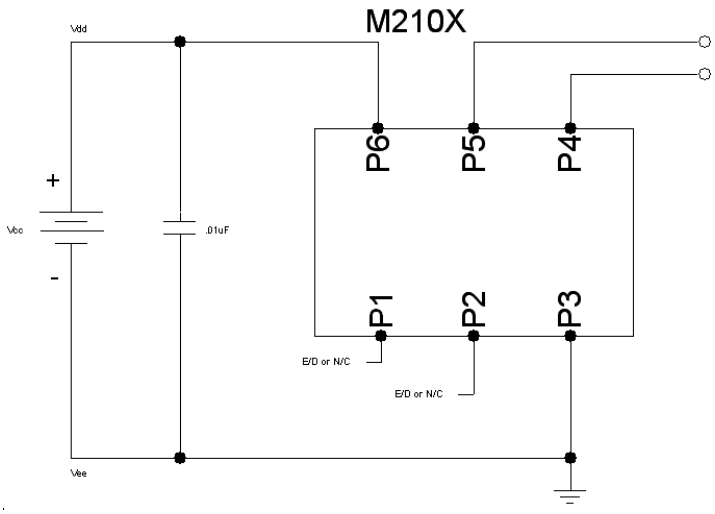
## Maximum Soldering Conditions

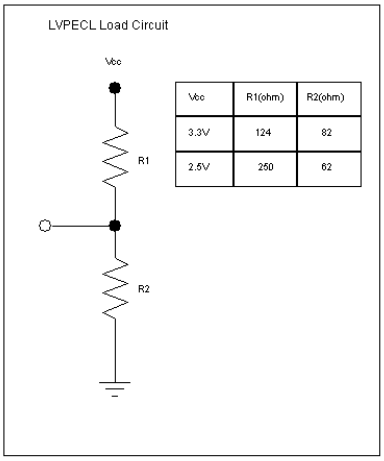


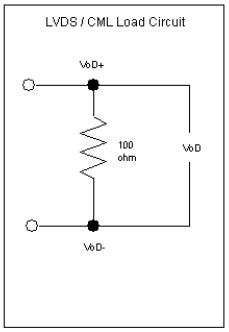

### Solder Conditions

Note: Exceeding these limits may damage the device.

## Typical Test Circuit & Load Circuit Diagrams




## Product Revision Table

| Date | Revision | PCN Number | Details of Revision |
|---|---|---|---|
| 7/20/07 | A | 10118 | IC Revision to improve phase noise and electrical performance |

For custom products or additional specifications contact our sales team at
***800.762.8800 (toll free) or 605.665.9321***

For more information on this product visit the MtronPTI website at
***www.mtronpti.com***