MMBT589LT1

High Current Surface Mount PNP Silicon Switching Transistor for Load Management in Portable Applications

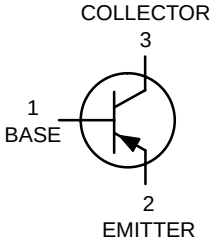
ON Semiconductor®

http://onsemi.com

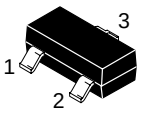
30 VOLTS, 2.0 AMPS PNP TRANSISTORS

Features

- Pb−Free Packages are Available



SOT−23 (TO−236)
CASE 318
STYLE 6



MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	−30	Vdc
Collector−Base Voltage	V_{CBO}	−50	Vdc
Emitter−Base Voltage	V_{EBO}	−5.0	Vdc
Collector Current − Continuous	I_C	−1.0	Adc
Collector Current − Peak	I_{CM}	−2.0	A

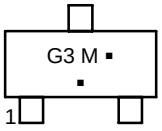
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR−5 Board, (Note 1) T_A = 25°C Derate above 25°C	P_D	310 2.5	mW mW/°C
Thermal Resistance, Junction−to−Ambient (Note 1)	$R_{\theta JA}$	403	°C/W
Total Device Dissipation Alumina Substrate, (Note 2) T_A = 25°C Derate above 25°C	P_D	710 5.7	mW mW/°C
Thermal Resistance, Junction−to−Ambient (Note 2)	$R_{\theta JA}$	176	°C/W
Total Device Dissipation (Ref. Figure 8) (Single Pulse < 10 sec.)	$P_{Dsingle}$	575	mW
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR−4 @ Minimum Pad
2. FR−4 @ 1.0 X 1.0 inch Pad

MARKING DIAGRAM



G3 = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
MMBT589LT1	SOT−23	3,000 / Tape & Reel
MMBT589LT1G	SOT−23 (Pb−Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Breakdown Voltage (I_C = −10 mAdc, I_B = 0)	$V_{(BR)CEO}$	−30	−	Vdc
Collector−Base Breakdown Voltage (I_C = −0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	−50	−	Vdc
Emitter−Base Breakdown Voltage (I_E = −0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	−5.0	−	Vdc
Collector Cutoff Current (V_{CB} = −30 Vdc, I_E = 0)	I_{CBO}	−	−0.1	μAdc
Collector−Emitter Cutoff Current (V_{CES} = −30 Vdc)	I_{CES}	−	−0.1	μAdc
Emitter Cutoff Current (V_{EB} = −4.0 Vdc)	I_{EBO}	−	−0.1	μAdc
ON CHARACTERISTICS				
DC Current Gain (Note 3) (Figure 1) (I_C = −1.0 mA, V_{CE} = −2.0 V) (I_C = −500 mA, V_{CE} = −2.0 V) (I_C = −1.0 A, V_{CE} = −2.0 V) (I_C = 2.0 A, V_{CE} = −2.0 V)	h_{FE}	 100 100 80 40	 − 300 − −	−
Collector−Emitter Saturation Voltage (Note 3) (Figure 3) (I_C = −0.5 A, I_B = −0.05 A) (I_C = −1.0 A, I_B = 0.1 A) (I_C = −2.0 A, I_B = −0.2 A)	$V_{CE(sat)}$	 − − −	 −0.25 −0.30 −0.65	V
Base−Emitter Saturation Voltage (Note 3) (Figure 2) (I_C = −1.0 A, I_B = −0.1 A)	$V_{BE(sat)}$	−	−1.2	V
Base−Emitter Turn−on Voltage (Note 3) (I_C = −1.0 A, V_{CE} = −2.0 V)	$V_{BE(on)}$	−	−1.1	V
Cutoff Frequency (I_C = −100 mA, V_{CE} = −5.0 V, f = 100 MHz)	f_T	100	−	MHz
Output Capacitance (f = 1.0 MHz)	Cobo	−	15	pF

3. Pulsed Condition: Pulse Width = 300 msec, Duty Cycle ≤ 2%

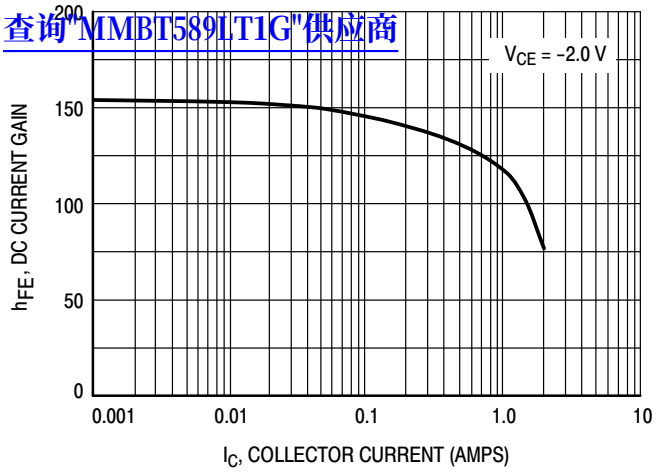


Figure 1. DC Current Gain versus Collector Current

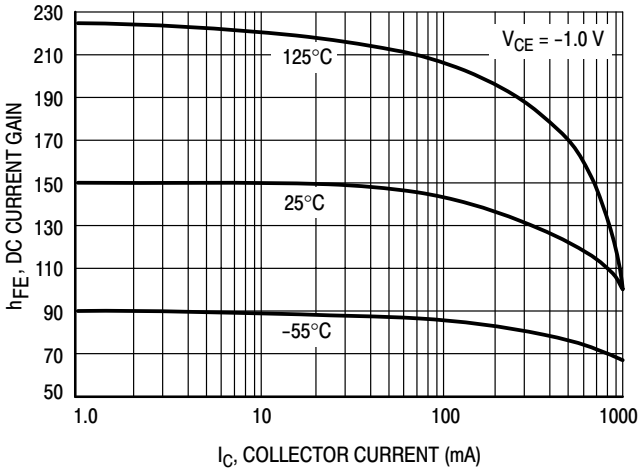


Figure 2. DC Current Gain versus Collector Current

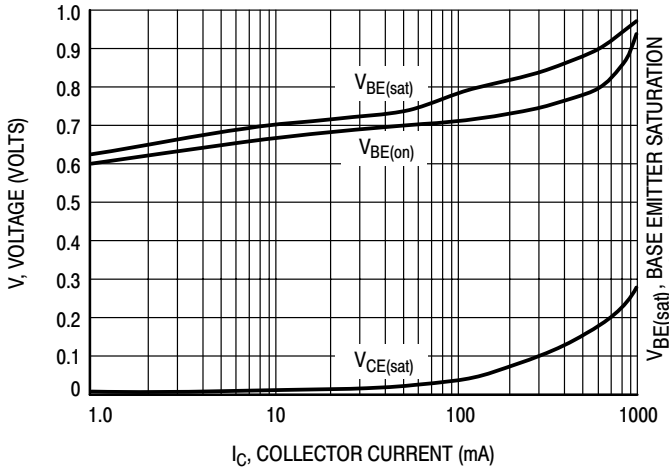


Figure 3. “On” Voltages

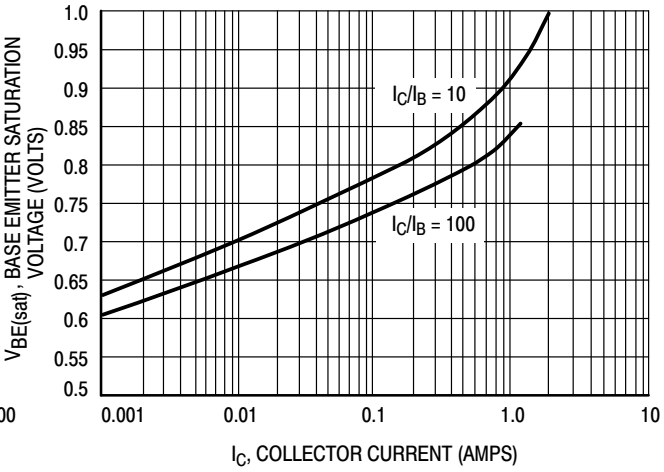


Figure 4. Base Emitter Saturation Voltage versus Collector Current

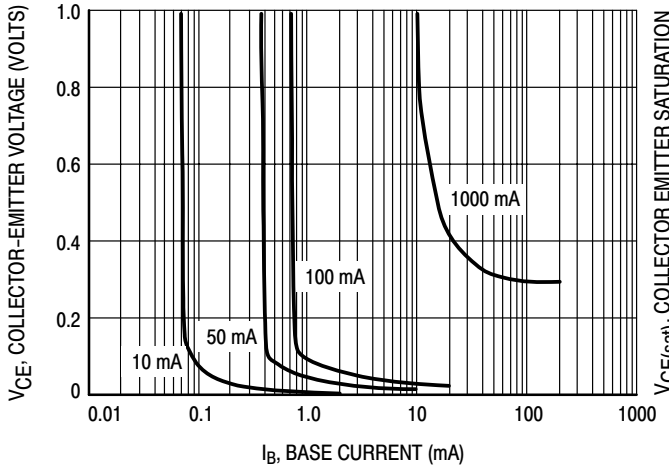


Figure 5. Collector Emitter Saturation Voltage versus Collector Current

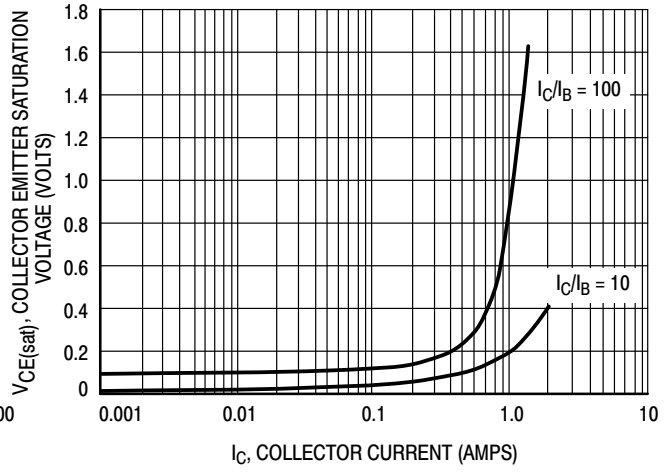


Figure 6. Collector Emitter Saturation Voltage versus Collector Current

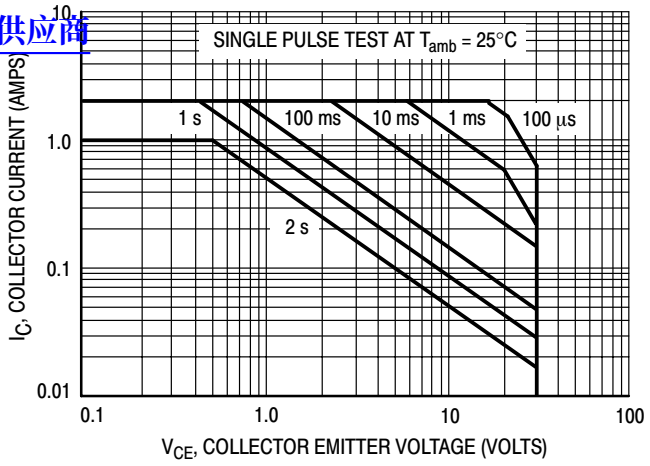


Figure 7. Safe Operating Area

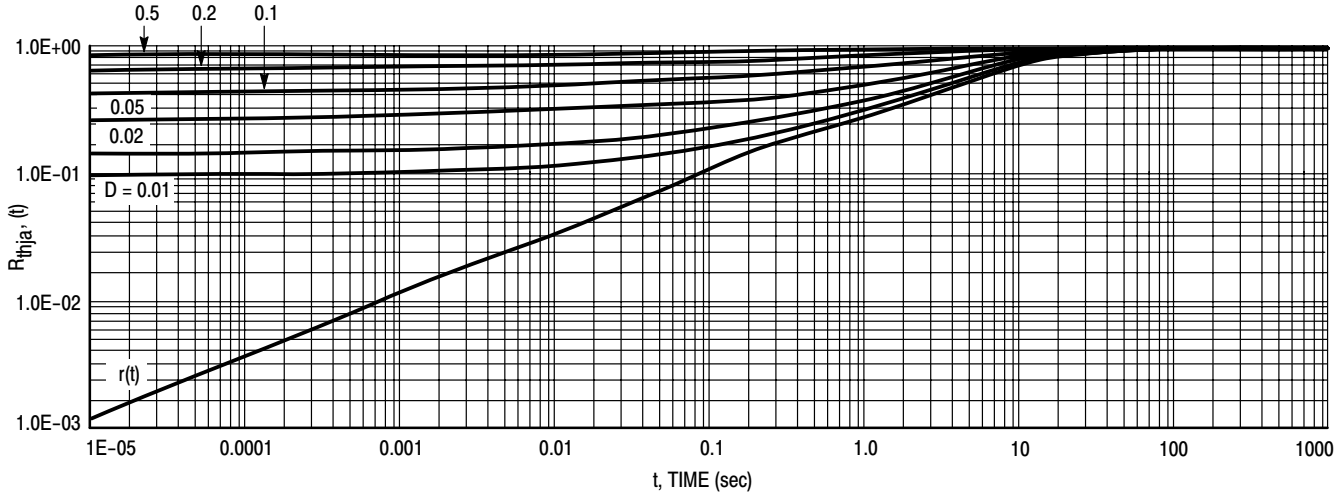
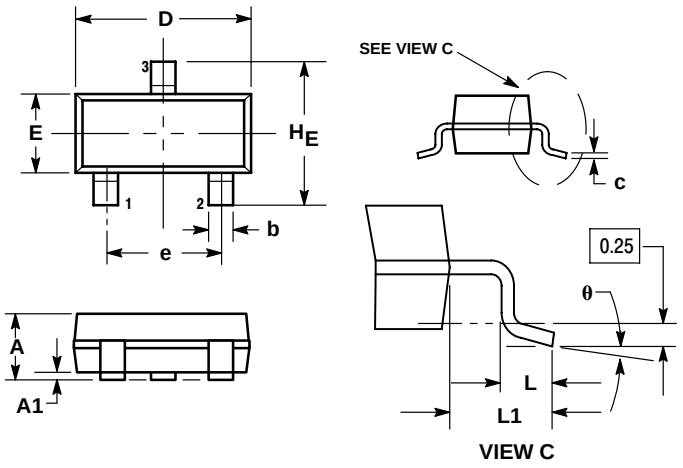


Figure 8. Normalized Thermal Response

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AN

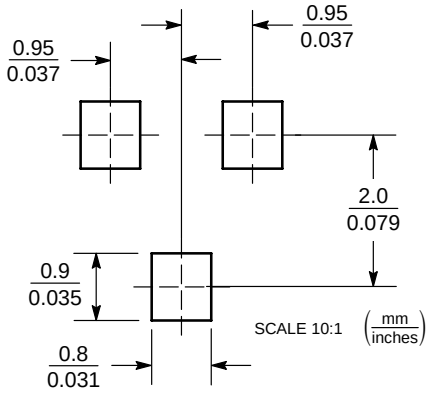


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−01 THRU −07 AND −09 OBSOLETE, NEW STANDARD 318−08.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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