SONY

DVB-T Demodulator

CXD1968AR

Description

The CXD1968AR is a 4th generation product in a successful family of DVB-T channel decoders that conforms to the ETSI (EN) 300-744 standard and demonstrates exceptional performance in the current industry regional receiver specifications including Nordig 1.0.2 and IEC (MBRAI) requirements.

This state of the art demodulator provides a fully flexible interface compatible with a wide variety of RF tuner solutions from today's common High IF or Low IF architectures to future direct conversion ZIF systems. It offers options to address the cost/performance balance for a range of DVB-T applications from digital only to digital/ analog hybrid systems. Advanced algorithms deliver optimal performance for each system configuration, while options to clock from a variety of tuner sources help to minimize system cost.

The highest technical performance is achieved through the implementation of advanced algorithms in synchronization and channel estimation, which result in robust decoding for challenging reception environments such as SFN's and portable reception. It also features an internal auto-acquisition controller that simplifies host software during scanning, and completely eliminates host software intervention during channel acquisition and recovery.

In summary, the CXD1968AR is a highly integrated DVB-T channel decoder that provides Sony's highest performance, most flexible configuration and design simplification for today's digital terrestrial receiver designs.

Applications:

- Digital terrestrial set top boxes
- Digital terrestrial PVRs and recordable DVD players
- Portable DVB-T receivers
- Terrestrial IDTV with digital only or hybrid tuner support
- PC-TV receiver modules
- DVB-T test equipment

E06905-PS

Features

- ◆ Fully complies with the ETSI EN 300-744 standard for DVB-T. Operates with all guard intervals, code rates and hierarchical modes
- ◆ Performance designed to Nordig Unified 1.0.2, EBook, DTG, IEC 62002-1/2 and EICTA (MBRAI), and all existing regional DTT specifications
- ◆ Smart auto acquisition controller for minimal host software intervention
- ◆ Operates from low cost tuner reference clock (4 to 20MHz) or standard 20.48MHz crystal for 6, 7 and 8MHz channels
- ◆ High and Low IF input frequency mode compatibility. High IF operation with all common SAW filter frequencies
- ◆ Silicon tuner Zero IF interface support with DC offset, I/Q amplitude correction and I/Q phase imbalance correction
- ◆ Impulse noise cancellation algorithm compliant with DTG and IEC (MBRAI) specification requirements
- ◆ Optimized for SFN channels with pre-cursive or post-cursive echoes, inside or outside guard interval
- ◆ Advanced channel corrector for low multipath channel loss and enhanced time varying channel performance
- ◆ Dual high performance differential 10-bit ADCs
- ◆ Digital filtering for improved ACI protection
- ◆ Digital carrier recovery with ±857kHz carrier offset recovery range including up to 3× ±1/6MHz transmitter offset
- ◆ Common Phase Error (CPE) correction
- ◆ Special features for fast 2K and 8K acquisition, including fast symbol number detection, automatic mode and guard detection
- ◆ Configurable parallel and serial MPEG2-TS interface with smoothing buffer
- ◆ Fast I^2C compatible bus interface provides access to channel SNR, individual carrier SNR, constellation data and TPS data including cell identification bits
- ◆ Very Low operating power consumption (140mW typ.)
- ◆ Standby mode including “Ultra Low” shutdown mode which stops all activity including crystal oscillator to reduce interference with analog TV and multi-tuner input systems
- ◆ Quiet I^2C output configuration for tuner control
- ◆ PWM outputs for external AGC control
- ◆ 5V tolerant inputs and outputs
- ◆ 64-pin LQFP package

1. Block Diagram

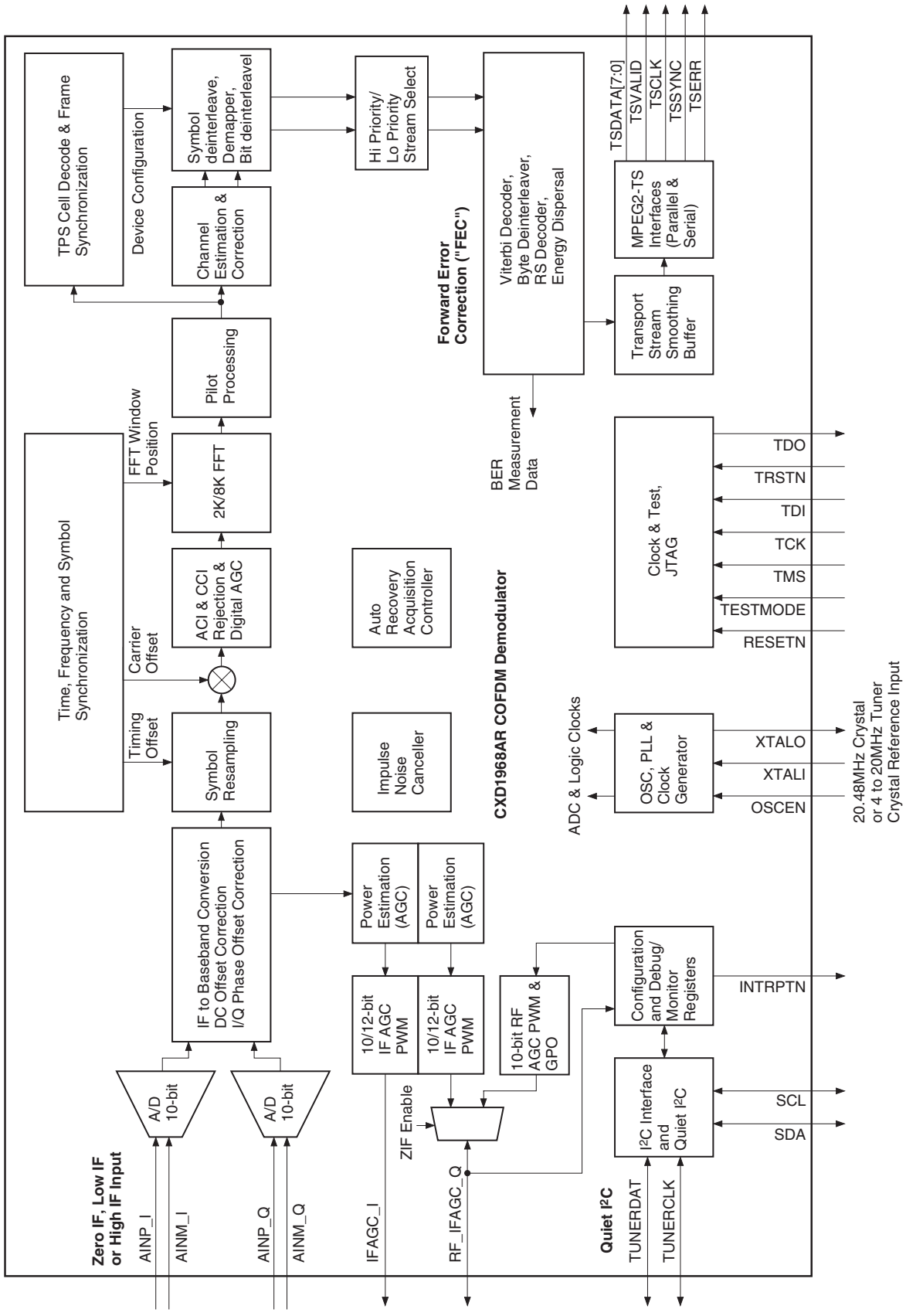


Fig. 1. Block Diagram

2. Functional Description

The block diagram of the CXD1968AR is shown in Fig. 1.

◆ Improvements over CXD1976R and CXD1973Q

The CXD1968AR incorporates some enhanced functionality over the CXD1976R. The following improvements offer performance benefits, system cost savings and simplify control of the device:

1. Auto-recovery/acquisition controller

This easy to use hardware controller eliminates the processing load on the host processor software during acquisition and will reacquire the channel if the transport stream is lost. The demodulator registers are initialized by host software after power up/reset, then the controller is enabled. The controller automatically acquires the channel selected by the tuner, and continuously monitors for loss of TS or TPS lock and reacquires the channel if necessary. This functionality also reduces host software overhead for zapping, as the host processor need only write a new channel frequency to the tuner – the demodulator will automatically acquire the new channel. The controller can also reduce host processor overhead during channel scanning. Conventional host control of the demodulator is also possible by disabling the controller.

2. Operation from a low cost tuner crystal reference

The CXD1968AR can be clocked from a standard 20.48MHz crystal (as in the CXD1976R) or from a tuner generated clock output, typically 4MHz, but can be in the range 4MHz to 20MHz by suitable programming of the PLL registers.

3. Impulse noise cancellation

This block compensates for the effects of impulse noise detected in the incoming signal using a proprietary algorithm.

4. Zero IF tuner interface

The CXD1968AR includes an optional Zero IF tuner interface to allow use of low cost silicon tuners. This interface includes several new blocks to handle typical signal impairments caused by the Zero IF tuning process:

I/Q amplitude imbalance correction (AGC)

Mismatches in the I and Q tuner signal paths can cause distortion of the I/Q signal. Dual AGC power estimation blocks individually monitor the I and Q input channels after the ADCs, and drive dual AGC amplifier PWM control outputs, allowing independent control of I and Q channel amplitudes in the tuner baseband amplifiers. The AGC gains of the I and Q channels can be read via I^2C.

I/Q phase quadrature imbalance correction (QIC)

Mismatches in the I/Q quadrature in the tuner local oscillator and signal paths can cause a uniform phase distortion of the I/Q signal across the band. This type of frequency independent I/Q phase imbalance can be corrected by this block. The detected I/Q phase imbalance can be read via I^2C.

DC offset correction

DC offsets in the input signal are estimated and removed by this block. The detected DC offset can be read via I^2C.

5. Improved ACI rejection

The Channel Selection Filter (CSF) provides additional rejection of adjacent channel interference, particularly in ZIF mode where there is reduced folding of ACI signals in-band during the ADC sampling process. This can reduce the complexity of the Zero IF tuner baseband filters.

6. Improved performance with echoes outside guard interval

The CXD1968AR includes improvements to allow pre-cursive or post-cursive echoes outside the guard interval, to meet the latest DTT specifications. This type of channel can occur in SFN networks.

7. Improved time varying channel performance

Performance has been improved in doppler channels to meet the latest DTT specifications. The symbol synchronization algorithm has also been improved to handle “birth-death” echo fading that is more likely in portable reception applications.

8. Improved reading of reserved TPS data

There are now separate “odd” and “even” banks of registers that latch the reserved TPS data including Cell-ID occurring on odd and even TPS frames. The length of the valid TPS data can also be read to determine whether Cell-ID and DVB-H signaling is present.

9. Standby power saving mode

The standby power has been reduced further. The design can enter and exit standby mode by I^2C control. The crystal or clock input is kept running in this mode.

10. Shutdown power saving mode

This is a very low power mode, where the crystal oscillator or clock input is stopped by the host processor setting the OSCEN input signal to logic 0. This prevents any clock/oscillator interference affecting analog TV reception.

◆ **COFDM Demodulator Core**

The main processing functions are;

10-bit ADC

IF Input Mode

Input to the CXD1968AR is a differential IF signal centered at either 4.57MHz or nominally 36.167MHz. The exact IF frequency can be set via the ITB_FREQ_1 and ITB_FREQ_2 registers. An integrated 10-bit A/D converter clocked at 20.48MHz is used to sample the IF signal. Input amplitude is nominally 1V peak-to-peak differential, but can also be set to 0.7V, 1.5V, or 2V peak-to-peak differential using I^2C registers.

Zero IF (ZIF) Input Mode

The I channel uses the same ADC described above for IF input signals. A second 10-bit ADC is used for the Q channel input. Both ADCs sample at 20.48MHz. Input amplitude is nominally 1V peak-to-peak differential, but can also be set to 0.7V, 1.5V, or 2V peak-to-peak differential using I^2C registers.

Power Estimation (AGC)

IF Mode

This block monitors the signal level at the output of the ADC and provides a Pulse Width Modulated (PWM) control signal to drive an external (analog) variable gain amplifier (VGA) in the tuner IF stage. This circuit operates as an automatic gain control loop and is normally configured to maximize ADC dynamic range determined by a fixed AGC target value. The enhanced AGC system modifies the AGC gain according to the characteristics of the received channel in order to better cope with interferers. The AGC output voltage is generated as a PWM signal and requires a simple external single pole RC filter to interface with the AGC system. The AGC gain value applied to the external amplifier can be read via a register to assist software RF AGC algorithms.

Zero IF (ZIF) Input Mode

In ZIF input mode, both the I and Q channels are monitored independently, each driving a separate PWM control signal (IFAGC_I, RF_IFAGC_Q) to allow separate tuner AGC amplifiers to correct for I/Q amplitude imbalances. Other features are similar to IF-mode AGC described above.

Automatic Gain Control – External RF

This block provides an additional Pulse Width Modulated (PWM) control signal (RF_IFAGC_Q) to drive the variable gain amplifier (VGA) in the tuner RF stage. The output value is set by an I^2C register. This feature is only available in IF input mode. In ZIF mode this pin is used by the Q channel AGC PWM output.

General-purpose I/O Port

The RF AGC pin can be configured to generate a logic level signal in place of the PWM output. This may be used for SAW switching, test output or other user-defined purpose. Alternatively this pin can be programed as a digital input, readable by I^2C. The above features are only available in IF input mode. In ZIF mode this pin is used by the Q channel AGC PWM output.

IF to Baseband Conversion (ITB)

This block translates the received digitized IF signal to complex baseband. Subsequent processing is performed on the complex baseband samples. This block is not used in ZIF input mode.

Symbol Resampling (ITP)

This block resamples the complex baseband data to compensate for errors between the transmitter clock and ADC sampling clock frequency thus ensuring the FFT block receives the correct number of samples per OFDM symbol. An all-digital resampling technique is used which eliminates the cost and stability issues associated with internal or external VCXOs. The timing offset can be read from an I²C register allowing external monitoring or control.

Frequency Synchronization Loop (CRL)

The frequency synchronization loop compensates for intentional transmitter carrier frequency offsets and tuner local oscillator frequency error inherent in the RF to IF conversion process. An all-digital AFC technique estimates the frequency shift using the pilots in the OFDM signal and derotates the I/Q constellation before the FFT process. Frequency offset information can be read from an I²C register. This information may be extracted during a channel scan and subsequently applied to the tuning when pre-selecting (zapping) a channel. The offset range can be programed to allow faster acquisition to broadcast channels even beyond 3 × ±166kHz transmitter offset. Scanning under software control is simplified using the extended acquisition range.

ACI and CCI Rejection and Digital AGC (CSF + CAS)

These blocks filter any residual adjacent channel interference such as NICAM energy leaking through the edges of the SAW filter. The CCI filter can optionally cancel co-channel interference such as vision carrier of an analog TV signal. Digital AGC is also performed to restore a consistent signal after filtering. The CCI filter is automatically applied in the presence of analog co-channel interference, resulting in optimum performance for the received channel. The CSF block provides extra adjacent channel rejection, particularly in ZIF mode where there is reduced folding in-band of ACI signals.

COFDM Symbol Synchronization Block (SYR)

This block acquires and tracks the position of the FFT sampling window within the OFDM symbol, to allow the FFT to recover the useful carriers including pilot tones with minimal ISI. This block can be programed to perform a fast detection of the guard time interval and mode without using TPS, reducing acquisition time. Alternatively a specific mode and guard configuration can be programed also reducing acquisition times for known channels.
The CXD1968AR utilizes a new tracking algorithm which improves symbol tracking in multipath channels, particularly beneficial for reception of SFN broadcasts where there can be echoes outside the guard interval. The algorithm permits acquisition and tracking of pre-cursive and post-cursive echo delays inside and outside the guard interval, and also automatically tracks the “birth” and “death” of echoes occurring at different delays, even if the delay of the main echo path changes. The tracker contains automatic CCI detection and filter selection further optimizing channel reception.

FFT Processor

This block performs a 2048 or 8192 point FFT on the derotated I/Q samples.

Pilot Processing and Common Phase Error (CPE) Correction (SCR and PPM)

This block corrects for the phase slope and common phase error present on the carriers due to the FFT trigger point being chosen to minimize ISI. A fast acquisition mode can be programed to allow the device to start outputting transport stream data before a full superframe has been received.

Channel Estimation

This block estimates a time varying channel frequency response using the pilot carriers embedded in every COFDM symbol. This estimate is then interpolated in the frequency domain and used to correct each of the individual OFDM carriers in the CHC block. This block also estimates the signal and noise power for each carrier, which is used as a reliability estimate to weight the soft decisions of each bit fed to the Viterbi decoder. This feature helps to improve PAL CCI performance where vision and sound carriers can distort nearby COFDM carriers.

Channel Correction (CHC)

This block uses the estimated channel frequency response to equalize the carriers against frequency selective attenuation in the channel.

TPS Cell Decode and Frame Synchronization (TPS)

The Transmission Parameter Signaling (TPS) pilots convey information used to configure the receiver and delimit the COFDM frame boundaries. This block decodes the TPS pilot carriers and generates frame synchronization signals. All the TPS information (shown below) is readable via I^2C registers.

- ◆ Length indicator – Needed to read Cell-ID and reserved TPS bits
- ◆ Frame number within superframe (0-3)
- ◆ Constellation (QPSK, 16QAM, 64QAM)
- ◆ Hierarchy information (non-hierarchical, α = 1, α = 2, α = 4)
- ◆ High priority stream code rates (1/2, 2/3, 3/4, 5/6, 7/8)
- ◆ Low priority stream code rates (1/2, 2/3, 3/4, 5/6, 7/8)
- ◆ Guard interval (1/32, 1/16, 1/8, 1/4)
- ◆ Transmission mode (2K, 8K)
- ◆ All TPS bits reserved for future use (S40-S53), such as Cell ID and DVB-H indicator bits

Symbol Deinterleaver (SDI)

The transmitter interleaves the QAM symbols to ensure that a given QAM symbol is mapped to a different carrier in each COFDM symbol, to avoid a succession of errors at the Viterbi decoder input due to frequency selective attenuation involving several adjacent carriers. The symbol deinterleaver deinterleaves the corrected carriers from the channel estimation and correction blocks together with the reliability information.

Symbol Demapper (DMP)

The demapper processes the complex symbols and reliability information issued from the symbol deinterleaver, generating weighted soft decision information for each bit.

Bit Deinterleaver (BDI)

Depending upon the QAM level used, the transmitter splits up the input data bits into 2, 4 or 6 streams which are then interleaved to ensure that consecutive input data bits are not mapped to the same QAM symbol. The bit deinterleaver reverses this process by deinterleaving the soft decision information for each bit from the Symbol Demapper. In hierarchical mode, this block outputs a high priority and low priority bit stream. In non-hierarchical mode, a single bit stream is output.

Low/High Priority Stream Select

For hierarchical transmissions, this block selects (via an I^2C register) either the high priority or low priority transport stream for processing by the remainder of the decoder as shown in Fig. 2.

◆ **Forward Error Corrector (FEC)**

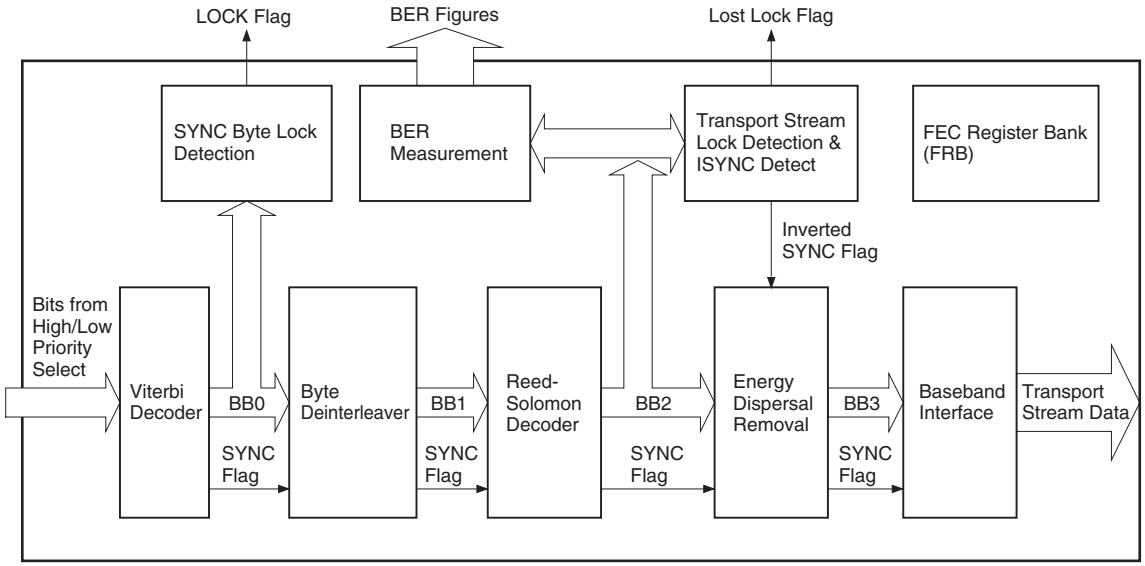


Fig. 2. FEC Block Diagram (Viterbi decoder to transport stream output only)

Viterbi Decoder (VIT)

The Viterbi decoder uses the weighted soft decision data to perform a maximum likelihood estimation of each received bit. All code rates in the ETSI (EN) 300 744 standard are supported. Bit error rates at the input and output of this decoder can be monitored via the I^2C bus. The serial bit stream output of the decoder is converted into byte wide format by a serial to parallel converter before it is passed to the byte deinterleaver.

Sync Byte Lock Detection

This block detects the MPEG2-TS sync bytes or inverted sync bytes at the output of the Viterbi decoder in order to ensure correct synchronization of the byte deinterleaving and correct identification of the inverted sync bytes.

Byte Deinterleaver

This block implements standard DVB compatible Forney type convolutional deinterleaving (I = 12, N = 204, M = 17, where M = N/I). Burst errors are split up across multiple MPEG2-TS packets, which increases the probability of successful Reed-Solomon error correction.

Reed-Solomon Decoder

This block is a DVB compatible (255,239) Reed-Solomon decoder implementing the standard DVB shortened (204,188) code using a (GF generation polynomial $p(x) = x^8 + x^4 + x^3 + x^2 + 1$) to correct up to t = 8 erroneous bytes per MPEG2-TS packet. R/S decoding errors occurring when more than 8 bytes are in error are used to calculate error statistics, and are also signaled on the MPEG2-TS interface TSERR signal.

Transport Stream Lock Detection and Sync Byte Inversion

This block detects the MPEG2-TS sync bytes and inverted sync bytes after correction by the R/S decoder in order to provide a more resilient lock detection mechanism which is called Transport Stream Lock in this document. Operation is similar to the sync byte lock detection block described above. This block also detects the inverted sync bytes, which are then inverted by the energy dispersal block.

Energy Dispersal

The error-corrected bytes are derandomized with a 15-stage PRBS (Pseudo Random Binary Sequence) generator, with polynomial $1 + X^{14} + X^{15}$ and start-up sequence “100101010000000”. Sync bytes are not derandomized, and when an inverted sync byte is detected, every 8th packet, the PRBS resets to the start-up sequence and the sync byte is reinverted. The derandomized data is output through the TSDATA pins, along with a data clock and synchronization signal.

◆ **MPEG2-TS Baseband Interface**

This block provides parallel and serial MPEG2-TS outputs. Due to the guard intervals and redundancy in the received COFDM signal, the MPEG2-TS output data can be bursty. MPEG2-TS packets can cross COFDM symbol boundaries resulting in periodic gaps between successive bytes in an MPEG2-TS packet. For this reason, the parallel and serial MPEG2-TS interfaces allow several different configurations of the TSCLOCK, TSERR, TSSYNC and TSVALID signals as described below. This block also smoothes the TS output in the time domain. This enables the serial interface to output data at the average rate rather than the peak rate and also reduces jitter on the PCR embedded in the TS.

Transport Stream Smoothing

When enabled, the transport stream smoothing function can operate in one of two modes:

- ◆ *Automatic Mode*, where the degree of smoothing is determined by reading the TPS data embedded in the DVB ensemble.
- ◆ *Manual Mode*, where the degree of smoothing is set by programming an I^2C register. In manual mode the quality of the smoothing depends on how the I^2C register is programed.

The effect of the transport stream smoothing function is different in parallel and serial modes:

- ◆ *Parallel Mode*: The frequency of the TSCLK output is almost the same as the data rate; there will be few gaps in the transport stream output (signaled by either TSVALID going inactive or a gated TSCLK – see below). These gaps will never be within the 188 valid data bytes in a packet. This is because TSCLK is slightly fast, because allowances have to be made for timing offsets between the transmitter and receiver.
- ◆ *Serial Mode*: The frequency of the TSCLK output is fixed at 41MHz (40.96MHz if a 20.48MHz crystal is used), irrespective of the data rate. The valid data outputs are spread evenly, but there will be gaps output (signaled by either TSVALID going inactive or a gated TSCLK – see below). These gaps will never be within a byte.

Parallel Output Mode

Fig. 3 illustrates the relationship between the CXD1968AR MPEG2 transport stream interface signals. The transport stream clock (TSCLK) can be programed for the external device to sample on the rising or falling edge (only rising edge sampling is shown here). The interface supports a number of additional signals, which indicate the integrity of the output data. Once the demodulator has achieved lock to the MPEG2 sync byte, the transport stream interface is activated. Fig. 3 shows a complete MPEG2 packet consisting of a sync byte (47h) data bytes (dd) and Reed-Solomon bytes (rr). Note that all the interface control signals have individual programmable polarity; active high signals are shown in the diagram.

TSCLK has two operating modes selected via I^2C:

- ◆ *Continuous Mode*, where the clock runs continuously during all 204 bytes of each packet, and during gaps between bytes, thus requiring the external device to use TSVALID to validate the 188 data and sync bytes.
- ◆ *Data Only Mode*, where the clock is activated only for each of the valid data bytes and remains inactive at all other times. There are two further sub-modes in TSCLK Data Only Mode selected via I^2C:
  - ◆ *188 Mode*, where TSCLK is active for the first 188 bytes in the TS packet.
  - ◆ *204 Mode*, where TSCLK is active for all 204 bytes in the TS packet.

TSDATA[7:0] is the byte wide MPEG2-TS data with programmable MSB/LSB ordering. The default is TSDATA7 being the MSB.

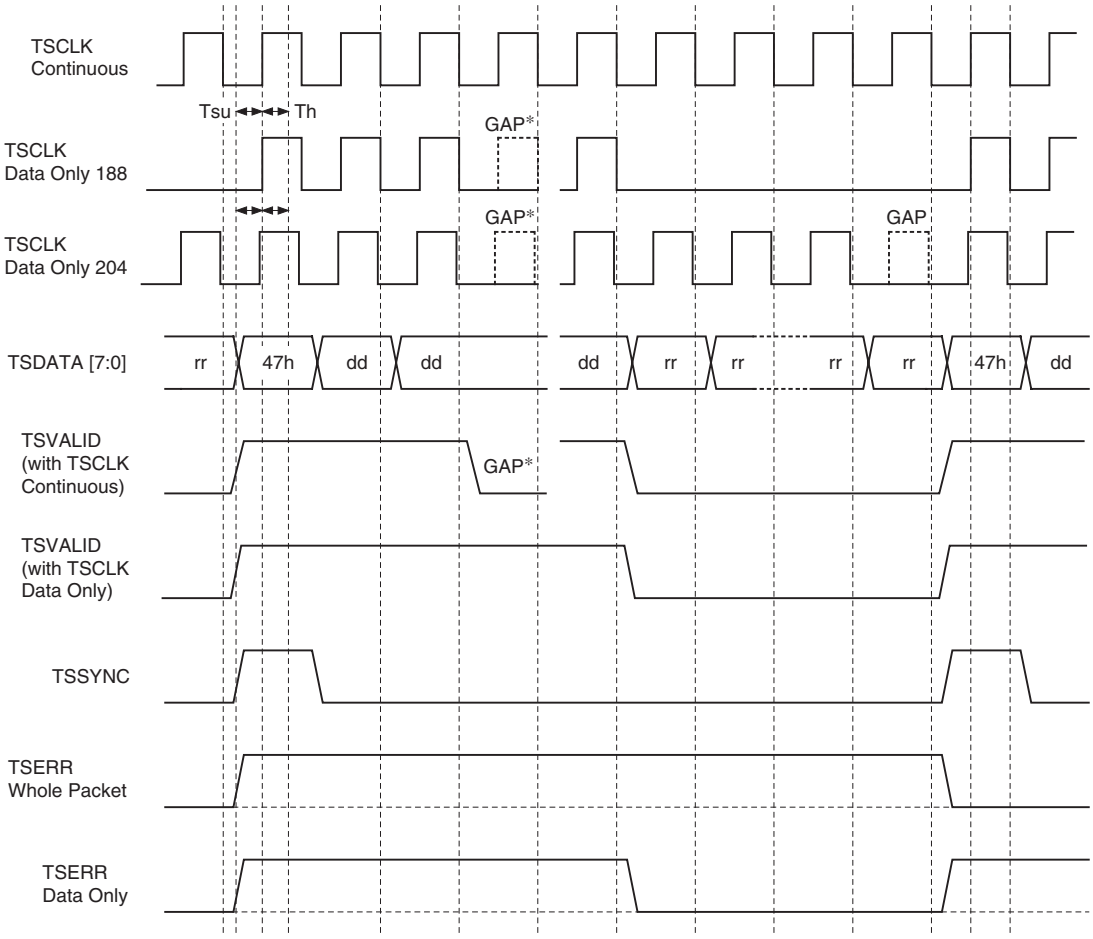
TSVALID identifies the data portion of transport stream packet (excludes R/S bytes). TSVALID has two operating modes depending on the TSCLK operating mode:

- ◆ *TSCLK in Continuous Mode*: TSVALID is set active for 1 TSCLK for each of the 188 data and sync bytes.
- ◆ *TSCLK in Data Only Mode*: TSVALID is set active during the 188 byte data portion of packet and inactive during the 16 Reed-Solomon bytes.

TSSYNC is set active during the MPEG2 sync byte and reset inactive for the remainder of the packet.

TSERR is only set active if the transport stream packet error flag is set within the MPEG2 TS. This signal indicates that the Reed-Solomon decoder was unable to correct all errors in the packet. There are 2 programmable modes for this signal:

- *Whole Packet Mode*: Active during the entire 204-byte packet.
- *Data Only Mode*: Active during the 188-byte data portion of packet and inactive during the 16 Reed-Solomon bytes.



* Gaps will not appear within the 188 valid data bytes (dd) in parallel mode if TS smoothing is enabled.

Fig. 3. MPEG2 Transport Stream Output Configurations (Parallel Mode)

Serial Output Mode

Fig. 4 illustrates the relationship between the CXD1968AR MPEG2 transport stream outputs when programed into serial output via I²C. The TSCLK can be programed for the external device to sample on the rising or falling edge (only rising edge sampling is shown here). The interface supports a number of additional signals, which indicate the integrity of the output data. Once the demodulator has achieved lock to the MPEG2 sync byte, the transport stream interface is activated. Data bits are shifted out on TSDATA0 or TSDATA7 (selectable via I²C), starting with the sync byte (47h). The remaining TSDATA signals are held inactive to reduce noise. The data bit order can be programed as MSB first or LSB first via an I²C register.

The frequency of the TSCLK output is 41MHz (40.96MHz if a 20.48MHz crystal is used) provided transport stream smoothing is enabled. It is recommended that the serial interface is only used with transport stream smoothing enabled.

Fig. 4 shows a complete MPEG2 packet consisting of a sync byte (47h) data bytes (dd) and Reed-Solomon bytes (rr). Note that all the interface control signals have individual programmable polarity; active high signals are shown in the diagram.

TSCLK has two operating modes and polarity selected via I²C. The operating modes are:

- *Continuous Mode*, where the clock runs continuously at a rate of 1 cycle per bit for all 204 bytes of each packet and during the gaps between bytes thus requiring the external device to use TSVALID to validate the 188 data and sync bytes. There are never any gaps between successive bits of the same byte.
- *Data Only Mode*, where the clock is activated only for 8 pulses on each byte output for each of the valid data bytes, and remains inactive at all other times. There are never any gaps between successive bits of the same byte. There are two further sub-modes in TSCLK Data Only Mode selected via I²C:
  - *188 Mode*, where TSCLK is active for the first 188 bytes in the TS packet.
  - *204 Mode*, where TSCLK is active for all 204 bytes in the TS packet.

Serial data can be output from either **TSDATA0** or **TSDATA7** under the control of I²C. MSB/LSB ordering is also selectable via I²C.

TSVALID identifies the data portion of transport stream packet (excludes R/S bytes). TSVALID has two operating modes selected depending on the TSCLK operating mode:

- *TSCLK in Continuous Mode*: TSVALID is set active for 8 TSCLK periods for each of the 188 data and sync bytes.
- *TSCLK in Data Only Mode*: TSVALID is set active during the 188 byte data portion of packet and inactive during the 16 Reed-Solomon bytes.

TSSYNC identifies the first byte in the transport stream packet and has two operating modes selectable by I²C:

- *Byte Mode*, where TSSYNC is set active for the first byte of the transport stream packet and reset inactive for the remainder of the packet.
- *Bit Mode*, where TSSYNC is set active for the first bit of the MPEG2 sync byte and reset inactive for the remainder of the packet.

TSERR is only set active if the transport stream packet error flag is set in the MPEG2 TS. This signal indicates that the Reed-Solomon decoder was unable to correct all errors in the packet. There are 2 programmable modes for this signal:

- *Whole Packet Mode*: Active during the entire 204-byte packet.
- *Data Only Mode*: Active during the 188-byte data portion of packet and inactive during the 16 Reed-Solomon bytes.

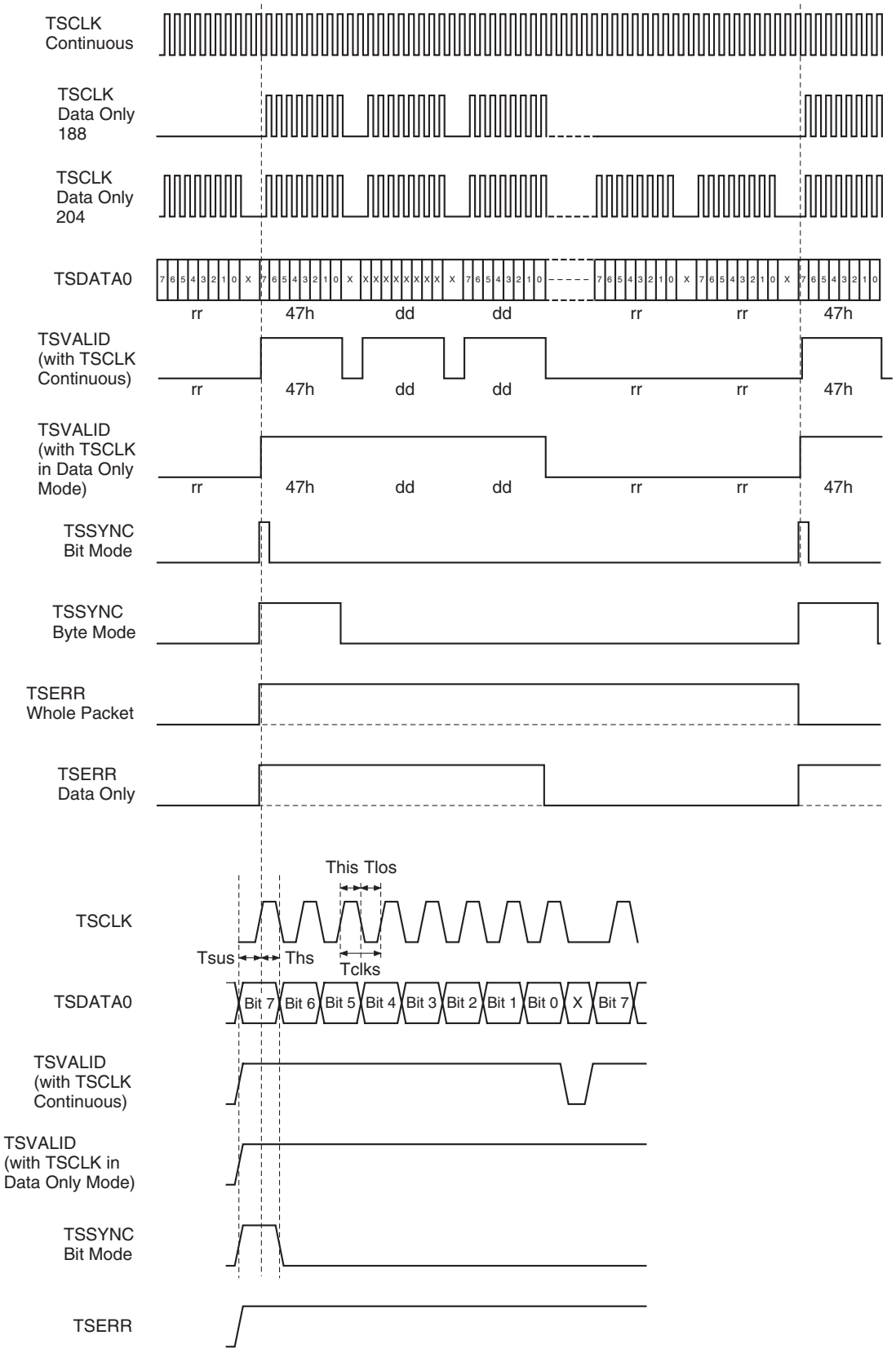


Fig. 4. MPEG2 Transport Stream Output Configurations (Serial Mode)

◆ Interrupts

The INTRPTN pin can be switched active low on the occurrence of one or more of the following conditions:

- Receipt of a TPS block
- Received TPS parameter change
- Receipt of a TPS block with a bad BCH check
- Change of AGC lock status
- TPS receive frame error
- Completion of FFT processing of the current symbol
- Occurrence of MPEG2 transport stream lock
- Loss of MPEG2 transport stream lock
- Occurrence of FEC (sync byte) lock
- Occurrence of errored second
- Occurrence of severely errored second
- Occurrence of more than 8-byte errors in transport stream packet (rejected codeword)
- TS smoothing circuit under/overflow

Separate interrupt enable and status bits for each interrupt are provided. An interrupt condition can be latched without generating INTRPTN to allow interrupt polling.

◆ Diagnostic Interface

There is a diagnostic interface, which enables the following to be read using the I^2C interface:

- Mean signal-to-noise ratio across all carriers
- Signal-to-noise ratio on each carrier
- Real and imaginary components of each carrier after channel correction
- Real and imaginary components of the channel estimate for each carrier
- Estimated noise power for each carrier

◆ BER Measurement

The CXD1968AR FEC includes comprehensive signal quality measurement logic. The current estimated Bit Error Rate (BER) of the received signal at various points in the receiver and a measure of the long-term signal quality are both available via I^2C registers. It is also possible for a highly accurate BER to be measured, with a transmitted sequence of NULL MPEG2 packets in accordance with ETSI TR 101 290 v1.2.1. The measurements available are;

1. **Pre-Viterbi decoder BER** (can be measured with real live MPEG2 datastreams)
2. **Post-Viterbi BER** can be measured in two ways:
   - Using live MPEG2 datastreams. This is an exact measurement provided each transport stream packet contains no more than 8-byte errors, and is an estimated measurement if the packet contains 8 or more errors.
   - Using MPEG2 NULL packets. This is an exact measurement based on comparison between the received packet and a stored MPEG2-TS NULL packet, and allows more than 8-byte errors in the received packet to occur without introducing inaccuracies in the BER measurement.
3. **Post R/S decoder BER** (requires MPEG2-TS NULL packets to be sent)
4. **Number of rejected codewords per second** (R/S decoder errors due to more than 8-byte errors occurring)
5. **Interrupt on occurrence of errored second** (ES, at least one rejected codeword/second)
6. **Interrupt on occurrence of severely errored second** (SES, n or more rejected codewords in a second where n is a programmable threshold)

◆ Tuner Control Interface

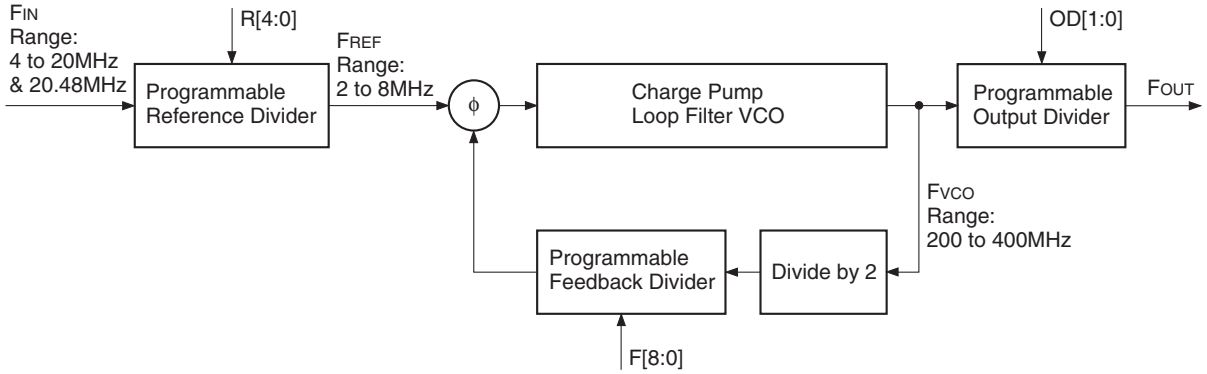
The Quiet I²C Module contained within the CXD1968AR allows the simple connection of slow I²C slave(s) to a 400kHz master by providing the necessary logic to guarantee all of the timing parameters for the slower device. If the slave is slower than 400kHz then it can use the slave acknowledge mechanism of holding the clock low between high phases. The Quiet I²C Module does not provide for multi-master arbitration.

In order to satisfy the tuner's requirement that the bus is normally quiet, the slave interface may be enabled or disabled.

◆ PLL Operation

Internal clock signals are derived from an all-digital PLL. The functionality of this circuit has been extended to allow operation with an optional external clock signal. A typical application could be to use a 4MHz clock provided by the RF tuner, permitting the removal of the 20.48MHz crystal and components.

The following diagram illustrates the configuration used to generate the internal clock signals when a 20.48MHz crystal is present.



In this example the clock source FIN is obtained from the crystal oscillator, running at a nominal 20.480MHz.

- ◆ The reference divider R[4:0] is set to ÷5 which in combination with the fixed ÷2 results in FREF of 2.048MHz.
- ◆ The feedback divider F[8:0] is set to ÷80 which in combination with the fixed ÷2 results in the VCO, FVCO running at 327.68MHz (not accessible to the user).
- ◆ The output frequency FOUT is divided by 4, OD[1:0] to give an 81.92MHz clock to the clock divider logic in the demodulator core.

Refer to the registers PLL_FODR (0xA7) and PLL_F (0xA8) for detailed programming information and a table of register settings for the supported external clock and crystal frequency combinations. The application note EAN-0066 provides programming examples.

Note) The internal clock frequency of 20.48MHz can change to 20.50MHz for some clock configurations. This will require alternative values of ITB_FREQ and TRL_NOM_RATE.

◆ JTAG Test Interface

Test Mode

The JTAG interface consists of five test pins available on the CXD1968AR. These are used only for embedded test and should be inactive for normal device operation. These pins are;

TRSTN	Pin 34
TDO	Pin 30
TDI	Pin 31
TMS	Pin 32
TCK	Pin 29

The JTAG interface conforms to the “IEEE 1149.1 Joint Test Action Group (JTAG)” standard.
The following instructions are available:

Instruction	Code
BYPASS	1111
EXTEST	0000
SAMPLE/PRELOAD	0001

Normal Device Operation

The input functions of this group have very weak internal pull-ups present on the pins. This is primarily to ensure that these pins cannot be left floating, a condition which could cause the device to draw excessive current.

Under circumstances that may be influenced by board layout and supply power-up effects, the JTAG circuit can be inadvertently activated in parallel with the normal operation of the demodulator. This results in the main I^2C bus locking.

This condition is readily identified but cannot be resolved without either a hardware reset or power-down. Once the main I^2C bus has locked it is not possible to communicate with the chip, hence only an external reset will permit resumption of normal operation.

If JTAG functionality is not required, the interface should be disabled to ensure this mode cannot be initiated. This is implemented by forcing the test block into permanent reset. The TRSTN and TCK inputs should be grounded.

For users who wish to implement the JTAG test mode in their equipment, it will be unacceptable to permanently ground the TRSTN and TCK inputs. It is suggested that these inputs are pulled to ground by an external resistor. A pull-down value of 10kΩ is recommended, however the choice of value will depend upon the driver circuit and speed of operation. This is illustrated in the application circuit in section 4.

3. Description of Operation

This section describes the operation of the CXD1968AR DVB-T COFDM demodulator IC and how to make use of these features when operating the device. It does not give a detailed description of the enhanced modes of operation, users should refer to the separate engineering application notes for additional information about these configurations and uses.

The following descriptions apply to the CXD1968AR used with a tuner providing a High IF signal at a nominal frequency of 36.1667MHz. Contact Sony for configuration recommendations when operating with Low IF (4.5MHz) or Zero IF at the e-mail support address CXD1968_support@eu.sony.com

EAN-0065 and EAN-0066 are intended to assist users familiar with its predecessor the CXD1976R, and intend to make the transition to the CXD1968AR.

Engineering Application Notes are available for download to registered users from the Sony Technical Library http://www.sonybiz.net/semiconductor.

◆ Processor Interface

The CXD1968AR must be configured by a host controller, which is required for initialization and to monitor its performance by writing and reading the CXD1968AR internal registers. The CXD1968AR controller interface is a serial interface which corresponds to the I²C standard. The I²C interface supports access at bit rates up to 400kbit/s.

The I²C uses an 8-bit address:

- The first 6 significant bits relate to the device type and are fixed at 110110.
- A single external address pin A0 is provided so that 2 different I²C slave address locations can be used. This permits multiple front-end configurations, for instance PVR application.
- The least significant bit is set to “1” for a write and “0” for a read.

Address pin	CXD1968AR I²C address	
A0	Binary	Hexadecimal
0	1101 100 R/W	D8h + R/W
1	1101 101 R/W	DAh + R/W

Examples used in this document assume an I²C address of 0xD8.
Reference to 0xD8 indicates a *write* instruction and to 0xD9 indicates a *read* instruction.

Multibyte Reads

Some registers contain fields more than 8 bits which are each accommodated across two or three registers. It is therefore possible for the field value to change in the time between two reads from the register pair. When a “1” is written to the freeze bit in the PIR_CTL register (whether it was previously “0” or not), the field values are latched and the multibyte value can be read without fear of reading a corrupt value. With the freeze bit set to “0” the data within the fields changes dynamically.

◆ Tuner Quiet I²C Interface

The tuner I²C interface allows the I²C interface to the tuner to be isolated from the host I²C interface to the rest of the system. This uses on-chip switching.
When an I²C master wants to send data to the tuner, it must first enable the slave interface before sending the data. To enable the tuner Quiet I²C interface the enable_quiet_I2C bit must be set in the TUNER_CTRL5 register (bit 7 at register address 0xAF).
The normal sequence of operation is;

1. Set the enable_quiet_I2C bit in TUNER_CTRL5.
2. Send/Receive the tuner I²C address and data as if it were being accessed directly by the host controller.
3. Reset the enable_quiet_I2C bit in TUNER_CTRL5.

```
Example: 0xD8   0xAF   0x80      ; enable quiet I²C bus
         0xC0   0xAA   0xBB...   ; read/write any number of messages
                                 ; to tuner @ address 0xC0 for example
         0xD8   0xAF   0x00      ; disable quiet I²C bus
```

◆ Reset

There are three types of reset. A hard reset is initiated at power up; cold and warm resets are initiated by programming the RST_REG register (below). With cold and warm resets, the host controller determines the type of reset and which parts of the CXD1968AR are to be reset.

Hard Reset

A hard reset is applied to all the CXD1968AR logic. A hard reset is initiated at power up by driving the RESETN pin low for more than 28ns. When the CXD1968AR is powered up, it must be hard reset. Whenever a hard reset occurs, the PLL will be out of tune. It must not drive logic until it has tuned. This is prevented by the reset to any PLL clocked logic being held in reset after a hard reset. The host controller must configure then enable the PLL output and release this reset after the PLL has tuned. The PLL output is enabled by setting the PLL_op_enable bit in the PLL_CONTROL register. The reset is released when the host controller resets the “hard” bit of the RST_REG register. The PLL tunes in 500μs.

Cold Reset

A cold reset is initiated by setting the cold bit in the RST_REG register, and resets any modules that are selected by the RST_REG register, including their I²C registers.

Warm Reset

A warm reset is initiated by setting the warm bit in the RST_REG register, and resets any modules that are selected by the RST_REG register, excluding their I²C registers.

◆ COFDM Demodulator Configuration

While there are many registers which can be programed to configure the COFDM demodulator, there are only a few which must be programed to setup the interface to the tuner. The following must be configured:

- Configure clock, PLL and ADC
- Set ITB frequency for chosen IF frequency
- Set TRL nominal rate for current channel bandwidth
- IF AGC sense *if required*
- Input spectrum inversion *if required*

Clock, PLL and ADC Configuration

This means setting the clock mode for operation using the internal oscillator (crystal) or from an external clock source (tuner). PLL divider settings according to the oscillator or clock frequency. The ADC powers-up in dual channel mode (defaults to ZIF input), for IF mode the unused Q channel is then turned-off.

A description has been given in section 2, PLL Operation, with reference to the application note EAN-0066 which includes code samples. Standard operation is described here with a 20.48MHz crystal.

```
Example:  0xD8  0xA7  0x6A   ; PLL comparison frequency and input divider
          0xD8  0xA8  0x50   ; set PLL feedback divider
          0xD8  0xA9  0x00   ; power up the PLL
          wait 500µs minimum ; PLL settling time
          0xD8  0xA9  0x20   ; enable PLL output
          0xD8  0xA2  0x00   ; clear hard reset
          0xD8  0xBA  0x43   ; enable clocking from the crystal
          0xD8  0xB9  0xB2   ; power down ADC_Q
```

Signal IF Frequency

The ADC input IF frequency is programed via the ITB_FREQ_1, 2 registers. These make up a 14-bit value – ITB frequency (**I**F-**T**o-**B**aseband). This value is calculated using the following formula:

$$\text{ITBFREQ} = \frac{-1 \times F_{IF}}{F_{ADC}} \times 16384$$

If the IF is being undersampled (as will be the case with a High IF signal input) then F_{IF} is the subsampled IF, thus for a 36.1667MHz IF a derived value of 4.79MHz should be used in the equation ($2 \times 20.480\text{MHz} - 36.1667\text{MHz} = 4.79\text{MHz}$):

IF mode	IF [MHz]	F_{IF} [MHz]	F_{ADC} [MHz]	ITBFREQ
Low	4.57	4.57	20.48	–3657 (31B7h)
High	36.00	4.96	20.48	–3968 (3080h)
High	36.125	4.835	20.48	–3868 (30E4h)
High	36.1667	4.7933	20.48	–3835 (3105h)
High	36.1667	4.8333	20.50	–3863 (30E9h)
High	36.00	5.00	20.50	–3996 (3064h)

```
Example:  0xD8  0x0C  0x05   ; write ITBFREQ in two bytes for
          0xD8  0x0D  0x31   ; 36.1667MHz IF and 20.48MHz clock
```

It is important that the ITB frequency should be calculated using the correct ADC clock frequency.

Note) The spectrum invert bit in register ITB_CTL 0x0B may need to be set for Low IF operation, this may also depend upon the tuner.

Channel Bandwidth

The channel bandwidth is set indirectly by programming the TRL_NOMINALRATE_0, 1, 2 registers. TRLNOMINALRATE has changed from a 16-bit number on the CXD1976R to a 24-bit number on the CXD1968AR. These registers set the nominal rate of the sample timing NCO. TRL nominal rate is the ratio of the FFT time sample clock to the (fixed) ADC clock frequency. The following formula should be used to determine the TRLNOMINALRATE value:

$$TRLNOMINALRATE = \frac{16 \times ChanBW}{F_{ADC} \times 7} \times (2^{24})$$

Note that the maximum allowable value of this register is 16777215 and the minimum is 11184811. Some common settings are given below, calculated for 20.48MHz and 20.5MHz clocks:

Channel bandwidth	F_{ADC} = 20.48MHz	F_{ADC} = 20.5MHz
8MHz	14979657 (E49249h)	14965043 (E45933h)
7MHz	13107200 (C80000h)	13094412 (C7CE0Ch)
6MHz	11234743 (AB6DB7h)	11223782 (AB42E6h)

Example: 0xD8 0x65 0x49 ; write TRL_NOMINALRATE in three bytes
0xD8 0x1B 0x92 ; for 8MHz RF channel
0xD8 0x1C 0xE4 ; and 20.480MHz clock

Note) Error in the calculation of TRLNOMINALRATE more than 50ppm may compromise acquisition of 8K transmissions.

Using Other IF Input Frequencies

IF signals outside the range 4.50MHz to 4.57MHz and 36.000MHz to 36.1667MHz are not recommended.

IF AGC Sense

The IF AGC sense is programed by setting the AGC_neg bit in the AGC_CTL register. When set the AGC level output decreases when a larger signal is required, otherwise the AGC level output increases when a larger signal is required.

Most tuners will not require this bit setting, so the register may not need to be programed.

Spectrum Inversion

The spectrum can be inverted to allow a reversed frequency spectrum from the tuner by setting the ITB invert spectrum bit in the ITB_CTL register.

This may be required for operation with dual-conversion and Low IF architecture tuners.

◆ Forward Error Corrector Configuration

Operation of the FEC block can be optimized by overriding some of the default register values. The following should be configured:

- Viterbi auto-reset
- Sync detect
- TS output mode

Viterbi Block

The disable bit in the AUTO_RESET register should be reset to optimize acquisition (the default value does not give optimum performance).

Example: 0xD8 0xB1 0x00 ; enable Viterbi auto-reset

FEC Block

The SET_SYNC_DETECT register should be set to 0x67 for optimum performance (the default value of 0xD6 does not give optimum performance).

Example: 0xD8 0x86 0x67 ; set sync detect

Transport Stream Outputs

Also, in order to obtain a watchable picture after TS lock, the transport stream outputs must be enabled (normally these are tri-stated on power-up) by clearing bit 1 of FEC_PARAMS register. The following lines enable the most commonly used parallel TS output format:

Example: 0xD8 0x80 0x18 ; enable parallel mode
0xD8 0x81 0xF4 ; preferred TS configuration

◆ COFDM Signal Acquisition

There are three stages in acquiring and locking to a COFDM signal. First, the COFDM demodulator must acquire the signal; then the FEC must synchronize to the Viterbi decoder output; finally, the FEC must synchronize to the transport stream.

The CXD1968AR contains a new auto-recover algorithm. This is a hardware implementation which automatically reacquires an interrupted signal without intervention from the host controller. After the initial setup this minimizes the load on the host processor.

The recommended method of operating the demodulator is to;

1. Configure the clocks and registers as described in the application note EAN-0066 and explained above.
2. Enable the core which will result in an acquired channel if present.
3. Set the auto-recover enable bit for automatic acquisition on any channel change.

This uses the default acquisition mode and will acquire the channel regardless of the DVB-T mode.

Default Acquisition

In this mode, nothing need be known about the transmission parameters (except the channel bandwidth). The COFDM demodulator tries all the guard intervals in the two modes (2K and 8K) and then waits until it has received a whole super-frame before decoding the TPS data and configuring itself to receive that particular COFDM signal. Signaled TPS data in the stream is valid for the NEXT super-frame so the decoder may have to wait for 5 frames – 1 symbol (= 339 symbols) before it can use the received transmission parameters.

Typical acquisition times for this mode: 125ms (2K) / 500ms (8K).

Settings for Faster Acquisition

There are several short cuts that can be taken to speed up acquisition. These depend on how the control registers are programed. It is not generally recommended that the user overrides the default settings unless the host processor has sufficient resources available.

Transport Stream Locking

FEC lock occurs at the input of the Reed-Solomon decoder when the number of sync bytes (47h) measured exceeds a certain value in the SET_SYNC_DETECT register. Transport Stream (TS) lock occurs at the output of the Reed-Solomon decoder, and uses the same mechanism as FEC lock.

The SET_SYNC_DETECT register can be used to adjust the criteria for gaining/losing lock. The higher the number of bytes required to gain lock, the harder it is to acquire lock, but, once acquired, the chip should be less likely to lose lock. Lock can be lost either by counting the number of missed sync bytes (Decrement mode) or one missed sync byte can lose lock straight away (Reset mode). Reset and decrement modes are independently settable for TS lock and FEC lock.

Example: 0xD8 0x86 0x67 ; recommended configuration

Reacquisition

It may be necessary to reacquire a COFDM signal, for example if the user were to select a different RF channel, because of reception problems with a poorly sited set-top aerial or to simplify channel scanning. It is recommended to use the auto-recovery algorithm and default acquisition settings to minimize host processor overhead.

The auto-recovery block has two modes of operation, scanning and zapping.

Scanning mode will tell the auto-recovery state machine to attempt only 1 acquisition when enabled, after which it falls back to an idle state. The status can read by the host processor, ie. TPS and/or TS lock at the end of acquisition. Note that ready bits will indicate if the status readings are valid, ie. the process has completed.

Zapping or channel change mode, also to be used during static operation to automatically recover a lost signal. In this mode the auto-recovery state machine will continuously monitor the demodulator status and reacquire when TPS/TS lock is lost. It is not necessary to read the status as it will continue to operate until disabled.

◆ **Transport Stream Outputs**

Transport stream data is output on the TSDATA outputs; it is clocked by the TSCLK output. The TSSYNC output is active during the first byte of a TS packet. The TSVALID output can be used to indicate valid data. The TSERR output indicates a TS packet containing uncorrected errors. The TSLOCK output is set active high when a valid transport stream is locked on to.

Enabling/Disabling the Transport Stream Output

The transport stream outputs are enabled by setting the Tri_State_Outputs bit in the FEC_PARAMS register.

Serial/Parallel Data Output Selection

The default transport stream output mode is parallel. A serial output can be selected by resetting the TS_parallel_sel bit in the FEC_PARAMS register.

Other Transport Stream Output Format Options

The default output format is as below:

- ◆ In parallel mode, the MSB is output on the TSDATA7 pin, the LSB on TSDATA0. In serial mode, the MSB is output first and the LSB last all on TSDATA0.
- ◆ Data should be sampled on the rising edge of TSCLK.
- ◆ TSVALID, TSSYNC and TSERR are all active high.
- ◆ TSVALID active high indicates a valid data.
- ◆ TSERR is active for the first 188 bytes if that packet contains an uncorrected error.
- ◆ TSCLK is gated so that edges occur when TSVALID is active.

The following options are available and can be selected by programming the FEC_PARAMS and BB_PARAMS registers:

- ◆ In parallel mode, the MSB can be output on TSDATA0 and the LSB on TSDATA7, and in serial mode the LSB can be output first and the MSB last by setting the Output_Sel_MSB bit in the FEC_PARAMS register.
- ◆ In serial mode, data can be output on TSDATA7 by setting the Ser_data-on_MSB bit in the FEC_PARAMS register.
- ◆ TSVALID, TSSYNC and TSERR can all be set active low by resetting the TSvalid_active_high, TSsync_active_high and TSerr_active_high bits respectively in the BB_PARAMS register.
- ◆ In parallel mode, the TSVALID output can be set to be active only during the first byte of a packet by setting the TSvalid_pulse bit in the BB_PARAMS register.
- ◆ TSERR can be set to be active only during the first byte (or bit in serial mode) by setting the TSerr_pulse bit in the BB_PARAMS register. If this bit is reset, then TSERR can be set to be active until the start of the next non errored TS packet by setting the TSerr_full bit in the BB_PARAMS register.
- ◆ TSCLK can be set to be active continuously by setting the TSclk_full bit in the BB_PARAMS register.

Transport Stream Smoothing

COFDM demodulation is naturally bursty. The demodulator operates on whole symbols of data at a time. A whole symbol must be stored before FFT processing can begin. Transformed data is read out of the FFT block as fast as possible into the following circuitry, resulting in a bursty TS. This bursty TS output can be smoothed by the on-chip TS smoothing buffer.

The TS smoothing buffer is enabled by setting the ENABLE bit in the SMOOTH_CTRL register. The smoothing buffer can operate in an automatic or manual mode.

Automatic Mode

In automatic mode, the smoothing buffer applies the correct degree of smoothing for the COFDM signal being demodulated. Automatic mode is set by setting the DATA_PERIOD_AUTO bit in the SMOOTH_CTRL register. The channel bandwidth must also be programed into the SMOOTH_CTRL register using the CHANNEL_WIDTH bits.

Example: 0xD8 0xB4 0x03 ; enable automatic mode for 8MHz channel

Manual Mode

In manual mode, the degree of smoothing must be programed into the SMOOTH_DP1, 0 registers. The SMOOTH_DP0 register bits represent the fractional number of clock periods per TS word. A read from the SMOOTH_DP0 register returns the current value of the fractional part of the data period value.

A read from SMOOTH_DP0 also causes the current value of the integer part of the data period value to be stored in a holding register, which can be accessed by reading from SMOOTH_DP1. For this reason it is recommended that SMOOTH_DP0 and SMOOTH_DP1 are read as a pair of registers, SMOOTH_DP0 first, followed by SMOOTH_DP1.

Writing to SMOOTH_DP0 only has an effect when the DATA_PERIOD_AUTO bit of the SMOOTH_CTRL register is set to “0”. In this case, writing to SMOOTH_DP0 has the effect of storing the 8-bit value in a holding register. Writing to SMOOTH_DP1 then has the effect of transferring data from the holding register to the SMOOTH_DP0 register proper. As with read accesses, it is recommended that write accesses to SMOOTH_DP0 and SMOOTH_DP1 are performed in pairs, SMOOTH_DP0 first, followed by SMOOTH_DP1.

The SMOOTH_DP0 register bits represent the integer number of clock periods per TS word. A read from the SMOOTH_DP1 register returns the integer part of the data period value previously stored in a holding register when a read from the SMOOTH_DP0 register occurred (see SMOOTH_DP0 above).

Writing to SMOOTH_DP1 only has an effect when the DATA_PERIOD_AUTO bit of the SMOOTH_CTRL register is set to “0”. In this case, writing to SMOOTH_DP1 has the expected effect of updating the SMOOTH_DP1 register value, and has the additional effect of transferring data from a holding register (updated during a SMOOTH_DP0 write operation) into the SMOOTH_DP0 register (see SMOOTH_DP0 above).

Monitoring the Smoothing Buffer Status

The status of the smoothing buffer can be monitored by reading the SMOOTH_STAT register.

The UNDERFLOW flag is set when an underflow condition has been detected. An underflow condition is where data is requested but cannot be provided because the read FIFO is empty. Note that when data is requested but cannot be provided because the next TS word is a sync and at the same time the SRAM FIFO does not contain a complete TS packet, this is part of the smoothing circuit's normal operation and is not classed as an underflow condition. Write a “1” to this bit location to clear this bit. Writing a “0” to this bit has no effect.

The OVERFLOW flag is set when an overflow condition has been detected. Write a “1” to this bit location to clear this bit. Writing a “0” to this bit has no effect.

Example: 0xD8 0xB5 0x03 ; to clear smoothing buffer status flags

◆ AGC

There are two AGC outputs from the CXD1968AR – one for the RF tuner stages and one for the IF tuner stages. These generate PWM outputs that need to be integrated off-chip to provide an analog control signal to drive an external variable gain amplifier (analog VGA) in the tuner. Each integrator is implemented with a simple external single pole RC filter, values selected to give a cutoff frequency of 400Hz, removing the high frequency components.

RF AGC

The RF AGC outputs a PWM value via the RF AGC pin, which has been programed into the RF_IFAGC_CTRL0 and RF_IFAGCQ_PWM registers (renamed to cover the new ZIF AGC modes). The RF AGC pin is enabled by setting the RF_AGC_EN bit in the RF_AGC_CTRL0 register.

The RF AGC pin may alternatively be used as a logic I/O pin, see below.

IF AGC

The IF AGC outputs a PWM value via the IF AGC pin. The AGC setting can be generated automatically or manually overridden.

Automatic Gain Control

The CXD1968AR contains an internal AGC block, which monitors the signal level at the output of the ADC and provides a Pulse Width Modulated (PWM) control signal to implement an automatic gain control loop. The AGC is capable of tracking out 60Hz AM interference with the specified time constant, and large changes in input level. A 40dB input swing can be corrected in 20ms (irrespective of QAM/ QPSK modulation scheme).

The IF AGC automatic mode is enabled by resetting the AGC Set bit in the AGC_CTL register. The sense of the output is controlled by the AGC Neg bit in the same register.

Manual Gain Control

The AGC loop can be set manually using the AGC Set bit in the AGC_CTL register and entering a value of 0 to 1023 in the AGC Manual field in this register.

RF AGC GPO

The RF AGC pin may be configured to generate a fixed logic “0” or “1” output level (3.3V) where the RF AGC variable output function is not required. A typical application is to switch a dual bandwidth SAW filter or other circuit function in software.

If the RF AGC output pin is to be used for this kind of application, the integrating RC filter is not required. This example generates a logic “1” or 3.3V level at this output.

Example: 0xD8 0xB2 0x07 ; set RF AGC output pin High

RF AGC GPI

The RF AGC pin may be configured as a logic input (3.3V logic but 5V tolerant) where the RF AGC variable output function is not required. This may be used to sense operation of an external circuit.

◆ Monitoring

Status Monitoring

Transport Stream Lock

This flag indicates that a valid MPEG2 transport stream is available at the CXD1968AR TSDATA outputs. Transport stream lock can be determined from reading the FEC_STATUS register, or from the INTERRUPT_SOURCE register. This bit is set in both registers whenever the Reed-Solomon FEC block has locked and a valid MPEG2 transport stream is now ready for output. Should the transport stream lose lock, then a TS lost lock flag bit is set in the FEC_PARAMS and INTERRUPT_SOURCE registers.

FEC Lock

FEC lock indicates that the Reed-Solomon FEC block has a coded MPEG2 transport stream at its input, which it is trying to decode. FEC lock can be determined from reading the FEC_STATUS register.

AGC Lock

The AGC lock flag in the COR_STAT register can be used to check that the input signal level is not varying and is not too high or too low (a high-level signal will cause distortion problems, and a low-level signal will suffer from quantization noise).

Core State Machine

The COFDM demodulator contains a state machine, which can be used to gain information as to why the CXD1968AR has not locked on to an incoming OFDM signal. The core has the following states:

0000	State machine not forced
0001	WAIT_TRL
0010	WAIT_AGC
0011	WAIT_SYR
0100	WAIT_PPM
0101	WAIT_TPS
0110	MONITOR _TPS

State 0: IDLE	Core is disabled.
State 1: WAIT_ TRL	Core is calculating a value to be used later.
State 2: WAIT_AGC	Core is waiting for input signal levels to stabilize to an acceptable value before attempting to demodulate the incoming signal.
State 3: WAIT_SYR	AGC has locked, waiting for the core to determine the guard interval and its position.
State 4: WAIT_PPM	Waiting for the pilot processing module to find the pilot carriers.
State 5: WAIT_TPS	Waiting for the core's TPS decoder to acquire frame sync (which determines the symbol number).
State 6: MONITOR_TPS	Signal ready to be fed to the Viterbi decoder, continue to monitor the TPS data for parameter changes.

Pre-Viterbi BER

Pre-Viterbi BER readings are available from the VIT_BER register. The sampling period is adjustable in the VIT_CTRL register.

Reed-Solomon BER

Pre- or Post-Reed-Solomon BER can be either measured or estimated using the BER_ESTIMATE register. In measurement mode, NULL packets must be used. In estimate mode, any data can be used. Estimation mode assumes that all post Viterbi errors are corrected by the Reed-Solomon decoder. Measurement mode is selected by setting the Measurement_Sel bit in the FEC_PARAMS register. Readings should be taken whenever the NEW_BER bit is set. If too many errors have been recorded during the specified measurement period, then the BERCNT_Overflow bit will be set. Should this occur, the reading should be discarded and a lower measurement period selected. The measurement period is set using the BER_PERIOD register.

Uncorrected Errors

Errored Second

This indicates that the Reed-Solomon FEC block could not correct all the errors found in one or more 204-byte packets received during the last second. This is because >8 errors were found in the packet. Errored second can be determined from reading the FEC_STATUS register, or from the INTERRUPT_SOURCE register.

Severely Errored Second

This indicates that the Reed-Solomon FEC block has been unable to correct the errors found in N or more 204-byte packets received during the last second. This is because >8 errors were found in each of the packets.

N is set using the LT_QLTY_THRESHOLD register. Typically, this can be used to set a threshold value with regard to picture degradation, depending on the quality of service required. Severely errored second can be determined from reading the FEC_STATUS register, or from the INTERRUPT_SOURCE register.

Codeword Reject Count

This indicates the number of rejected codewords (MPEG-2 packets) in one second. This is recognized to be a particularly useful measurement as it is more closely aligned to receiver picture failure than BER.

Signal-to-Noise Estimate

The CHC_SNR register can be used to obtain an estimate of the signal-to-noise ratio of the received signal either for each carrier individually or as a mean across the channel.

If the mean bit in the SNR_CARRIER_2 register is set, then a mean value across the channel can be read from the CHC_SNR register.

If the mean bit in the SNR_CARRIER_2 register is reset then the carrier number can be selected by programming the SNR carrier number bits in the SNR_CARRIER_1, 2 registers and after at most one symbol the SNR for that carrier can be read from the CHC_SNR register (the host controller must wait for one symbol to be sure that the data is ready).

A higher value indicates a lower operating SNR. The estimated value is independent of the channel response, and accurate to about ±1dB. The value in this register (N) can be converted to an approximate dB value using the following empirical formula:

$$\mathrm{SNR[dB]} = \frac{\mathrm{CHC\_SNR}}{8}$$

Interrupts

These can be used to quickly ascertain the status of the chip. This can be done in one of two ways:

1. Regularly polling the interrupt flags over the I²C bus.
2. Using the INT pin to raise a hardware interrupt, then getting the host controller to read the interrupt flags to determine the type of interrupt.

The interrupts are of two basic types:

1. High-level interrupts: the flags for these are contained in the interrupt status register (INTERRUPT_SOURCE).
2. OFDM core interrupts: the flags for these are contained in the core interrupt status register (COR_INTSTAT).

High-level Interrupts

These interrupts relate to the key stages in acquiring transport stream lock. Interrupt flags are available for the following events:

0. COFDM demodulator interrupt (poll the COR_INTSTAT register to find out why)
1. Transport stream lock
2. Transport stream lost lock
3. Reserved
4. Errored second detected
5. Severely errored second detected
6. Codeword rejected (>8 errors in current packet)
7. Transport stream smoothing under/over flow

To clear each interrupt, write a “1” to the corresponding bit in the INTERRUPT_SOURCE register after the interrupt has occurred.

COFDM Demodulator Interrupts

COFDM demodulator interrupt flags are available for the following events:

0. AGC lock change (AGC gained lock/AGC lost lock)
1. End of symbol (from Symbol Recovery block)
2. FFT done: FFT processing complete on current symbol
3. Receipt of a TPS block
4. Change of TPS parameters
5. TPS block has a bad BCH checksum.

Enabling Core Interrupts

Interrupts are enabled using the COR_INTEN register. To enable any core interrupt, the INTEN Global bit in the COR_INTEN register must be set. Each individual interrupt is then enabled by setting the appropriate bit in the COR_INTEN register.

Low-power Standby Mode

This mode reduces the nominal power consumption of the CXD1968AR in IF mode from 140mW to 10mW.

To obtain maximum benefit it is necessary in software to;

◆ Disable PLL and stop internal clocks
◆ Power-down the ADC

Recovery from low-power standby mode can be achieved by cold reset to all blocks.

Example: 0xD8 0xA9 0x41 ; power-down PLL and stop clock
0xD8 0xB9 0x01 ; power-down ADC

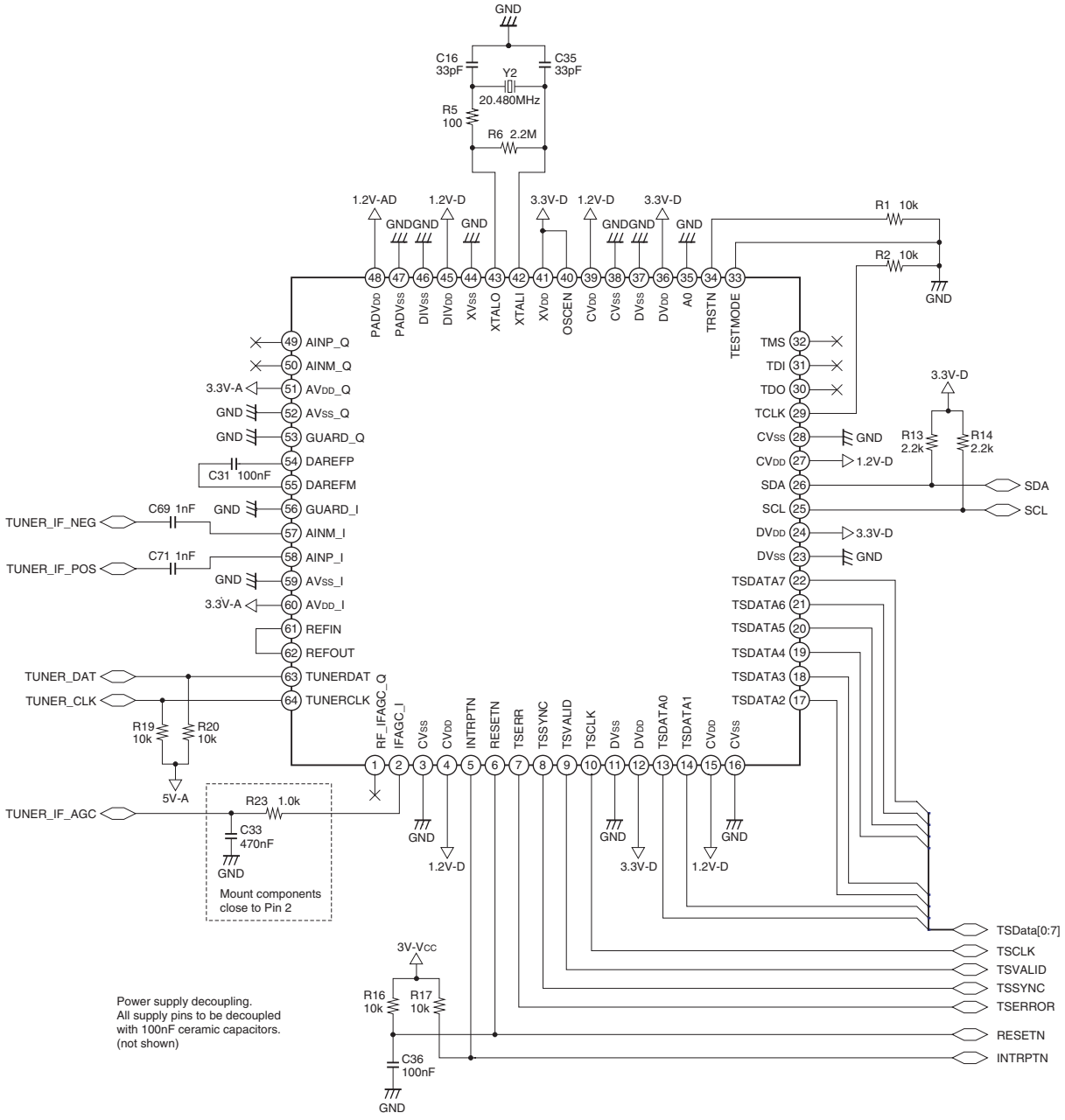
Ultra Low-power Shutdown Mode

This mode reduces the nominal power consumption of the CXD1968AR in IF mode from 140mW to < 1mW.

This mode is entered through external control of OSCEN (Pin 40). Grounding this pin will stop the crystal oscillator and all on-chip activity.

The CXD1968AR should be reset when resuming from shutdown mode.

4. Application Circuit



Note) **For High IF or Low IF mode, use PIN 57, 58 (AINM_I, AINP_I) as the ADC input.**
And, PIN 49, 50, which are unused, should be kept open.

Fig. 5. Application and Test Measurement Schematic for IF Mode of Operation

5. Design Guidelines

This section describes the application of the CXD1968AR DVB-T COFDM demodulator IC.

The schematic contained within the previous section should be used to assist with following descriptions.

Refer to the separate engineering application notes for additional information about specific configurations and uses. EAN-0065 is intended to assist users familiar with the CXD1976R in making the transition to the CXD1968AR.

Circuit Configurations

The CXD1968AR has the capability to operate with High IF, Low IF and Zero IF conventional or silicon tuners. The application described in this section is for a conventional High IF tuner.

ADC Input

The ADC input of the CXD1968AR is directly compatible with differential sources. Where the tuner can supply only a single-ended IF signal, a balun is recommended to maximize the dynamic range of the IF strip.

The ADC input has a high impedance input (> 1kΩ). The tuner output impedance is normally low (< 100Ω) and it is not necessary to match to the ADC. The differential inputs are self-biasing and our recommendation is to AC couple the input signals with 1nF or larger capacitors.

Note) For High IF or Low IF mode, use PIN 57, 58 (AINM_I, AINP_I) as the ADC input.

ADC Reference Components

The ADC reference voltage at Pins 61 and 62 (connected together) should be decoupled with 100nF multilayer capacitor for optimum performance.

AGC

The CXD1968AR generates an IF AGC output. This signal is a digital PWM format requiring an integrating RC filter to provide a variable DC control voltage for the tuner or IF circuit.

A second AGC output can be generated for RF gain control. The output signal is also PWM format, but may be configured as a fixed logic level output for general-purpose control functions. When used as an AGC output, an integrating RC filter is required. This pin may alternatively be used as a logic input at a nominal 3.3V but is 5V compliant.

The application values for the PWM integrating filter of 1000Ω and 470nF are chosen to give a 0.5ms time constant which approximates to a 400Hz cutoff frequency. For the IF AGC loop, this value is chosen as a compromise between suppressing the PWM high-frequency components and permitting the AGC loop to track 50/60Hz AM interference which may be present on the received signal. Typically the AGC response time to a step input, as might occur changing channel, is 20ms. If the filter values are modified perhaps to achieve faster channel acquisition, then note the possible impact on AM rejection.

Clock and Crystal Oscillator

The oscillator cell will operate with an external crystal or use an external clock, this is configured at start-up by register settings described in the application note EAN-0066. If using an external clock, this must be present before programming can be applied.

Performance with an external clock may be compromised if the quality of the reference signal is poor.

JTAG

The JTAG facility can be utilized, but refer to section 2 of this datasheet for information on how to configure the connections.

It may be necessary to apply pull-down resistors to these pins:

TCK	Pin 29
TRSTN	Pin 34

Power Supply Sequencing

During the power-up sequence of the 1.2V and 3.3V supplies, it is important to ensure that the 1.2V supply is not applied before the 3.3V supply. Failure to do this could result in latch up and the CXD1968AR will not function correctly.

During power-down the 3.3V supply should not fall below the 1.2V supply, as both decay.

Both conditions can be met by deriving the 1.2V supply from the 3.3V supply.

If this configuration is not utilized or the timing cannot be guaranteed, it is possible to prevent supply latch-up by adding a Schottcky diode between the supplies. Connect the diode with anode to 1.2V supply and cathode to 3.3V supply. This is only appropriate when both analog and digital 3.3V supplies are derived from the same regulator. The diode used must be a Schottcky type for low forward voltage drop, ie. 0.4V or less. This solution is applicable to both power-up and power-down conditions.

Reset

Note the hardware reset requirements outlined in section 3. As has been stated, when the CXD1968AR is powered up, it must be hard reset. This can be achieved simply by using an external RC circuit with time constant of around 1ms, values of 10kΩ and 100nF are employed in the recommended application. Alternatively this function may be provided by a specific device or host controller and the timing will be dependant upon supply rise time.

Pull-ups

The following pins should be used with pull-up resistors:

SDA	Pin 26
SCL	Pin 25
QSDA	Pin 63
QSCLK	Pin 64
INTRPTN	Pin 5 (if used)

A nominal value of 10kΩ is used with the CXD1968AR but other values are permissible dependant upon the interface requirement. The maximum loading is stated in the DC Electrical Characteristics, a value of less than 1000Ω is not advisable.

Printed Board Layout

Board layout recommendation for CXD1968AR.

Supply and Ground

The CXD1968AR uses three supplies:

1.2V digital	for core processing
3.3V digital	for clock and I/O
3.3V analog	for ADC

All supplies should be decoupled close to the supply pins.

A single ground plane is recommended. However in some situations a split analog/digital ground plane can offer improved immunity from digital noise. Which option yields better performance will depend upon the application, ie. location of supplies and interference sources.

These rules should be adhered to, minimizing the risk of performance degradation:

- The supplies may be tracked-in (2-layer board) or assigned to a specific power-plane (multilayer). With either form it is essential to provide a low-impedance ground return to the source of the supply. A continuous ground plane is preferred as a starting point.
- The quiet analog section resides at one corner of the device, Pins 47 to 62. The supply to this section should feed into and return (via ground) without crossing over the digital section of board.
- The digital section should avoid a ground return path through the analog section. Failure to ensure this may compromise performance of the demodulator.

If it is not possible to ensure uninterrupted ground return paths back to each supply source, it may be necessary to partition the ground plane to force digital supply ground return currents to avoid the analog section. It is also advisable to link analog and digital grounds in the area directly below the CXD1968AR.

ESD

Other constraints include immunity from ESD. The instantaneous energy presented by any electrical impulse should avoid passing close to or through the CXD1968AR. Similarly any connection to the CXD1968AR should not be susceptible to or protected against ESD pickup. For circuit connections that may travel outside of the immediate vicinity around the CXD1968AR, it is recommended that low-value series resistors are employed to limit charge transfer. A typical value would be 47 to 100Ω.

ADC Input

The signal connections to the ADC input should be of similar length and routed together. Failure to do so may compromise the common mode rejection properties of the differential input circuit. Low-impedance drive to the ADC will minimize the risk of spurious pickup.

The connection between tuner IF output and the CXD1968AR ADC input should be routed over continuous analog ground plane.

ADC Reference Components

As for the ADC input connection, the capacitor between DAREFP and DAREFM should be positioned above continuous analog ground plane.

AGC

The AGC PWM integrating RC filter (either IF or RF when used) should be positioned as close to the CXD1968AR as practical, ideally within 5mm. The pinout of the CXD1968AR has been improved to assist this constraint. It will prevent harmonics of the PWM signal breaking through into the IF circuit. The PWM edges are slew-rate limited but good practice will ensure no interference with the IF input.

Crystal Oscillator

When used with an external clock signal, a level of 1Vp-p is recommended. This should be AC coupled, 1nF minimum. The oscillator cell will operate as a buffer but requires the 2.2MΩ feedback resistor, as present for the crystal, to provide a DC path for the self-biasing action.

Transport Stream

The transport stream data rate is relatively low for smoothed parallel mode of operation, but is clocked at 40MHz in serial mode. In this mode the logic edges could create significant reflection in unterminated long printed-board tracks. It is recommended that source resistors are used at the CXD1968AR prior to launching along tracks of 50mm or more. A suitable source resistor value of 39 to 47Ω should be considered.

6. Electrical Characteristics

Absolute Maximum Ratings

(Ta = 25℃, AVSS = 0V, DVSS = 0V, CVSS = 0V)

Item	Symbol	Condition	Min.	Max.	Unit
Digital power supply (I/O)	DVDD		–0.5	+4.6	V
Analog power supply (ADC)	AVDD		–0.5	+4.6	V
Digital power supply (Core)	CVDD		–0.5	+1.68	V
Input voltage	Vin		–0.5	+4.6	V
Output voltage	Vout		–0.5	+4.6	V
Analog voltage	Vina	DAREFN, DAREFP, REFIN, VCM, REXT_I, REXT_Q, AINM_I, AINP_I, AINM_Q, AINP_Q	–0.5	+4.6	V
Operating temperature	Topr		–40	+125	℃
Storage temperature	Tstg		–65	+150	℃

Note) 1. The device must be operated within the limits of the absolute maximum ratings. If the device is operated outside these conditions, the device may be permanently damaged.

2. Functional operation at or outside any of the conditions indicated in the absolute maximum ratings is not implied.

3. Exposure of the device to the absolute maximum rating condition for extended periods can affect system reliability.

4. 5V tolerant inputs are only 5V tolerant while the device power is applied. If no device power is applied there in no protection to 5V levels and the device may be permanently damaged. It is important to observe the conditions for 5V protection when sequencing power supplies in the application.

5. Refer to section 5, Design Guidelines, regarding power-up/down sequencing. The core (1.2V) should not be powered-up when the I/O (3.3V) is powered-down.

Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital power supply (I/O)	DVDD	DVSS = 0	3.0	3.3	3.6	V
Analog power supply	AVDD	AVSS = 0	3.0	3.3	3.6	V
Digital power supply (Core)	CVDD	CVSS = 0	1.08	1.2	1.32	V
DC input voltage	VIH		2		5.5	V
DC input voltage	VIL		–0.3		0.8	V
High-level and Low-level output current	IOH, IOL	Pins RF_AGC_Q, IFAGC_I, TUNERDAT, TUNERCLK, TSVALID, TSERR, TSDATA[7:0], TSSYNC			8.0	mA
		Pins TDO, INTRPTN, TSCLK, SCL, SDA			12	mA
Operating frequency (Internal Xtal oscillator)	Fop			20.48		MHz
Operating frequency (External 4-20MHz reference)	Fop			20.50		MHz
Ambient temperature	Ta		0		+70	℃

DC Electrical Characteristics

(0℃ < Ta < 70℃, AVSS = 0V, DVSS = 0V, CVSS = 0V, 3.0V ≤ AVDD ≤ 3.6V, 3.0V ≤ DVDD ≤ 3.6V, 1.08V ≤ CVDD ≤ 1.32V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Low voltage	V_{IL}		–0.3		0.8	V
Input High voltage	V_{IH}		2		5.5	V
Input Low current	I_{IL}		–10			μA
Input pull-up resistor	R_{PU}		39	55	85	kΩ
Input High current	I_{IH}				10	μA
Input pull-down resistor	R_{PD}		45	93	198	kΩ
Output voltage Low	V_{OL}	I_{OL} = 8mA, Pins RF_AGC_Q, IFAGC_I, TUNERDAT, TUNERCLK, TSVALID, TSERR, TSDATA[7:0], TSSYNC I_{OL} = 12mA, Pins TDO, INTRPTN, TSCLK, SCL, SDA			0.4	V
Output voltage High	V_{OH}	I_{OL} = 8mA, Pins RF_AGC_Q, IFAGC_I, TUNERDAT, TUNERCLK, TSVALID, TSERR, TSDATA[7:0], TSSYNC I_{OL} = 12mA, Pins TDO, INTRPTN, TSCLK, SCL, SDA	2.4			V
Supply current (IF mode)	$I_{DD3.3}$	Current with TS outputs enabled		24		mA
	$I_{DD1.2}$			50		mA
Supply current (ZIF mode)	$I_{DD3.3}$	Current with TS outputs enabled		40		mA
	$I_{DD1.2}$			50		mA
ADC input dynamic range	V_{AIN}	Differential signal	0.7, 1.0, 1.5, 2.0			Vp-p
Common mode output	V_{CM}				1.25	V

Note) Electrical characteristics measured with 50pF load.

AC Electrical Characteristics

Transport Stream Interface

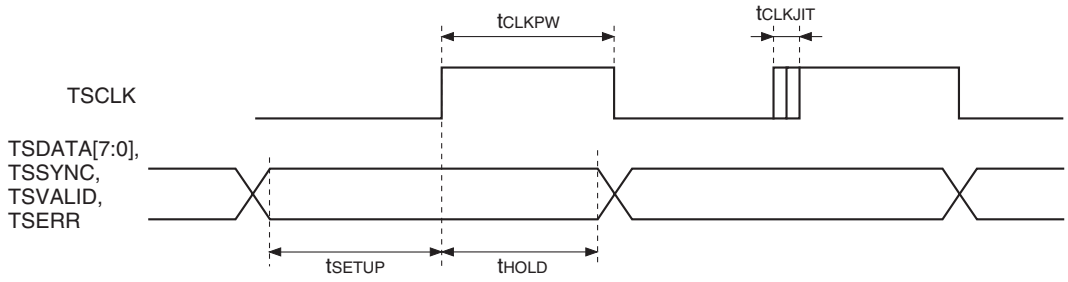


Fig. 6. Transport Stream Timing Diagram

Conditions
Temperature: 0℃ < Ta < 70℃
Voltage: 3.15V ≤ AV_{DD} ≤ 3.45V, 3.15V ≤ DV_{DD} ≤ 3.45V, 1.08V ≤ CV_{DD} ≤ 1.32V

Parallel Mode – Smoothing Off

Item	Symbol	Min.	Typ.	Max.	Unit
Transport stream setup time	t_{SETUP}	39		45	ns
Transport stream hold time	t_{HOLD}	45		49	ns
TSCLK frequency			10.25		MHz
TSCLK width	t_{CLKPW}		48		ns
TSCLK jitter	t_{CLKJIT}			1	ns

Parallel Mode – Smoothing On

Item	Symbol	Min.	Typ.	Max.	Unit
Transport stream setup time	t_{SETUP}	120		728	ns
Transport stream hold time	t_{HOLD}	125		708	ns
TSCLK frequency		0.68		3.7	MHz
TSCLK width	t_{CLKPW}		44		ns
TSCLK jitter	t_{CLKJIT}			24.8	ns

Serial Mode – Smoothing Off

Item	Symbol	Min.	Typ.	Max.	Unit
Transport stream setup time	t_{SETUP}	3		4.6	ns
Transport stream hold time	t_{HOLD}	3.8		5	ns
TSCLK frequency			81.96		MHz
TSCLK width	t_{CLKPW}		5.5		ns
TSCLK jitter	t_{CLKJIT}			1	ns

Serial Mode – Smoothing On

Item	Symbol	Min.	Typ.	Max.	Unit
Transport stream setup time	t_{SETUP}	9		12	ns
Transport stream hold time	t_{HOLD}	12		15	ns
TSCLK frequency			41.67		MHz
TSCLK width	t_{CLKPW}		12		ns
TSCLK jitter	t_{CLKJIT}			1	ns

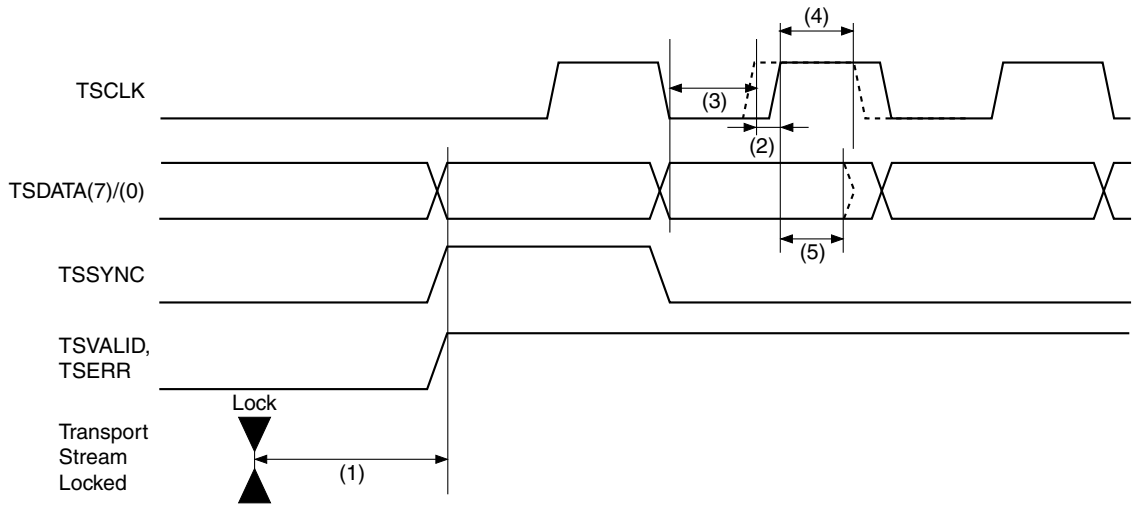
Note) Dependent upon code-rate and modulation.

Transport Stream Interface (Serial Mode)

(0℃ < Ta < 70℃, AV_{SS} = 0V, DV_{SS} = 0V, CV_{SS} = 0V, 3.15V ≤ AV_{DD} ≤ 3.45V, 3.15V ≤ DV_{DD} ≤ 3.45V, 1.08V ≤ CV_{DD} ≤ 1.32V)

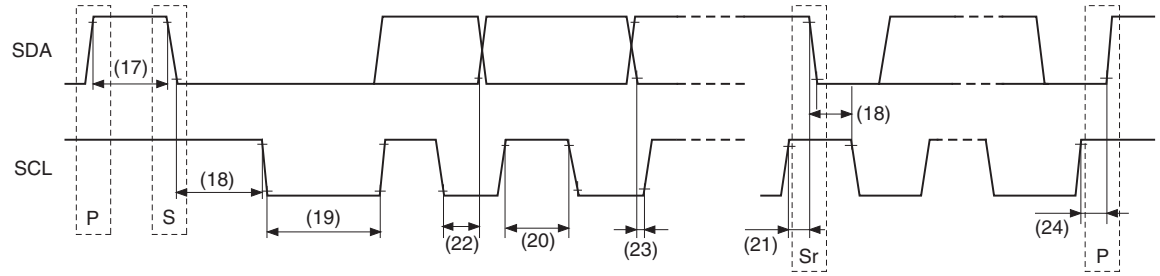
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
t_{TSLOCK}, Transport stream locked to valid TSSYNC, TSVALID and TSERR	(1)		146			ns
$t_{TSJIT(E)}$, Transport stream clock jitter (smoothing enabled)	(2)				1	ns
t_{TSSU}, Transport stream TSDATA, TSSYNC, TSVALID and TSERR setup time to TSCLK active edge	(3)		6			ns
$t_{TSPW(E)}$, Transport stream TSCLK pulse width (smoothing enabled)	(4)			12.2		ns
$f_{TSCLK(E)}$, Transport stream TSCLK frequency (smoothing enabled)				41		MHz
t_{TSHD}, Transport stream TSDATA, TSSYNC, TSVALID and TSERR hold time from TSCLK active edge	(5)		3			ns

Note) The items in the above table are applicable only if transport stream smoothing is enabled. Use of the serial transport stream output interface with transport stream smoothing disabled is not recommended.



Tranport Stream Interface (Serial Mode)

I²C Interface



(0℃ < Ta < 70℃, AV_{SS} = 0V, DV_{SS} = 0V, CV_{SS} = 0V, 3.15V ≤ AV_{DD} ≤ 3.45V, 3.15V ≤ DV_{DD} ≤ 3.45V, 3.15V ≤ CV_{DD} ≤ 3.45V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
f_{SCL}, SCL clock frequency	(16)		0		400	kHz
t_{SDABUF}, Bus free time between a STOP(P) and START(S) condition	(17)		1.3			µs
t_{STAHD}, Hold time (repeated) START condition. After this period, the first clock pulse is generated.	(18)		0.6			µs
t_{SCLLOW}, Low period of SCL clock	(19)		1.3			µs
$t_{SCLHIGH}$, High period of SCL clock	(20)		0.6			µs
t_{STASU}, Setup time for a repeated START condition	(21)		0.6			µs
t_{SDAHD}, SDA data hold time	(22)		0		0.9	µs
t_{SDASU}, SDA data setup time	(23)		100			ns
t_{STOSU}, Setup time for STOP condition	(24)		0.6			µs

7. Package Pin Layout

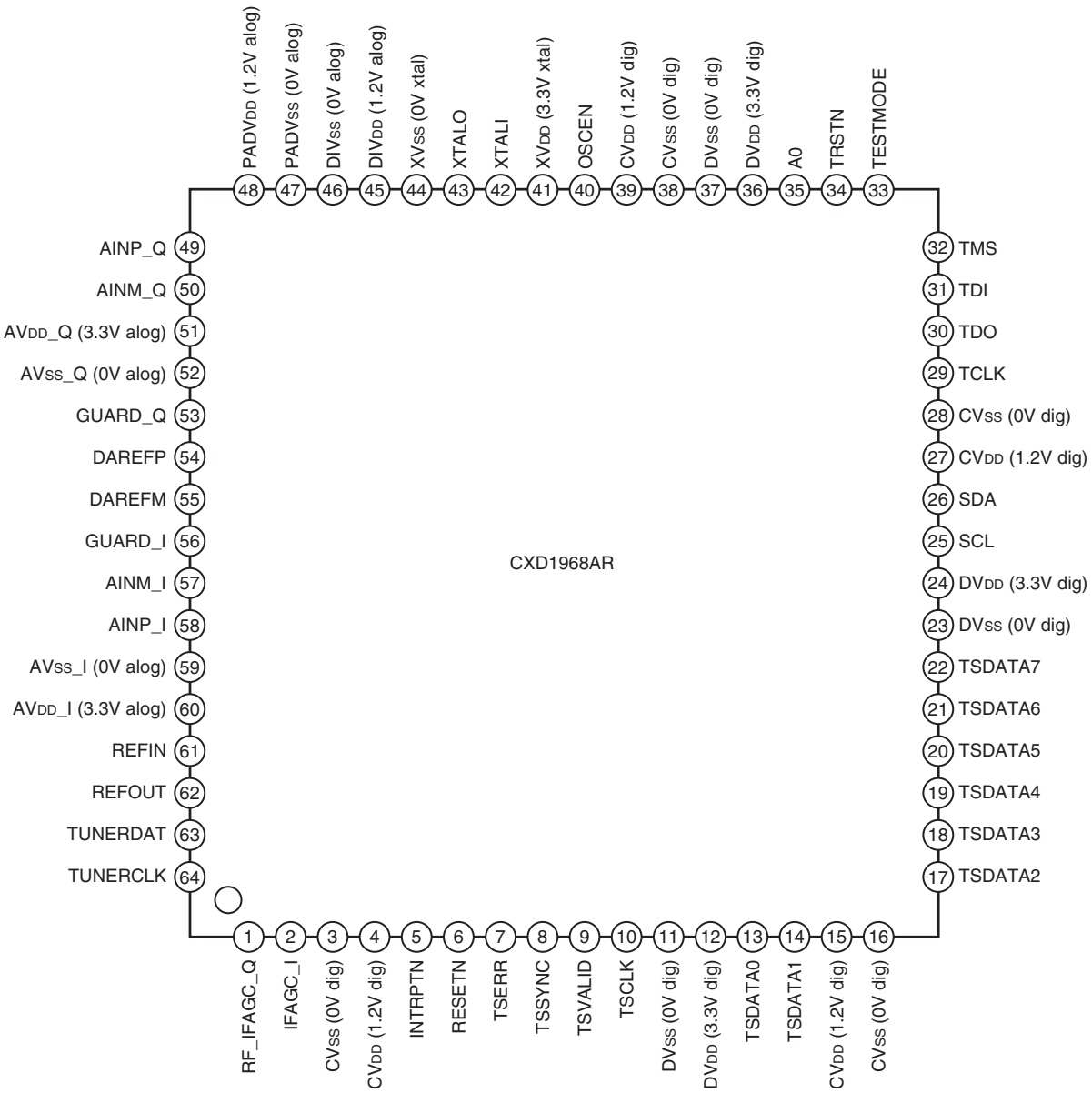


Fig. 7. CXD1968AR Pinout

8. Pin Description

Pin No.	Symbol	Type	Drive	Function
Clock and Reset				
43	XTALO	Output	N/A	Crystal oscillator cell output.
42	XTALI	Input	N/A	Crystal oscillator cell input and input for 4-20MHz tuner clock reference.
40	OSCEN	Input	N/A	Crystal oscillator cell enable.
6	RESETN	Input 5V tolerant Schmitt trigger	N/A	Active low hardware reset.
Dual ADC Interface				
55	DAREFM	Analog output	N/A	Output pin to external 0.1μF bypass capacitor for the ADC internal DAC lower reference voltage.
54	DAREFP	Analog output	N/A	Output pin to external 0.1μF bypass capacitor for the ADC internal DAC upper reference voltage.
61	REFIN	Analog input	N/A	Reference voltage input for the I channel ADC, normally left unconnected.
62	REFOUT	Analog input/ output	N/A	Ground reference input for REFIN (Pin 52), normally left unconnected.
57	AINM_I	Analog input	N/A	Differential analog input (I channel ADC).
58	AINP_I	Analog input	N/A	Differential analog input (I channel ADC).
56	GUARD_I	Analog input	N/A	Guard ring input for I channel ADC, this should be connected to analog AVSS_I via a low impedance trace.
53	GUARD_Q	Analog input	N/A	Guard ring input for Q channel ADC, this should be connected to analog AVSS_Q via a low impedance trace.
50	AINM_Q	Analog input	N/A	Differential analog input (Q channel ADC).
49	AINP_Q	Analog input	N/A	Differential analog input (Q channel ADC).
MPEG2 Transport Stream Interface				
22 21 20 19 18 17 14 13	TSDATA7 TSDATA6 TSDATA5 TSDATA4 TSDATA3 TSDATA2 TSDATA1 TSDATA0	Tri-state output 5V tolerant slew rate limited[7:1] with pull-up	8mA	MPEG2 transport stream parallel data output. If serial mode is selected data output is either TSDATA0 (Pin 13) or TSDATA7 (Pin 22). Tri-state following hardware reset.
9	TSVALID	Tri-state output 5V tolerant slew rate limited output with pull-up	8mA	Identifies data portion of transport stream packet (excludes parity bytes). The polarity and timing of this valid signal are programmable. Tri-state following hardware reset.
10	TSCLK	Tri-state output 5V tolerant	12mA	MPEG2 transport stream byte clock. If serial MPEG2 transport stream is selected this output becomes the bit clock. The polarity of this clock is programmable. Tri-state following hardware reset.

Pin No.	Symbol	Type	Drive	Function
8	TSSYNC	Tri-state output 5V tolerant slew rate limited output with pull-up	8mA	Indicates MPEG2 47h sync byte in transport stream packet. The polarity of this sync signal is programmable. Tri-state following hardware reset.
7	TSERR	Tri-state output 5V tolerant slew rate limited output with pull-up	8mA	MPEG2 transport stream error flag. Indicates uncorrectable errors in current packet. The polarity and timing of this error signal is programmable. Tri-state following hardware reset.
Host Control Interface				
26	SDA	Bi-directional 5V tolerant slew rate limited open-drain output	12mA	I^2C data. Must be pulled up by external resistor to 3.3V or 5V. Suggested value 10k.
25	SCL	Bi-directional 5V tolerant slew rate limited open-drain output	12mA	I^2C clock. Must be pulled up by external resistor to 3.3V or 5V. Suggested value 10k.
35	A0	Input 5V tolerant	N/A	I^2C address (variable part). Bit 0 of I^2C device address. Connect to either DV_{DD} or DV_{SS}.
5	INTRPTN	Output 5V tolerant open-drain slew rate limited output	12mA	Programmable interrupt pin. Must be pulled up by external resistor to 3.3V or 5V. Suggested value 10k.
Tuner Interface (Control and AGC)				
2	IFAGC_I	Output Slew rate limited	8mA	IF AGC pulse width modulated (PWM) output for I channel ADC.
1	RF_IFAGC_Q	Bi-directional 5V tolerant slew rate limited output with pull-up	8mA	Mode 1: RF AGC pulse width modulated (PWM) output (IF mode only) Mode 2: IF AGC pulse width modulated (PWM) output for Q channel ADC (ZIF mode) Mode 3: PLL locked status input, and general-purpose input (IF mode only) Mode 4: General-purpose digital output (IF mode only)
64	TUNERCLK	Bi-directional 5V tolerant open-drain output	8mA	Quiet I^2C clock. Must be pulled up by external pull-up resistor to 3.3V or 5V if used. Suggested value 10k.
63	TUNERDAT	Bi-directional 5V tolerant open-drain output	8mA	Quiet I^2C data. Must be pulled up by external pull-up resistor to 3.3V or 5V if used. Suggested value 10k.
Testability and Evaluation Interface				
33	TESTMODE	Input 5V tolerant with pull-down	N/A	*Normal Mode*: Connect to DV_{SS}. *JTAG Test Mode*: Set high to enable scan test or SRAM BIST modes.
34	TRSTN	Input 5V tolerant with pull-up	N/A	*Normal Mode*: Connect to DV_{SS}. JTAG Test Mode: JTAG test reset input
30	TDO	Tri-state output 5V tolerant	12mA	*Normal Mode*: Leave unconnected. *JTAG Test Mode*: JTAG test data output

Pin No.	Symbol	Type	Drive	Function
31	TDI	Input 5V tolerant with pull-up	N/A	*Normal Mode*: Leave unconnected. *JTAG Test Mode*: JTAG test data input
32	TMS	Input 5V tolerant with pull-up	N/A	*Normal Mode*: Leave unconnected. *JTAG Test Mode*: JTAG test mode select
29	TCK	Input 5V tolerant	N/A	*Normal Mode*: Connect to DVSS. *JTAG Test Mode*: JTAG test clock.
Power Supplies				
23, 11, 37	DVSS	Digital I/O power supply		Supplies digital I/O cell power. Connect to DVSS (0V).
36, 24, 12	DVDD	Digital I/O power supply		Supplies digital I/O cell power. Connect to DVDD (3.3V ± 10%).
28, 16, 3, 38	CVSS	Digital core logic power supply		Supplies internal digital logic and SRAM power. Connect to DVSS (0V).
39, 27, 15, 4	CVDD	Digital core logic power supply		Supplies internal digital logic and SRAM power. Connect to DVDD (1.2V ± 10%).
46	DIVSS	Digital power supply		Supplies ADC “clock divider” function only. Connect to clean supply DVSS (0V) for best ADC operation.
45	DIVDD	Digital power supply		Supplies ADC “clock divider” function only. Connect to clean supply DVDD (1.2V ± 10%) for best ADC operation.
47	PADVSS	PLL analog and digital supply		Supplies analog functions within PLL. No connection to other digital supplies within IC. For best performance connect to clean separate supply. Connect to DVSS (0V).
48	PADVDD	PLL analog and digital supply		Supplies analog functions within PLL. No connection to other digital supplies within IC. For best performance connect to clean separate supply. Connect to DVDD (1.2V ± 10%).
59	AVSS_I	Analog power supply		Supplies ADC (I channel) functions and analog I/O power. Connect to clean AVSS (0V).
60	AVDD_I	Analog power supply		Supplies ADC (I channel) functions and analog I/O power. Connect to clean AVDD (3.3V ± 10%).
52	AVSS_Q	Analog power supply		Supplies ADC (Q channel) functions and analog I/O power. Connect to clean AVSS (0V).
51	AVDD_Q	Analog power supply		Supplies ADC (Q channel) functions and analog I/O power. Connect to clean AVDD (3.3V ± 10%).
44	XVSS	Analog power supply		Supplies crystal only. Connect to clean AVSS (0V).
41	XVDD	Analog power supply		Supplies crystal only. Connect to clean AVDD (3.3V ± 10%).

9. Control Register Definitions

Register Map

Name	Addr.	R/W	7	6	5	4	3	2	1	0
CXD1968AR COFDM Core Registers										
COR_CTL	00	R/W	Reserved		Core Active	Hold	Core State[3:0]			
COR_STAT	01	R	CHC Tracking	TPS Locked	SYR Locked	AGC Locked	Core State[3:0]			
COR_INTEN	02	R/W	INTEN Global	Reserved	INTEN SYR SymEnd	INTEN FFT Done	INTEN AGC Lock Change	INTEN TPS RCVD BCHBad	INTEN TPS RCVD Changed	INTEN TPS RCVD Update
COR_INTSTAT	03	R/W	Reserved		INTSTAT SYR SymEnd	INTSTAT FFT Done	INTSTAT AGC Lock Change	INTSTAT TPS BadBCH	INTSTAT TPS RCVD Changed	INTSTAT TPS RCVD Update
COR_MODEGUARD	04	R/W	ZIF Enable	Reserved			Force	Mode	Guard	
AGC_CTL	05	R/W	Delay Startup[7:5]			AGC Use Last Value	AGC BW Reduction[1:0]		AGC Neg	AGC Set
AGC_MANUAL	06	R/W	AGC Manual[7:0]							
	07	R/W	Reserved				AGC Manual[11:8]			
AGC_TARGET	08	R/W	AGC Target[7:0]							
AGC_GAIN	09	R/W	AGC Gain I[7:0]							
	0A	R/W	AGC After DCC	Lock Q	Lock I	AGC Locked	AGC Gain I[11:8]			
ITB_CTL	0B	R/W	Reserved							ITB Invert Spectrum
ITB_FREQ	0C	R/W	ITB Frequency[7:0]							
	0D	R/W	Reserved		ITB Frequency[13:8]					
CAS_CTL	0E	R/W	CCS Enable	ACS Disable	DAGC Disable	DAGC BW Reduction[1:0]	CCSMU[2:0]			
CAS_FREQ	0F	R/W	CCS Freq[7:0]							
CAS_DAGCGAIN	10	R	CAS DAG Gain[7:0]							
TEST9	11	R/W	TEST9[7]	TEST9[6:3]				TEST9[2]	TEST9[1]	TEST9[0]
SYR_STAT	12	R	Reserved		TEST5	SYR Locked	Reserved	SYR Mode	SYR Guard[1:0]	
FFT_CTL	17	R/W	Reserved					FFT Test Trigger	FFT Manual Mode	FFT Inverse Transform
SCR_CTL	18	R/W	Reserved	SYR Adjust Decay[2:0]			Reserved		SCR No Common Phase	SCR Disable
PPM_CTL	19	R/W	Reserved	PPMMaxFreq[2:0]			Reserved	PPM Reduced Search Time Enable	PPM Disable Find Scattered Pilots	PPM Bypass Corr
TRL_CTL	1A	R/W	Reserved	TRL Track Gain Factor[3:0]				TRL Loop Gain[2:0]		
TRL_NOMINALRATE_1	1B	R/W	TRL Nominal Rate[15:8]							
TRL_NOMINALRATE_2	1C	R/W	TRL Nominal Rate[23:16]							
TRL_TIME	1D	R	TRL Timing Offset[7:0]							
	1E	R	TRL Timing Offset[15:8]							
CRL_CTL	1F	R/W	CRL Disable Fine	CRL Track Gain Factor[3:0]				CRL Loop Gain[2:0]		
CRL_FREQ	20	R	CRL Frequency Offset[7:0]							
	21	R	CRL Frequency Offset[15:8]							
	22	R	Sign Ext	CRL Frequency Offset[22:16]						

Name	Addr.	R/W	7	6	5	4	3	2	1	0
CHC_CTL	23	R/W	Mean Pilot Gain[2:0]			Manual Mean Pilot	Disable Bad Pilots	Disable Noise Normal	Disable CHC Predictor	CHC Interpolator
CHC_SNR	24	R	CHC SNR[7:0]							
BDI_CTL	25	R/W	Reserved						BDI LPSelect	Reserved
DMP_CTL	26	R/W	Reserved							DMP Disable CSI Weight
TPS_RCVD_1	27	R	Reserved	TPS Changed	TPS BCHOK	TPS Sync	Reserved		TPSRCVFrame[1:0]	
TPS_RCVD_2	28	R	Reserved	TPSRCVHierarchy[2:0]			Reserved		TPSRCV Constellation[1:0]	
TPS_RCVD_3	29	R	Reserved	TPSRCVLPCode[2:0]			Reserved	TPSRCVHPCode[2:0]		
TPS_RCVD_4	2A	R	Reserved		TPSRCVGuard[1:0]		Reserved		TPSRCVMode[1:0]	
TPS_RESERVED_1_ODD	2B	R	TPS Reserved Odd[7:0]							
TPS_RESERVED_2_ODD	2C	R	Reserved		TPS Reserved Odd[13:8]					
TPS_SET_1	2D	R/W	Reserved						TPSSETFrame[1:0]	
TPS_SET_2	2E	R/W	Reserved	TPSSETHierarchy[2:0]			Reserved		TPSSET Constellation[1:0]	
TPS_SET_3	2F	R/W	Reserved	TPSSETLPCode[2:0]			Reserved	TPSSETHPCode[2:0]		
TPS_CTL	30	R/W	Reserved					Use First TPS Now	TPS Ignore BCH	TPS Disable Update
CTL_FFTOSNUM	31	R	Reserved	CTL FFTOSNUM[6:0]						
PIR_CTL	34	R/W	Reserved							Freeze
SNR_CARRIER	35	R/W	SNR Carrier Number[7:0]							
	36	R/W	Mean	Reserved		SNR Carrier Number[12:8]				
PPM_CPAMP	37	R	PPMContPilotCorrAmp							
CAS_CTRL_2	46	R/W	TPS Length Indicator[5:0]						CCS State	ACSDIS2
SYR_EPLEP	47	R/W	Reserved	Signalscf			SYR_EPLEP[3:0]			
SYR_NUMSYMSTTRACK2K	48	R/W	Reserved		NUMSYMSTTRACK2K[5:0]					
SYR_NUMSYMSTTRACK8K	49	R/W	Reserved		NUMSYMSTTRACK8K[5:0]					
SYR_TRACKCLIPLEVEL	4A	R/W	Reserved		FTRACKCLIPLEVEL[2:0]			TTRACKCLIPLEVEL[2:0]		
SYR_DOPPLER	4B	R/W	Reserved		DOPPLERHYSTER[2:0]			FALSEALIASLEVEL[2:0]		
SYR_MISC1	4C	R/W	ZEROGUARDBACKOFF[2:0]			AUTOGUARDBACKOFF[3:0]				ONE-PATH SLOPE ENABLE
SYR_MISC2	4F	R/W	CCIDETECTLEVEL[2:0]			FORCEDOFFSET[4:0]				
SYR_MISC3	51	R/W	Reserved	CIRHOLDBACKOFF[1:0]		CIRHOLDLEVEL[1:0]		CIR HOLD DISABLE	HALFTIME CONTROL[1:0]	
AGC_ENH_CTL	52	R/W	Reserved		AGC_PW 12BIT ENABLE	AGCENHUPDATE[3:0]				AGC ENH ENABLE
AGC_MEAN_CX	53	R/W	Reserved				AGCMEANCX[3:0]			
AGC_BWREDOFFSET	54	R/W	Reserved				AGCBWREDOFFSET[3:0]			
AGC_MINGAIN	55	R/W	AGCMINGAIN[7:0]							
AGC_MODIFIED_TARGET_I	56	R	AGC MODIFIED TARGET I[7:0]							
SYR_MISC4	57	R/W	CCS Count Limit[3:0]				MP Moved Count Limit[3:0]			
SYR_NUMBINSLOOKBACK	58	R/W	Reserved		Num Bins LookBack[5:0]					
New Registers for CXD1968AR										
SYR_CPLXMFENABLE	59	R/W	8K 1/4	8K 1/8	8K 1/16	8K 1/32	2K 1/4	2K 1/8	2K 1/16	2K 1/32
TEST10	5A	R/W	Reserved				TEST10[3]	TEST10[2]	TEST10[1]	TEST10[0]
TEST11	5B	R/W	Reserved		TEST11[5:0]					

Name	Addr.	R/W	7	6	5	4	3	2	1	0
SYR_MISC5	5C	R/W	Skirtrmv	Numsymsftrack_lut[2:0]			Post echo ext enable	Nttrack chc	FFT 512	Echo stretch
AGC_MOD_TARGET_Q	5F	R	AGC_modified_target_q[7:0]							
AGC_GAIN_3	60	R	Agc_gain_q[7:0]							
AGC_GAIN_4	61	R	Reserved				Agc_gain_q[11:8]			
QIC_MISC1	62	R/W	Reserved				QIC Enable	QIC Gain[2:0]		
QIC_IQPHASEERR	63	R	IQPhaseErr[7:0]							
TRL_NOMINALRATE_0	65	R/W	trlnominalrate_0[7:0]							
CHC_LEAKAGE	6B	R/W	Reserved				CHC_LEAKAGE[3:0]			
TEST1	6C	R/W	Reserved							TEST1[0]
TEST2	6D	R/W	TEST2[7:0]							
TEST3	70	R/W	TEST3[7]	Reserved		TEST3[4:0]				
TEST4	71	R	TEST4[7:0]							
TEST5	72	R	TEST5[7:0]							
TEST6	73	R	TEST6[7:0]							
TEST7	74	R/W	TEST7[7:0]							
TEST8	75	R/W	TEST8[7:0]							
AUTORCV_1	76	R/W	Reserved	Prescale_Val[6:0]						
AUTORCV_2	77	R/W	Activate	Scanning	XMS_Tuner_Wait[1:0]		Demod_Timeout_2K[3:0]			
CSF_MISC	78	R/W	Reserved							CSF_ Enable
AUTORCV_3	79	R/W	Reserved			TS_Lock_Timeout[4:0]				
AUTORCV_4	7A	R	Autorcv_Reserved[3:0]				Demod_Status[3:0]			
TPS_RESERVED_1_EVEN	7B	R	TPS_Reserved_Even[7:0]							
TPS_RESERVED_2_EVEN	7C	R	Reserved		TPS_Reserved_Even[13:8]					
DCC_OFFSET_I	7D	R	DCC_Offset_I[7:0]							
DCC_OFFSET_Q	7E	R	DCC_Offset_Q[7:0]							
DCC_MISC	7F	R/W	Reserved					DCC_Gain[1:0]		DCC_ Enable
FEC Registers										
FEC_PARAMS	80	R/W	Tsclk cont	Auto clear	Ser data on msb	TS parallel sel	Output Sel Msb	Measurement Sel	Tri State Outputs	Rs Disable
BB_PARAMS	81	R/W	Tsvalid Active High	Tssync Active High	Tserr Active High	Latch on posedge	Tsclk _204	TSsync byte	Tserr full	Tsclk full
BER_PERIOD	83	R/W	Reserved		Berest test mode	Ber Est Period[4:0]				
FEC_STATUS	84	R	Ber_ses	Ber_es	Lck Flag	Ts Llck Flag	Ts Synch Lock	Vtb Sync	New Ber es	Reserved
SET_SYNC_DETECT	86	R/W	Synch Cntr Mode	Ts Synch Cntr Mode	Sync Loss Lddr Length[2:0]			Synch Lddr Lngth[2:0]		
LT_QLTY_THRESHOLD	87	R/W	LT QLTY THRESHOLD[7:0]							
BER_ESTIMATE	88	R	BERCNT[7:0]							
	89	R	BERCNT[15:8]							
	8A	R	New Estimate	Reserved		BERCNT overflow	BERCNT[19:16]			
CWRJCT_CNT	8B	R	CWRJCT CNT[7:0]							
	8C	R	CWRJCT CNT[15:8]							
VIT_CTRL	90	R/W	Rate Sel	Rate[2:0]			Reserved	Bert[2:0]		
VIT_SN	91	R/W	Reserved			SN[9:5]				
VIT_ST	92	R/W	Reserved				ST[12:9]			

Name	Addr.	R/W	7	6	5	4	3	2	1	0
VIT_BER	93	R	VBER[7:0]							
	94	R	VBER[15:8]							
Miscellaneous Registers										
CHIP_INFO	A0	R	CHIP Identification						Version	
RST_REG	A2	R/W	Adc rst	Cofdm rst	Vit rst	Fec rst	Reserved	Hard	Cold	Warm
INTERRUPT_SOURCE	A3	R/W	Ts if int	Cofdm Int	Ts synch Lock	Ts Llck Flag	Reserved	Ber_Es	Ber_Ses	Rs Cwrjct Flag
INTERRUPT_MASK	A4	R/W	Ts if int en	Cofdm Int En	Ts Synch	Ts Llck Flag En	Reserved	Ber_Es En	Ber_Ses En	Rs Cwrjct Flag En
TIMEOUT_VAL	A6	R/W	TIMEOUT VAL[7:0]							
PLL_FODR	A7	R/W	Reserved	OD[1:0]		R[4:0]				
PLL_F	A8	R/W	F[7:0]							
PLL_CONTROL	A9	R/W	Reserved	PLL power down	PLL op enable	PLL bypass	Ext clk enable	PLL op invert	PLL test mode	Clock disable
TUNER_CTRL_5	AF	R/W	Enable quiet i2c	i2c FET enable	Reserved					
AUTO_RESET	B1	R/W	Reserved							disable
RF_IFAGC_CTRL	B2	R/W	RF/IF AGCQ PWM[1:0]		Reserved	IF AGC EN	RF/IF AGCQ MODE		RF/IF AGCQ GPO	RF/IF AGCQ GPI
	B3	R/W	RF/IF AGCQ PWM[9:2]							
SMOOTH_CTRL	B4	R/W	CHANNEL WIDTH[1:0]		Reserved			RESET	DATA PERIOD AUTO	ENABLE
SMOOTH_STAT	B5	R/W	Reserved						UNDER FLOW	OVER FLOW
SMOOTH_DELAY	B6	R/W	DELAY[7:0]							
SMOOTH_DP	B7	R/W	DATA_PERIOD[7:0]							
	B8	R/W	DATA_PERIOD[15:8]							
ADC_CONTROL	B9	R/W	Reserved	Reserved	RST_Q	Reserved	Reserved	Reserved	RST_I	Reserved
ADC_CONTROL2	BA	R/W	REFSEL		Ext A/D Select	ADC Offset 2s Comp	ADC test mode	DCCEN	CLKRCVEN	Reserved
RAM_CONTROL	BC	R/W	Reserved							RAM_ STAND BY
ADC_CONTROL3	BD	R/W	RINTEN_Q	RINTSEL_Q[2:0]			RINTEN_ I	RINTSEL_I[2:0]		
ADC_STATUS	BE	R	OVF_Q	UDF_Q	OVF_I	UDF_I	Reserved			

CXD1968AR COFDM Demodulator Core Registers

COR_CTL	Read/Write	RESET: 0x00
Offset Address: 0x00		

Bit	Name	Description		Default	R/W
7:6	Reserved			00	R/W
5	Core Active	Set to enable core operation. When “0” the core reverts to and is held in its IDLE mode. This bit will be the normal method of core enable and disable.		0	R/W
4	Hold	Set to prevent the state machine from changing state. For debugging only.		0	R/W
3:0	Core State	0000: State machine not forced 0001: WAIT_TRL 0010: WAIT_AGC 0011: WAIT_SYR 0100: WAIT_PPM 0101: WAIT_TPS 0110: MONITOR _TPS 0111 to 1111: Reserved	Core state override control, when a non-zero value is written into these bits the core state machine is forced into a specific state as listed. This field is for debugging only and not expected to be used in normal operation. In particular backward transitions may give rise to unpredictable behavior.	0000	R/W

COR_STAT	Read Only
Offset Address: 0x01	

Bit	Name	Description		Default	R/W
7	CHC Tracking	Set when CHC enters tracking state.		—	R
6	TPS Locked	Set when “acceptable” TPS data has been received. This depends on a good TPS BCH check (TPS_BCHOK) unless TPS_CTL (TPS Ignore BCH) is set – this differentiates TPS locked from TPS_RCVD_1 (TPSBCHOK). Cleared when the state machine is forced back into the IDLE state.		—	R
5	SYR Locked	Set when SYR is locked (guard interval and symbol position determined).		—	R
4	AGC Locked	Set when the AGC is locked.		—	R
3:0	Core State	0000: IDLE 0001: WAIT_TRL 0010: WAIT_AGC 0011: WAIT_SYR 0100: WAIT_PPM 0101: WAIT_TPS 0110: MONITOR _TPS 0111 to 1111: Reserved	Current core state	—	R

COR_INTEN	Read/Write	RESET: 0x00
Offset Address: 0x02		

Bit	Name	Description	Default	R/W
7	INTEN Global	Set to enable interrupts COR_INTEN[5:0].	0	R/W
6	Reserved		0	R/W
5	INTEN SYR SymEnd	Set to enable an interrupt on SYR symbol end.	0	R/W
4	INTEN FFT Done	Set to enable an interrupt on completion of FFT processing.	0	R/W
3	INTEN AGC Lock Change	Set to enable an interrupt on change of AGC lock.	0	R/W
2	INTEN TPS RCVD BCHBad	Set to enable an interrupt on receipt of a TPS block with bad BCH check. This interrupt is NOT influenced by the TPS_CTL (TPS Use BCH) register setting.	0	R/W
1	INTEN TPS RCVD Changed	Set to enable an interrupt on a change of TPS data (except frame number). This interrupt indicates that the contents of the TPS_RCVD_2, 3, 4 registers have changed, this only occurs at the end of a frame.	0	R/W
0	INTEN TPS RCVD Update	Set to enable an interrupt on receipt of a TPS block. This interrupt indicates that the TPS_RCVD_1, 2, 3, 4 registers have been updated, this only occurs at the end of a frame.	0	R/W

COR_INTSTAT	Read/Write	RESET: 0x00
Offset Address: 0x03		

Bit	Name	Description		Default	R/W
7:6	Reserved			00	R/W
5	INTSTAT SYR SymEnd	Interrupt on SYR symbol end.	Write a “1” to the appropriate bit to clear the interrupt flag.	0	R/W
4	INTSTAT FFT Done	Interrupt on FFT complete.		0	R/W
3	INTSTAT AGC Lock Change	Interrupt on change of AGC lock.		0	R/W
2	INTSTAT TPS BCHBad	Interrupt on receipt of a TPS block with bad BCH check.		0	R/W
1	INTSTAT TPS RCVD Changed	Interrupt on a change of TPS data (except frame number).		0	R/W
0	INTSTAT TPS RCVD Update	Interrupt on receipt of a TPS block.		0	R/W

COR_MODEGUARD	Read/Write	RESET: 0x00
Offset Address: 0x04		

Bit	Name	Description		Default	R/W
7	ZIF_ENABLE	If set, Zero IF interface is enabled. The core expects the presence of both I and Q channels.		0	R/W
6:4	Reserved			000	R/W
3	Force		If set, this forces the core to use the set mode and guard. The core will not attempt to lock to any other mode and guard even if they are set incorrectly.	0	R/W
2	Mode	0: Mode = 2K 1: Mode = 8K	Sets the mode for which the core attempts lock. Only applicable if Force = 1. If the mode is known then setting the mode here will reduce lock times.	0	R/W
1:0	Guard	00: Guard interval = 1/32 01: Guard interval = 1/16 10: Guard interval = 1/8 11: Guard interval = 1/4	Sets the guard interval for which the core attempts initial lock. If this is set incorrectly then the core will still automatically recover the correct guard. If the guard is known then setting the guard here will reduce lock times.	00	R/W

AGC_CTL	Read/Write	RESET: 0x08
Offset Address: 0x05		

Bit	Name	Description		Default	R/W
7:5	Delay Startup	Once the AGC has locked, the core begins acquisition. Setting these bits allows this to be delayed. The length of time delayed is DelayStartup × 4 symbols (in 8K mode) or DelayStartup × 16 symbols (in 2K mode). For example a value of DelayStartup = 3 will delay the acquisition by ~11ms in with a 1/32 guard (i.e. 12 8K-symbols or 48 2K-symbols).		000	R/W
4	AGC Use Last Value	After the COR_CTL (Core Active) bit has been set, then a value of zero in this bit will cause the AGC to start at mid range and the DAGC to start at a gain of “1”. In this instance it is necessary to wait for the external RC to settle. If this bit is set then the AGC and DAGC will retain their last gain settings which is useful for reducing lock times for reacquisition after loss of lock.		0	R/W
3:2	AGCBW Reduction	00: No reduction 01: Reduce BW by 2 10: Reduce BW by 4 (Default) 11: Reduce BW by 8	When the AGC loop locks the BW of the loop is reduced by the following factors.	10	R/W
1	AGC Neg	When set, the AGC level output decreases when a larger signal is required, otherwise the AGC level output increases when a larger signal is required.		0	R/W
0	AGC Set	When set, the AGC output gain control value is set to AGC Manual. The AGC continues to monitor the received signal level.		0	R/W

AGC_MANUAL_1 Read/Write RESET: 0x00 Offset Address: 0x06				
Bit	Name	Description	Default	R/W
7:0	AGC Manual	AGC manual setting bits 7:0	00h	R/W

AGC_MANUAL_2 Read/Write RESET: 0x00 Offset Address: 0x07				
Bit	Name	Description	Default	R/W
7:4	Reserved		0000	R/W
3:0	AGC Manual	AGC manual setting bits 11:8	0000	R/W

Note) 1. In the time interval between host writes to AGC_MANUAL_1 and AGC_MANUAL_2, the manual control to the AGC will have an intermediate value.
2. AGC Manual has been extended by 2 bits for the CXD1968AR and CXD1976R compared to the CXD1973Q. AGC_MANUAL_2[3:2] were previously reserved bits that are now used for this purpose.
3. AGC_MANUAL is a 2's compliment value.

AGC_TARGET Read/Write RESET: 0x28 Offset Address: 0x08				
Bit	Name	Description	Default	R/W
7:0	AGC Target	AGC target bits 7:0. This register sets the base AGC target level.	28h	R/W

Note) The default value will give 12.5dB headroom with 1Vp-p ADC input range for gaussian signals.

AGC_GAIN_1 Read Only Offset Address: 0x09				
Bit	Name	Description	Default	R/W
7:0	AGC Gain I	Current (or latched) AGC gain bits 7:0	—	R/W

AGC_GAIN_2 Read/Write RESET: 0x00 Offset Address: 0x0A				
Bit	Name	Description	Default	R/W
7	AGC_AFTER_DCC	If set, the input signal to AGC is a DC-free signal, provided DCC is enabled.	0	R/W
6	LOCK_Q	AGC locked indication on the Q channel	0	R
5	LOCK_I	AGC locked indication on the I channel	0	R
4	AGC Locked	AGC locked indication	0	R
3:0	AGC Gain I	Current (or latched) AGC gain bits 11:8	0	R

Note) 1. AGC gain is the AGC value in normal operation, but is NOT influenced by AGC_CTL (AGC Set). Refer to PIR_CTL register description for details of the latched mode.
2. The AGC gain range read back is –2048 to +2047.
3. AGC Gain has been extended by 2 bits for the CXD1968AR and CXD1976R compared to the CXD1973Q. AGC_GAIN_2[3:2] were previously reserved bits that are now used for this purpose.

ITB_CTL	Read/Write	RESET: 0x00
Offset Address: 0x0B		

Bit	Name	Description	Default	R/W
7:1	Reserved		00h	R/W
0	Spec Invert	Set to allow reversed frequency spectrum from tuner	0	R/W

ITB_FREQ_1	Read/Write	RESET: 0x00
Offset Address: 0x0C		See table below for recommended values.

Bit	Name	Description	Default	R/W
7:0	ITB Frequency[7:0]	Bits 7:0 of ITB frequency	00h	R/W

ITB_FREQ_2	Read/Write	RESET: 0x30
Offset Address: 0x0D		See table below for recommended values.

Bit	Name	Description	Default	R/W
7:6	Reserved		00	R/W
5:0	ITB Frequency[13:8]	Bits 13:8 of ITB frequency	30h	R/W

Note) The ITB_FREQ_1, 2 registers set the nominal IF frequency that is expected to be sampled by the ADC.

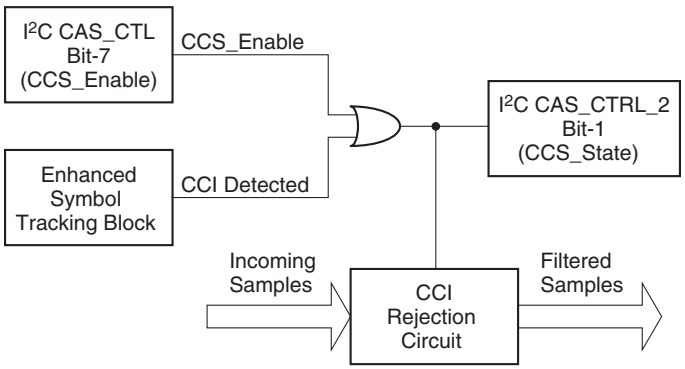
$$\text{ITBFREQ} = \frac{-1 \times F_{IF}}{F_{ADC}} \times 16384$$

If the IF is being undersampled (e.g. for High IFs) then F_{IF} is the subsampled IF equal to; $2 \times F_{ADC} - F_{IF}$. e.g. for 36.125MHz IF with a 20.48MHz ADC clock, F_{IF} = 4.835MHz.

IF [MHz]	F_{IF} [MHz]	F_{ADC} [MHz]	ITBFREQ
4.57	4.57	20.48	–3657 (31B7h)
36.00	4.96	20.48	–3968 (3080h)
36.125	4.835	20.48	–3868 (30E4h)
36.1667	4.7933	20.48	–3835 (3105h)
36.1667	4.8333	20.50	–3863 (30E9h)
36.0	5.0	20.50	–3996 (3064h)

CAS_CTL Read/Write RESET: 0x14 Offset Address: 0x0E					
Bit	Name	Description		Default	R/W
7	CCS Enable	Enable co-channel interference suppression (CCS) continuously within the CAS block. The CCS is off by default during normal operation, but is enabled automatically if CCI is detected regardless of the setting of this bit.		0	R/W
6	ACS Disable	Disable first stage of adjacent channel interference suppression within the CAS block. The first stage of ACS is on by default. The second stage can be enabled by CAS_CTRL_2 register for increased ACI rejection in 1 SAW tuner designs.		0	R/W
5	DAGC Disable	Disable the digital AGC within the CAS block. The digital AGC is on by default		0	R/W
4:3	DAGCBW Reduction	00: No reduction 01: Reduce BW by 2 10: Reduce BW by 4 (default) 11: Reduce BW by 8	Reduce DAGC BW once the SYR has locked.	10	R/W
2:0	CCSMU	Set the BW of the co-channel suppression filter. A large value corresponds to wide BW and vice versa. The reset value of 4 gives good performance for PAL interference.		100	R/W

Note) This diagram illustrates the selection logic for control of the CCI filter.



CAS_FREQ	Read/Write	RESET: 0xB3
Offset Address: 0x0F		

Bit	Name	Description	Default	R/W
7:0	CCS_Freq	Sets the center frequency of the co-channel suppression filter. The actual frequency (in MHz) is equal to; CCS center frequency = CCS_Freq × channel BW / 224 CCS_Freq is an 8-bit signed number and the reset value of –77 corresponds to a center of frequency of –2.75MHz in 8MHz channels. This is the same frequency as the vision carrier of PAL signals and thus centers the co-channel suppression filter on the vision carrier.	B3h	R/W

Note) 1. The co-channel suppression filter is automatically enabled by the enhanced symbol tracking block to remove co-channel interference whenever it is detected. It is also automatically enabled during acquisition. It is therefore important to program the CAS_FREQ register with the nominal frequency of the vision carrier of the likely CCI interference. Example values are given below.

2. For optimum performance this setting should be modified if the transmitter carrier frequency is offset, also shown in this table.

Vision carrier nominal position [MHz]	Channel BW [MHz]	CCS_Freq for COFDM offset CCS_Freq = (Fvc – Foffset) × 224 / BW						
		–500kHz	–333kHz	–166kHz	0kHz	166kHz	333kHz	500kHz
–1.75	6	–47 (D1h)	–53 (CBh)	–59 (C5h)	–65 (BFh)	–72 (B8h)	–78 (B2h)	–84 (ACh)
–2.25	7	–56 (C8h)	–61 (C3h)	–67 (BDh)	–72 (B8h)	–77 (B3h)	–83 (ADh)	–88 (A8h)
–2.75	8	–63 (C1h)	–68 (BCh)	–72 (B8h)	–77 (B3h)	–82 (AEh)	–86 (AAh)	–91 (A5h)

CAS_DAGCGAIN	Read Only
Offset Address: 0x10	

Bit	Name	Description	Default	R/W
7:0	CAS DAGC Gain	Digital automatic gain controller gain indication from CAS block. The actual gain of the digital AGC can be read from this register and is coded as follows. Actual gain = CAS DAGC Gain / 16 Therefore a gain of “1” is equivalent to a setting of “16” in this register.	—	R

TEST9	Read/Write	RESET: 0x00
Offset Address: 0x11		

Bit	Name	Description	Default	R/W
7	TEST9[7]		0	R/W
6:3	TEST9[6:3]		00h	R/W
2	TEST9[2]		0	R/W
1	TEST9[1]		0	
0	TEST9[0]		0	R/W

SYR_STAT Read Only Offset Address: 0x12					
Bit	Name	Description		Default	R/W
7:6	Reserved			—	R
5	TEST5			—	R
4	SYR Locked		SYR locked indication (guard detection and symbol position determined)	—	R
3	Reserved			—	R
2	SYR Mode	0: 2K 1: 8K	SYR detected mode	—	R
1:0	SYR Guard	00: 1/32 01: 1/16 10: 1/8 11: 1/4	SYR detected guard interval	—	R

FFT_CTL Read/Write RESET: 0x00 Offset Address: 0x17				
Bit	Name	Description	Default	R/W
7:3	Reserved		00h	R/W
2	FFT Test Trigger	A “0” to “1” transition causes the FFT to be triggered to perform an FFT on its current input buffer. Software should write “1” then “0” to this bit.	0	R/W
1	FFT Manual Mode	Set to disable FFT input buffer filling with off-air data.	0	R/W
0	FFT Inverse Transform	Inverse FFT selection. Set to “0” for normal OFDM demodulation.	0	R/W

SCR_CTL Read/Write RESET: 0x30 Offset Address: 0x18					
Bit	Name	Description		Default	R/W
7	Reserved			0	R/W
6:4	SYR Adjust Decay	000: 1 001: 1/2 010: 1/4 011: 1/8 100: 1/16 101: 1/32 110: 1/64 111: 1/128	These bits are not used in the CXD1968AR.	011	R/W
3:2	Reserved			00	R/W
1	SCR No Common Phase	Set to disable common phase error correction.		0	R/W
0	SCR Disable	Set to disable carrier phase slope correction. Note that this is not compatible with SYR tracking, so SYR_CTL (SYR Tracking Disable) must also be set.		0	R/W

PPM_CTL_1	Read/Write	RESET: 0x10
Offset Address: 0x19		See table below for settings.

Bit	Name	Description	Default	R/W
7	Reserved		0	R/W
6:4	PPMMaxFreq	Maximum search range setting for coarse frequency offset.	001	R/W
3	Reserved		0	R/W
2	Reduced Search Time Enable	If set, equalizes the frequency range in Hz searched in 2K and 8K modes. If clear, the search range in Hz is 4 times larger in 2K mode than in 8K mode, which can unnecessarily increase acquisition time in 2K mode. This setting is backward compatible with the CXD1973Q.	0	R/W
1	PPM Disable FindScat Pilots	Set to disable scattered pilot correlation. If disabled, acquisition is slowed down because the demodulator must wait for all TPS configuration before it can complete the acquisition sequence. The recommended setting for this bit is “0”.	0	R/W
0	PPM Bypass Corr	Set to bypass continuous pilot correlator.	0	R/W

Note) The CXD1968AR can acquire a wider range of frequency offsets than the CXD1973Q.
The table below shows the ranges that may be programed using PPMMaxFreq.

Reduce search time enable	PPM Max Freq	2K search range				8K search range				Remarks
		±FFT bins	Channel [±kHz]			±FFT bins	Channel [±kHz]			
			8MHz	7MHz	6MHz		8MHz	7MHz	6MHz	
0	000	31	138.4	121.1	103.8	31	34.6	30.3	25.9	Compatible with the CXD1973Q
0	001	63	281.3	246.1	210.9	63	70.3	61.5	52.7	Compatible with the CXD1973Q
0	010	127	567.0	496.1	425.2	127	141.7	124.0	106.3	Compatible with the CXD1973Q
0	011	255	1138.4	996.1	853.8	255	284.6	249.0	213.4	Compatible with the CXD1973Q
0	100	383	1709.8	1496.1	1282.4	383	427.5	374.0	320.6	
0	101	511	2281.3	1996.1	1710.9	511	570.3	499.0	427.7	
0	110	639	2852.7	2496.1	2139.5	639	713.2	624.0	534.9	
0	111	767	3424.1	2996.1	2568.1	767	856.0	749.0	642.0	
1	000	31	138.4	121.1	103.8	31	34.6	30.3	25.9	
1	001	31	138.4	121.1	103.8	63	70.3	61.5	52.7	
1	010	31	138.4	121.1	103.8	127	141.7	124.0	106.3	
1	011	63	281.3	246.1	210.9	255	284.6	249.0	213.4	166kHz transmit offset networks
1	100	63	281.3	246.1	210.9	383	427.5	374.0	320.6	
1	101	127	567.0	496.1	425.2	511	570.3	499.0	427.7	333kHz transmit offset networks
1	110	127	567.0	496.1	425.2	639	713.2	624.0	534.9	
1	111	255	1138.4	996.1	853.8	767	856.0	749.0	642.0	500kHz transmit offset networks

TRL_CTL	Read/Write	RESET: 0x14
Offset Address: 0x1A		

Bit	Name	Description	Default	R/W
7	Reserved		0	R/W
6:3	TRL Track Gain Factor	Additional gain (x/16) applied during tracking (default is to reduce gain by 1/8 during tracking).	0010	R/W
2:0	TRL Loop Gain	Sets the gain (x/16) of the sample timing loop during acquisition. Also sets the gain (combined with TRL track gain factor) during tracking.	100	R/W

TRL_NOMINALRATE_1	Read/Write	RESET: 0x00
Offset Address: 0x1B		See table below for recommended values.

Bit	Name	Description	Default	R/W
7:0	TRL Nominal Rate	Bits 15:8 of TRL nominal rate	00h	R/W

TRL_NOMINALRATE_2	Read/Write	RESET: 0x80
Offset Address: 0x1C		See table below for recommended values.

Bit	Name	Description	Default	R/W
7:0	TRL Nominal Rate	Bits 23:16 of TRL nominal rate	80h	R/W

Note) 1. The TRL_NOMINALRATE is a 24-bit non-contiguous register comprising three 8-bit registers called TRL_NOMINALRATE_2, TRL_NOMINALRATE_1 and TRL_NOMINALRATE_0. Also see the TRL_NOMINALRATE_0 register at address 0x65.

2. Sets the nominal rate of the sample timing NCO. This can be used to allow reduced bandwidth (6 and 7MHz) operation without changing crystal or tuner clock reference frequencies. TRL nominal rate is the ratio of the FFT time sample clock to the (fixed) ADC clock frequency.

$$\text{TRLNOMINALRATE} = \frac{16 \times \text{ChanBW}}{F_{ADC} \times 7} \times (2^{24})$$

The maximum allowable value of this register is 16777215. The minimum TRL nominal rate is 11184810.66 = AAAAABh. Some common settings are given below for a 20.48MHz crystal supplying the ADC clock, or from a 20.5MHz ADC clock derived from the PLL output.

Channel bandwidth	F_{ADC} = 20.48MHz	F_{ADC} = 20.5MHz
8MHz	14979657 (E49249h)	14965043 (E45933h)
7MHz	13107200 (C80000h)	13094412 (C7CE0Ch)
6MHz	11234743 (AB6DB7h)	11223782 (AB42E6h)

TRL_TIME_1		Read Only		
Offset Address: 0x1D				
Bit	Name	Description	Default	R/W
7:0	TRL Timing Offset	Current (or latched) bits 7:0 of TRL timing offset	—	R

TRL_TIME_2		Read Only		
Offset Address: 0x1E				
Bit	Name	Description	Default	R/W
7:0	TRL Timing Offset	Current (or latched) bits 15:8 of TRL timing offset	—	R

Note) 1. Refer to PIR_CTL register description for details of the latched mode. The timing offset in ppm is equal to;

Offset (ppm) = $1e^6 \times$ TRL timing offset / TRL_NOMINALRATE / 16

Example: for 8MHz OFDM using a 20.48MHz crystal

Offset (ppm) = TRL timing offset / 239.67

2. TRL timing offset is a signed quantity, in two's complement format.

CRL_CTL		Read/Write		RESET: 0x24
Offset Address: 0x1F				
Bit	Name	Description	Default	R/W
7	CRL Disable Fine	Set to disable SYR fine offset correction on CRL during acquisition.	0	R/W
6:3	CRL Track Gain Factor	Additional gain (x/16) applied during tracking (default is to reduce gain by 1/4 during tracking).	0100	R/W
2:0	CRL Loop Gain	Sets the gain (x/16) of the carrier loop during acquisition. Also sets the gain (combined with CRL track gain factor) during tracking.	100	R/W

CRL_FREQ_1 Read Only Offset Address: 0x20				
Bit	Name	Description	Default	R/W
7:0	CRL Frequency Offset	Current (or latched) bits 7:0 of CRL frequency offset	—	R

CRL_FREQ_2 Read Only Offset Address: 0x21				
Bit	Name	Description	Default	R/W
7:0	CRL Frequency Offset	Current (or latched) bits 15:8 of CRL frequency offset	—	R

CRL_FREQ_3 Read Only Offset Address: 0x22				
Bit	Name	Description	Default	R/W
7	SEXT	Sign extension: CRL frequency offset (23) ≤ CRL frequency offset (22)	—	R
6:0	CRL Frequency Offset	Current (or latched) bits 22:16 of CRL frequency offset	—	R

Note) 1. Refer to PIR_CTL register description for details of the latched mode.

2. The following relationships are defined:

   The carrier offset in FFT bins is equal to CRL frequency offset / 4096.

   For 2K mode, the carrier offset frequency (Hz) is equal to;
   CRL frequency offset × 1.0899 in 8MHz channel
   CRL frequency offset × 0.9537 in 7MHz channel
   CRL frequency offset × 0.8174 in 6MHz channel

   For 8K mode, the carrier offset frequency (Hz) is equal to;
   CRL frequency offset × 0.2725 in 8MHz channel
   CRL frequency offset × 0.2384 in 7MHz channel
   CRL frequency offset × 0.2044 in 6MHz channel

3. The value read back from the combined CRL_FREQ_1, CRL_FREQ_2, CRL_FREQ_3 registers in the CXD1968AR and CXD1976R is 1/4 of the value read back by the same registers in the CXD1973Q due to the increased frequency offset search range of the CXD1968AR and CXD1976R.

4. CRL frequency offset is a signed quantity, in two's complement format.

CHC_CTL_1		Read/Write		RESET: 0x01	
Offset Address: 0x23					
Bit	Name	Description		Default	R/W
7:5	Mean Pilot Gain	000: gain = 0 001: gain = 1/32 010: gain = 1/16 011: gain = 1/8 100: gain = 1/4 101: gain = 1/2 110, 111: gain = 1	Sets the mean pilot gain used in the channel predictor if the manual mean pilot bit is set.	000	R/W
4	Manual Mean Pilot	Set to allow the mean pilot gain to take on the value in bits 5:7. In normal operation the mean pilot gain is adaptively adjusted to suit the channel conditions.		0	R/W
3	Disable Bad Pilots	Set to disable bad pilots from being dropped in the PPM.		0	R/W
2	Disable Noise Normal	Set to disable noise normalization between scattered and continuous pilots.		0	R/W
1	Disable CHC Predictor	Set to disable the adaptive time domain prediction on the pilots.		0	R/W
0	CHC Interpolator	0: Linear 1: FIR	Sets the frequency domain interpolation method used.	1	R/W

CHC_SNR		Read Only		
Offset Address: 0x24				
Bit	Name	Description	Default	R/W
7:0	CHC SNR	Estimated signal-to-noise ratio (SNR) in dB. The value in this register either gives the average SNR of the channel or the SNR of a selected pilot as defined in the CHC_SNR_CARRIER register. The estimated value is independent of the channel response, and accurate to about ±1dB. $SNR[dB] = \frac{CHC\_SNR}{8}$ Note: The value compresses near the extremes.	—	R

BDI_CTL	Read/Write			RESET: 0x00
Offset Address: 0x25				
Bit	Name	Description	Default	R/W
7:2	Reserved		00h	R/W
1	BDI LPSelect	0: HP data and code rate 1: LP data and code rate	Selects priority of data for output to the FEC.	0	R/W
0	Reserved		NB: Do not set this bit to “1”.	0	R/W

DMP_CTL	Read/Write		RESET: 0x00
Offset Address: 0x26			
Bit	Name	Description	Default	R/W
7:1	Reserved		00h	R/W
0	DMP Disable CSI Weight	Set to disable soft decision weighting by CSI.	0	R/W

TPS_RCVD_1	Read Only		
Offset Address: 0x27			
Bit	Name	Description	Default	R/W
7	Reserved		—	R
6	TPS RCVD Changed Flag	Set when an update to TPS_RCVD_2, 3, 4 caused the data contents of the registers to change.	—	R
5	TPS RCVD BCHOK Flag	Set if the BCH check on the TPS data of the previous frame was correct. This bit is NOT influenced by TPS_CTL (TPS Use BCH).	—	R
4	TPS RCVD Sync Flag	Set if a TPS sync sequence was received. If the control state machine is in MONITOR_TPS, then this bit indicates presence/absence of a sync sequence in the previous frame (updated every time a new TPS frame is received). If the control state machine is NOT in MONITOR_TPS then this bit asserts as soon as a sync sequence is detected, deasserting if the BCH check subsequently fails.	—	R
3:2	Reserved		—	R
1:0	TPSRCVFrame	Frame number (within super-frame) indicated by TPS data received in the previous frame.	—	R

TPS_RCVD_2 Read Only Offset Address: 0x28					
Bit	Name	Description		Default	R/W
7	Reserved			—	R
6:4	TPSRCVHierarchy	000: Non hierarchical 001: α = 1 010: α = 2 011: α = 4 100 to 111: Reserved	Hierarchy information for current scheme	—	R
3:2	Reserved			—	R
1:0	TPSRCVConstellation	00: QPSK 01: QAM-16 10: QAM-64 11: Reserved	Constellation for current modulation scheme	—	R

TPS_RCVD_3 Read Only Offset Address: 0x29					
Bit	Name	Description		Default	R/W
7	Reserved			—	R
6:4	TPSRCVLPCode	000: 1/2 001: 2/3 010: 3/4 011: 5/6 100: 7/8 101 to 111: Reserved	Low priority stream code rate	—	R
3	Reserved			—	R
2:0	TPSRCVHPCode	000: 1/2 001: 2/3 010: 3/4 011: 5/6 100: 7/8 101 to 111: Reserved	High priority stream code rate	—	R

TPS_RCVD_4 Read Only Offset Address: 0x2A					
Bit	Name	Description		Default	R/W
7:6	Reserved			—	R
5:4	TPSRCVGuard	00: 1/32 01: 1/16 10: 1/8 11: 1/4	Guard interval	—	R
3:2	Reserved			—	R
1:0	TPSRCVMode	00: 2K Mode 01: 8K Mode 10, 11: Reserved	Transmission mode information	—	R

TPS_RESERVED_1_ODD		Read Only		
Offset Address: 0x2B				
Bit	Name	Description	Default	R/W
7:0	CELLID[15:8]	TPS reserved bits S40-S47 representing Cell-ID bits 15:8 respectively, received in TPS frame numbers 1 and 3.	—	R

TPS_RESERVED_2_ODD		Read Only		
Offset Address: 0x2C				
Bit	Name	Description	Default	R/W
7:6	Reserved			
5	TimeSliced Data	TPS reserved bit S48 – DVB-H time sliced data present in received data. In hierarchical mode, these bits correspond to HP stream.	—	R
4	MPE-FECData	TPS reserved bit S49 – DVB-H MPE-FEC encoded data present in received data. In hierarchical mode, these bits correspond to HP stream.	—	R
3:0	TPS_RESERVED_ODD	TPS reserved bits S50-S53 received during TPS frame numbers 1 and 3.	—	R

TPS_SET_1		Read/Write		RESET: 0x00
Offset Address: 0x2D				
Bit	Name	Description	Default	R/W
7:2	Reserved		00h	R/W
1:0	TPSSETFrame	Current frame number within super-frame as maintained by internal counters. The frame number is required to determine super-frame boundaries (for TPS_SET_x updates). The frame counter is initialized to the first received TPS frame data (TPSRCVFrame), i.e., TPS data received while the control state machine is in the WAIT_TPS state. The symbol counter increments at end of FFT processing. The frame counter increments when the symbol counter wraps from 67 to 0. With the control state machine in IDLE, writes to TPS_SET_1 take immediate effect. Otherwise, setting by the host takes effect at the beginning of the next frame (when FFT output symbol number wraps from 67 to 0). Only then will the register read-back the data written by the host.	00	R/W

TPS_SET_2	Read/Write	RESET: 0x00
Offset Address: 0x2E		

Bit	Name	Description		Default	R/W
7	Reserved			0	R/W
6:4	TPSSETHierarchy	000: Non hierarchical 001: α = 1 010: α = 2 011: α = 4 100 to 111: Reserved	Hierarchy information for current scheme	000	R/W
3:2	Reserved			00	R/W
1:0	TPSSETConstellation	00: QPSK 01: QAM-16 10: QAM-64 11: Reserved	Constellation for current modulation scheme	00	R/W

Note) 1. Data in this register corresponds to the actual parameters used by the core.

2. This register is updated (If TPS_CTL -TPS Disable Update is NOT set) from TPS_RCVD_2 when TPSSETFrame transitions from “3” to “0” (super-frame). Notice that the timing of the update does not coincide with updates to the TPS_RCVD_2 register.

3. With the control state machine in IDLE, writes to TPS_SET_2 take immediate effect. Otherwise, setting by the host takes effect at the beginning of the next super-frame. Only then will the register read-back the data written by the host.

TPS_SET_3	Read/Write	RESET: 0x00
Offset Address: 0x2F		

Bit	Name	Description		Default	R/W
7	Reserved			0	
6:4	TPSSETLPCode	000: 1/2 001: 2/3 010: 3/4 011: 5/6 100: 7/8 101 to 111: Reserved	Low priority stream code rate	000	R/W
3	Reserved			0	R/W
2:0	TPSSETHPCode	000: 1/2 001: 2/3 010: 3/4 011: 5/6 100: 7/8 101 to 111: Reserved	High priority stream code rate	000	R/W

Note) 1. Data in this register corresponds to the actual parameters used by the core.

2. This register is updated (If TPS_CTL -TPS Disable Update is NOT set) from TPS_RCVD_3 when TPSSETFrame transitions from “3” to “0” (super-frame). Notice that the timing of the update does not coincide with updates to the TPS_RCVD_3 register.

3. With the control state machine in IDLE, writes to TPS_SET_3 take immediate effect. Otherwise, setting by the host takes effect at the beginning of the next super-frame. Only then will the register read-back the data written by the host.

TPS_CTL		Read/Write		RESET: 0x04
Offset Address: 0x30				
Bit	Name	Description	Default	R/W
7:3	Reserved		00h	R/W
2	Use First TPS Immediately	By default, TPS_SET_2, 3 registers are updated from TPS_RCVD_2, 3 when TPSSetFrame transitions from “3” to “0” (super-frame). If this bit is set, then the FIRST acceptable TPS RCVD data (while state-machine is in WAIT_TPS) is loaded into the TPS_SET_2, 3 registers irrespective of TPS RCVD Frame number. This could assist faster acquisition, except in the superframe immediately prior to a parameter change.	1	R/W
1	TPS Ignore BCH	By default, TPS RCVD and TPS SET registers are updated only if the BCH check is OK (“good TPS”). When TPS Ignore BCH is set both TPS_RCVD and TPS_SET registers are updated irrespective of the BCH check.	0	R/W
0	TPS Disable Update	When set, this bit disables updating of the “SET” TPS data from “RCVD” TPS data in the data stream.	0	R/W

CTL_FFTOSNUM		Read Only		
Offset Address: 0x31				
Bit	Name	Description	Default	R/W
7	Reserved		—	R
6:0	CTL FFTOSNUM	FFT output symbol number counter (0...63). This counter increments every symbol when new symbol data is available at the output of the FFT. A value of 127 read from this register implies that the counter is not yet running (symbol number is not valid).	—	R

PIR_CTL		Read/Write		RESET: 0x00
Offset Address: 0x34				
Bit	Name	Description	Default	R/W
7:1	Reserved		00h	R/W
0	Freeze	AGC_GAIN, TRL_TIMEOFF, CRL_FREQOFF and BER_ESTIMATE are fields more than 8 bits which are each accommodated in more than one register. It is therefore possible for the field value to change in the time between the two reads from the register pair. When a “1” is written to the freeze bit (whether it was previously “0” or not), the field values are latched. With the freeze bit “0” the data within the fields changes dynamically.	0	R/W

SNR_CARRIER_1		Read/Write		RESET: 0x00
Offset Address: 0x35				
Bit	Name	Description	Default	R/W
7:0	SNR Carrier Number	Bits 7:0 of SNR_CARRIER. The 13 bits of the SNR carrier number specify which carrier's SNR is output in the CHC_SNR register allowing the SNR of each carrier to be monitored. Note: Once this register has been set then it may take up to 1 symbol (~1ms in 8K, ~0.25ms in 2K) for the CHC_SNR register to contain the correct value.	00h	R/W

SNR_CARRIER_2		Read/Write		RESET: 0x80
Offset Address: 0x36				
Bit	Name	Description	Default	R/W
7	Mean	If set, this outputs the means SNR of all the continuous pilots in the CHC_SNR register, otherwise the SNR of the specified carrier is output.	1	R/W
6:5	Reserved		00	R/W
4:0	SNR Carrier Number	Bits 12:8 of SNR_CARRIER. The 13 bits of the SNR carrier number specify which carrier's SNR is output in the CHC_SNR register allowing the SNR of each carrier to be monitored. Note: Once this register has been set then it may take up to 1 symbol (~1ms in 8K, ~0.25ms in 2K) for the CHC_SNR register to contain the correct value.	00h	R/W

PPM_CPAMP		Read Only		
Offset Address: 0x37				
Bit	Name	Description	Default	R/W
7:0	PPMContPilotCorrAmp	This value is the output of the PPM continuous pilot correlator. During continuous pilot correlation, it holds the peak detected value, at the end of scattered pilot correlation shows the peak detected value, and during normal operation shows a running measurement of the continuous pilot correlation. A value below 20 (2K) or 80 (8K) indicates that the OFDM signal may have disappeared, or is extremely noisy. A peak value of 42 or 176 (2K or 8K respectively) is attained with a perfect signal.	—	R

CAS_CTRL_2	Read/Write	RESET: 0x01
Offset Address: 0x46		

Bit	Name	Description	Default	R/W
7:2	TPS_LENGTH_INDICATOR	TPS bits S17-S22 – Indicates length of valid TPS data. Common values are; 0x17 (DVB-T no cell ID) 0x1F (DVB-T/H with cell ID) 0x21 (DVB-H with cell ID and TimeSlice and MPE-FEC signaled via TPS bits)	00h	R/W
1	CCS_STATE	Indicates status of CCS filter. 0: CAS CCS filter not active 1: CAS CCS filter active	0	R
0	ACSDIS2	Disable CAS block 2nd ACI filter stage.	1	R/W

SYR_EPLEP	Read/Write	RESET: 0x2F
Offset Address: 0x47		

Bit	Name	Description	Default	R/W
7	Reserved		0	R/W
6:4	signalscf	Noise rms level scale factor – determines lowest level of echo that can be equalized.	010	R/W
3:0	syr_eplep[3:0]	Edge of guard allowance in samples to optimize post-cursive long echo performance.	1111	R/W

SYR_NUMSYMSTTRACK2K	Read/Write	RESET: 0x10
Offset Address: 0x48		

Bit	Name	Description	Default	R/W
7:6	Reserved		00	R/W
5:0	NUMSYMSTTRACK2K	This register controls, for 2K mode, the duration of each symbol tracking period, in number of symbols, for the enhanced tracking block in time domain tracking mode.	10h	R/W

SYR_NUMSYMSTTRACK8K	Read/Write	RESET: 0x10
Offset Address: 0x49		

Bit	Name	Description	Default	R/W
7:6	Reserved		00	R/W
5:0	NUMSYMSTTRACK8K	This register controls, for 8K mode, the duration of each symbol tracking period, in number of symbols, for the enhanced tracking block in time domain tracking mode.	10h	R/W

SYR_TRACKCLIPLEVEL	Read/Write	RESET: 0x22
Offset Address: 0x4A		

Bit	Name	Description	Default	R/W
7:6	Reserved		00	R/W
5:3	FTRACKCLIPLEVEL	Sets the threshold of useful equalization i.e. the level of any echo path that must be equalized relative to the frequency domain noise floor. The default value of 4 relates to an echo level at approximately –21dB of the main path. (0: Lowest level, 7: Highest level).	100	R/W
2:0	TTRACKCLIPLEVEL	Sets the threshold of useful equalization i.e. the level of any echo path that must be equalized relative to the time domain noise floor. The default value of 2 relates to an echo level at approximately –21dB of the main path. (0: Lowest level, 7: Highest level).	010	R/W

SYR_DOPPLER	Read/Write	RESET: 0x14
Offset Address: 0x4B		

Bit	Name	Description	Default	R/W
7:6	Reserved		00	R/W
5:3	DOPPLERHYSTER	Sets the number of tracking periods during which the enhanced symbol tracker must observe a persistent change in the channel profile before reacting to it. Increasing this register value prevents the symbol tracker reacting to spurious and/or transient events.	010	R/W
2:0	FALSEALIASLEVEL	Sets the threshold level (FALSEALIASLEVEL) for valid path energy detection in the channel transfer function used for symbol tracking.	100	R/W

SYR_MISC1	Read/Write	RESET: 0xFE
Offset Address: 0x4C		

Bit	Name	Description	Default	R/W
7:5	ZEROGUARDBACKOFF	Sets threshold that must be satisfied to provide enough certainty to an auto-guard/mode detection outcome of 2K, 1/32. Lower to tighten the decision and increase to loosen the decision.	111	R/W
4:1	AUTOGUARDBACKOFF	Sets the threshold that must be satisfied to provide enough certainty on the auto-guard/mode detection outcome. Lower to tighten the decision and increase to loosen the decision.	1111	R/W
0	ONEPATH SLOPE ENABLE	Allows single path channels to be treated as long post-cursive or pre-cursive channels.	0	R/W

SYR_MISC2	Read/Write	RESET: 0x85
Offset Address: 0x4F		

Bit	Name	Description	Default	R/W
7:5	CCIDETECTLEVEL	Sets the threshold for turning on the CAS block co-channel suppression filter if CCI has been detected.	100	R/W
4:0	FORCEDOFFSET	Causes the enhanced symbol tracker to consistently shift the FFT window for each symbol by FORCEDOFFSET samples i.e. cause the FFT window to be early by FORCEDOFFSET samples. Use with modest values in doppler channels.	00101	R/W

Note) 1. The CCS filter is turned on whenever CCI is detected, and during acquisition even if the CCS Enable bit (bit 7 of the CAS_CTL register) is clear, so it is important that the CAS_FREQ register is set to the correct frequency to cancel the vision carrier of any CCI present. See description of the CAS_FREQ register.

2. Ensure that CCS is disabled prior to acquisition. Failure to do so will prevent automatic selection of CCS.

SYR_MISC3	Read/Write	RESET: 0x6A
Offset Address: 0x51		

Bit	Name	Description	Default	R/W
7	Reserved		0	R/W
6:5	CIRHOLDBACKOFF	Sets the amount of reduction α to apply to the CIR averaging where the averaging of the CIR from symbol to symbol is; $avCIR = avCIR + curCIR \times 2^{-\alpha}$	11	R/W
4:3	CIRHOLDLEVEL	Sets the power threshold which the CIR has to exceed to be deemed stable during an enhanced tracking period so that reduced CIR averaging can take place.	01	R/W
2	CIRHOLD DISABLE	0: Reduces averaging of the CIR in the enhanced tracker when the CIR profile is seen to be stable during a tracking period – desirable for time varying channels. 1: Maintain full averaging through out the tracking period.	0	R/W
1:0	HALFTIMECONTROL	Sets the calculation method for the duration of a tracking period (in symbols) for the enhanced tracker. 00: Duration fixed to NUMSYMSTTRACK2K or NUMSYMSTTRACK8K. 01: Duration alternates between N and 0.5N where N is either NUMSYMSTTRACK2K for 2K mode and NUMSYMSTTRACK8K for 8K mode. 10: Duration determined randomly from period to period. Ideal for time varying channels. 11: Reserved	10	R/W

AGC_ENH_CTL	Read/Write	RESET: 0x0C
Offset Address: 0x52		

Bit	Name	Description	Default	R/W
7:6	Reserved		00	R/W
5	AGC_PWM12BITENABLE	When set the 12-bit AGC and PWM is selected. This gives 12-bit resolution on the IFAGC PWM output instead of 10-bit resolution on the CXD1973Q.	0	R/W
4:1	AGCENHUPDATE	Enhanced AGC update rate. These bits determine the rate (in ADC samples) at which the AGC target level is updated when the enhanced AGC is enabled. The update rate in samples is given by; Samples per update = (AGCENHUPDATE + 1) × 8192 The default is 57,344 samples.	0110	R/W
0	AGC ENHENABLE	Enhanced AGC enable. When set, the AGC target level set by the AGC_TARGET register, is automatically optimized to maximize ADC dynamic range, once AGC lock has occurred. This improves performance in channels where the interference produces non-gaussian distribution in the sampled input signal, such as channels with large amounts of PAL ACI. This is not recommended for use with dual AGC control in ZIF mode.	0	R/W

AGC_MEAN_CX	Read/Write	RESET: 0x04
Offset Address: 0x53		

Bit	Name	Description	Default	R/W
7:4	Reserved		0000	R/W
3:0	AGCMEANCX	Sets the mean value of threshold crossings in enhanced AGC algorithm. This value determines the number of times a sample can exceed an internal threshold before the AGC target value is decreased. The recommended value is “4”.	0100	R/W

AGC_BWREDOFFSET	Read/Write	RESET: 0x0A
Offset Address: 0x54		

Bit	Name	Description	Default	R/W
7:4	Reserved		0000	R/W
3:0	AGCBWREDOFFSET	AGC bandwidth reduction offset. Sets a base level AGC gain reduction which is reduced further by AGC_CTL (AGC BW Reduction) after AGC lock is achieved.	1010	R/W

Note) 1. Higher values result in lower gains, lower bandwidth and longer acquisition times.
2. Lower values result in higher gains, higher bandwidth and shorter acquisition times.
3. To prevent excessive AGC gain fluctuation from too high a bandwidth, it is recommended that the sum of AGCBWREDOFFSET and AGC_CTL(AGC BW Reduction) should exceed 4. The default of AGCBWREDOFFSET = 10 maintains compatibility with the CXD1973Q.

AGC_MINGAIN		Read/Write		RESET: 0x80
Offset Address: 0x55				
Bit	Name	Description	Default	R/W
7:0	AGCMINGAIN	AGC minimum gain. Sets a minimum gain limit for the IFAGC output. This register is a signed 8-bit value which sets the minimum gain according to the table below.	80h	R/W

Note) 1. MinGain is the minimum gain limit required at the IFAGC output, scaled to a 12-bit or 10-bit signed value depending upon the AGC resolution set in the AGC_PWM_ENH_CTL register.

AGC resolution (bits)	AGC_CTL (AGC_NEG)	AGCMINGAIN
12	0	MinGain / 16
12	1	–MinGain / 16
10	0	MinGain / 4
10	1	–MinGain / 4

Example using 12-bit AGC with positive gain polarity:
Where the IFAGC output gain range is from –2048 (low gain) to +2047 (high gain) in 12-bit AGC mode with AGC_CTL (AGC_NEG) = 0, and the minimum gain is to be limited to -1024.

AGCMINGAIN = –1024/16 = –64

Example using 10-bit AGC with negative gain polarity:
Where the IFAGC output gain range is from +512 (low gain) to –512 (high gain) in 10-bit AGC mode with AGC_CTL (AGC_NEG) = 1, and the minimum gain is to be limited to 256.

AGCMINGAIN = –256/4 = –64

2. The default value of –128 is compatible with the CXD1973Q giving full AGC gain range with no limiting.

AGC_MODIFIED_TARGET_I		Read Only		
Offset Address: 0x56				
Bit	Name	Description	Default	R/W
7:0	AGC_MODIFIED_TARGET_I	When the AGC is “not locked”, this register will read back the user requested AGC target value as set in the AGC_TARGET register. When the AGC is “locked” (and the AGC_ENHANCED_ENABLE bit is set active high in the AGC_PWM_ENH_CTL register), this register will contain the top 8 MSBs of the internally modified AGC target value as dictated by the I channel conditions.	—	R

SYR_MISC4	Read/Write	RESET: 0x03
Offset Address: 0x57		

Bit	Name	Description	Default	R/W
7:4	CCS Count Limit	Sets CCS count limit. If zero, the CCS filter remains on once enabled by the enhanced tracker.	0000	R/W
3:0	MP Moved Count Limit	Sets MP moved count limit. The maximum number of enhanced symbol tracker periods for automatic update. Set to “0” to disable this functionality.	0011	R/W

SYR_NUMBINSLOOKBACK	Read/Write	RESET: 0x0F
Offset Address: 0x58		

Bit	Name	Description	Default	R/W
7:6	Reserved		00	R/W
5:0	NumBinsLookBack	Sets the range over which to search for each new update to the FFT window start time during each enhanced tracker tracking period.	0Fh	R/W

Registers new to CXD1968AR

SYR_CPLXMFENABLE		Read/Write		RESET: 0xFF
Offset Address: 0x59				
Bit	Name	Description	Default	R/W
7	8K 1/4	Enables complex matched filtering for the enhanced tracker in the named modes. Improves doppler channel performance.	1	R/W
6	8K 1/8		1	R/W
5	8K 1/16		1	R/W
4	8K 1/32		1	R/W
3	2K 1/4		1	R/W
2	2K 1/8		1	R/W
1	2K 1/16		1	R/W
0	2K 1/32		1	R/W

TEST10		Read/Write		RESET: 0x0F
Offset Address: 0x5A				
Bit	Name	Description	Default	R/W
7:4	Reserved		0	R/W
3	TEST10[3]		1	R/W
2	TEST10[2]		1	R/W
1	TEST10[1]		1	R/W
0	TEST10[0]		1	R/W

TEST11		Read/Write		RESET: 0x10
Offset Address: 0x5B				
Bit	Name	Description	Default	R/W
7:6	Reserved		00	R/W
5:0	TEST11[5:0]		10h	R/W

SYR_MISC5	Read/Write	RESET: 0x79
Offset Address: 0x5C		

Bit	Name	Description	Default	R/W
7	SKIRTRMV	Enables removal of skirt in enhanced tracking mode.	0	R/W
6:4	NUMSYMSFTRACK_LUT	Must be set to “7” in the CXD1968AR.	111	R/W
3	POST ECHO EXT ENABLE	Set to “0” to enable a longer observation period before responding to emerging pre-echoes.	1	R/W
2	NTTRACK CHC	Controls re-computations inside enhanced tracker.	0	R/W
1	FFT 512	Enables use of 512 point IFFT in enhanced tracker.	0	R/W
0	ECHO STRETCH	Enables support for automatically detecting and tracking echoes outside the guard interval.	1	R/W

Note) Use Sony recommended settings for this register.

AGC_MOD_TARGET_Q	Read Only
Offset Address: 0x5F	

Bit	Name	Description	Default	R/W
7:0	AGC_MODIFIED_ TARGET_Q	When the AGC is “not locked”, this register will read back the user requested AGC target value as set in the AGC_TARGET register. When the AGC is “locked” (and the AGC_ENHANCED_ENABLE bit is set active high in the AGC_PWM_ENH_CTL register), this register will contain the top 8 MSBs of the internally modified AGC target value as dictated by the Q channel conditions.	—	R

AGC_GAIN_3	Read Only
Offset Address: 0x60	

Bit	Name	Description	Default	R/W
7:0	AGC_GAIN_Q	Current (or latched) AGC gain bits 7:0 for the Q channel	—	R

AGC_GAIN_4	Read Only
Offset Address: 0x61	

Bit	Name	Description	Default	R/W
7:4	Reserved		—	R
3:0	AGC_GAIN_Q	Current (or latched) AGC gain bits 11:8 for the Q channel	—	R

QIC_MISC1		Read/Write		RESET: 0x0B
Offset Address: 0x62				
Bit	Name	Description	Default	R/W
7:4	Reserved		0	R/W
3	QIC ENABLE	If set, enables the IQ phase imbalance (non-frequency selective) detection/correction. This bit should be set when using ZIF tuners to correct I/Q phase imbalance.	1	R/W
2:0	QIC_GAIN	Sets the loop gain value of the IQ phase imbalance corrector: smaller values speed up the convergence rate.	011	R/W

QIC_GAIN	Loop gain value
000	1/256
001	1/512
010	1/1024
011	1/2048
100	1/4096
101	1/8192
110	1/16,384
111	1/32,768

QIC_IQPHASEERR		Read	0x00
Offset Address: 0x63			
Bit	Name	Description	Default	R/W
7:0	IQPhaseErr	Detected IQ phase imbalance value. Phase imbalance (Degrees) = IQPhaseErr / 4	—	R

TRL_NOMINALRATE_0		Read/Write	0x00
Offset Address: 0x65			
Bit	Name	Description	Default	R/W
7:0	TRL Nominal Rate	Bits 7:0 of TRL nominal rate	00	R/W

Note) 1. The TRL_NOMINALRATE is a 24-bit non-contiguous register comprising three 8-bit registers called TRL_NOMINALRATE_2, TRL_NOMINALRATE_1 and TRL_NOMINALRATE_0.

2. Also see TRL_NOMINALRATE_1 at address 0x1B and TRL_NOMINALRATE_2 at address 0x1C.

CHC_LEAKAGE	Read/Write	RESET: 0x0B		
Offset Address: 0x6B				
Bit	Name	Description	Default	R/W
7:4	Reserved		0	R/W
3:0	CHC_LEAKAGE	CHC correction factor for doppler channels. If CHC_LEAKAGE set to “0”, no correction is applied. otherwise; Correction factor = 1 / [$2^{(CHC\_LEAKAGE + 2)}$] ie. For CHC_LEAKAGE = 11 (default); Correction factor = 1/8192	Bh	R/W

TEST1	Read/Write	RESET: 0x00		
Offset Address: 0x6C				
Bit	Name	Description	Default	R/W
7:1	Reserved		0	R/W
0	TEST1[0]	Test use only	0	R/W

TEST2	Read/Write	RESET: 0x00		
Offset Address: 0x6D				
Bit	Name	Description	Default	R/W
7:0	TEST[7:0]	Test use only	00	R/W

TEST3	Read/Write	RESET: 0x0A		
Offset Address: 0x70				
Bit	Name	Description	Default	R/W
7	TEST3[7]	Test use only	0	R/W
6:5	Reserved		00	R/W
4:0	TEST3[4:0]	Test use only	Ah	R/W

TEST4	Read Only			
Offset Address: 0x71				
Bit	Name	Description	Default	R/W
7:0	TEST[7:0]	Test use only	—	R

TEST5		Read Only		
Offset Address: 0x72				
Bit	Name	Description	Default	R/W
7:0	TEST5[7:0]	Test use only	—	R

TEST6		Read Only		
Offset Address: 0x73				
Bit	Name	Description	Default	R/W
7:0	TEST6[7:0]	Test use only	—	R

TEST7		Read/Write		RESET: 0x00
Offset Address: 0x74				
Bit	Name	Description	Default	R/W
7:0	TEST7[7:0]	Test use only	00h	R/W

TEST8		Read/Write		RESET: 0xFF
Offset Address: 0x75				
Bit	Name	Description	Default	R/W
7:0	TEST8[7:0]	Test use only	FFh	R/W

AUTORCV_1		Read/Write		RESET: 0x29
Offset Address: 0x76				
Bit	Name	Description	Default	R/W
7	Reserved		0	R/W
6:0	PRESCALE_VAL	Used to define the number of clock periods contained in a 1μs time interval, for use by the auto-recovery state machine. Will allow definitions for up to 127MHz logic clock frequencies, where logic clock frequency = 2 × ADC clock frequency.	29h	R/W

AUTORCV_2	Read/Write	RESET: 0x18
Offset Address: 0x77		

Bit	Name	Description	Default	R/W
7	ACTIVATE	When set, this bit will activate the auto-recovery functionality.	0	R/W
6	SCANNING	Used to differentiate between channel scanning (setup mode) and channel zapping (user mode). When set to “1”, this specifies the scanning mode. When cleared to “0”, this specifies zapping mode.	0	R/W
5:4	XMS_TUNER_WAIT	The delay specified here will be used as the waiting time before advancing the auto-recovery state machine to the demodulator acquisition state. 00: 7ms delay 01: 49ms delay 10: 119ms delay 11: 147ms delay	01	R/W
3:0	DEMOD_TIMEOUT_2K	This value specifies the maximum delay required to achieve a TPS-data locked indication once the tuner is settled, (2K mode ONLY, using 7ms increments). Timeouts for the 8K mode are calculated automatically by the CXD1968AR using this 2K timeout value, as shown below. 2K mode → Maximum AGC lock time + 235 symbols → 47ms + 65.8ms Timeout value for “demod_timeout_2k” = 66/7ms ≅ 9. TPS_demod_timeout for 8K = AGC_lock time + [demod_timeout_2K × 4] The recommended value for the “demod_timeout_2k” register is 9h (1001’b).	1000	R/W

Note) The table below describes the receiver mode of operation with respect to the values contained in the coreactive bit (0x00, bit5) and the activate AR bit (0x77 bit7).

Coreactive	AR active	Description
0	0	Chip idle (as in the CXD1973Q/CXD1976R)
0	1	Auto-recovery state machine active
1	0	Ordinary/Default manual mode active (as in the CXD1973Q/CXD1976R)
1	1	User has programed core active as well as setting AR active. Auto-recovery will take over control, but this is not a recommended mode of use.

CSF_MISC	Read/Write	RESET: 0x01
Offset Address: 0x78		

Bit	Name	Description	Default	R/W
7:1	Reserved	TBD	0	R/W
0	CSF_ENABLE	If set, channel selection filter enabled.	1	R/W

AUTORCV_3	Read/Write	RESET: 0x1C		
Offset Address: 0x79				
Bit	Name	Description	Default	R/W
7:5	Reserved	TBD	000	R/W
4:0	TS_LOCK_TIMEOUT	This value represents the maximum allowable delay for achieving a TS lock indication, after a TPS locked indication has been achieved. Worst case delay = 204 symbols (8K) + 38 packets @ 5M baud = 195ms (= 28 using 7ms increments)	11100	R/W

AUTORCV_4	Read Only			
Offset Address: 0x7A				
Bit	Name	Description	Default	R/W
7:4	AUTORCV_RESERVED	TBD	—	R
3:0	DEMOD_STATUS	This signifies the current status of the demodulator as reported by the auto-recovery state machine. BIT 0: When set, reports that the TPS status can now be read (TPS_STATUS_READY). BIT 1: When set, reports that the TS status can now be read (TS_STATUS_READY). BIT 2: When set, reports TPS lock achieved. When cleared, reports TPS lock NOT achieved. Only valid when bit 0 is set. BIT 3: When set, reports TS lock achieved. When cleared, reports TS lock NOT achieved. Only valid when bit 1 is set.	—	R

TPS_RESERVED_1_EVEN	Read Only			
Offset Address: 0x7B				
Bit	Name	Description	Default	R/W
7:0	CELLID[7:0]	TPS reserved bits S40-S47 representing Cell-ID bits 7:0 respectively, received in TPS frame numbers 2 and 4.	—	R

TPS_RESERVED_2_EVEN Read Only Offset Address: 0x7C				
Bit	Name	Description	Default	Bit
7:6	Reserved	Not used	—	R
5	TimeSlicedData	TPS reserved bit S48 – DVB-H time sliced data present in received data. In hierarchical mode, these bits correspond to LP stream.	—	R
4	MPE-FECData	TPS reserved bit S49 – DVB-H MPE-FEC encoded data present in received data. In hierarchical mode, these bits correspond to LP stream.	—	R
3:0	TPS_RESERVED_EVEN	TPS reserved bits S50-S53 received during TPS frame numbers 2 and 4.	—	R

DCC_OFFSET_I Read Only Offset Address: 0x7D				
Bit	Name	Description	Default	R/W
7:0	DCC_OFFSET_I	Detected DC offset value on the I channel (signed)	—	R

DCC_OFFSET_Q Read Only Offset Address: 0x7E				
Bit	Name	Description	Default	R/W
7:0	DCC_OFFSET_Q	Detected DC offset value on the Q channel (signed)	—	R

DCC_MISC Read/Write RESET: 0x03 Offset Address: 0x7F				
Bit	Name	Description	Default	R/W
7:3	RESERVED		00000	R/W
2:1	DCC_GAIN	Sets the DCC gain value as indicated in the table below: Register value / 2K Mode / 8K Mode 0 / 2^{-16} / 2^{-18} 1 / 2^{-17} / 2^{-19} 2 / 2^{-18} / 2^{-20} 3 / 2^{-19} / 2^{-21}	01	R/W
0	DCC_ENABLE	If set, DC offset cancellation is enabled. This bit should be set when using DC-coupled ZIF tuners.	1	R/W

FEC Registers

FEC_PARAMS		Read/Write		RESET: 0x1A
Offset Address: 0x80				fec_param reset
Bit	Name	Description	Default	R/W
7	Tsclk_cont	If the TSCLK output is gated (bit Tsclk_full of BBPARAMS low) and TS smoothing enabled (bit ENABLE of SMOOTH_CTRL high), then setting this bit ensures that the TSCLK output remains active during any gap in the TS output. 0: TSCLK inactive during gaps 1: TSCLK active during gaps	0	R/W
6	Auto_clear	Auto clearing of Interrupt flag. 0: Auto clear disabled 1: Auto clear enabled	0	R/W
5	Ser_data_on_msb	When the transport stream is operating in its serial mode (see bit 4 below) this bit controls on which TSDATA bit the serial data is presented. 0: Data is presented on TSDATA[0] 1: Data is presented on TSDATA[7]	0	R/W
4	TS_parallel_sel	Determines whether the parallel or serial interface for the transport stream is selected. 0: Serial interface selected 1: Parallel interface selected When serial interface selected, Pins TSDATA[7] or TSDATA[0] (see bit 5 above) drive the serial data.	1	R/W
3	Output_Sel_Msb	Selects whether the most significant bit of a byte is presented on TSDATA bit[7] or bit[0]. In serial mode this bit selects whether the most significant bit is presented as the first or last bit of a byte. 0: MSB is TSDATA[0] (last bit, serial mode). 1: MSB is TSDATA[7] (first bit, serial mode).	1	R/W
2	Measurement_Sel	Selects BER Measurement or Estimation. 0: Estimation 1: Measurement When Measurement is selected, the RS_DISABLE bit must also be set to enable BER measurement to be made.	0	R/W
1	Tri_State_Outputs	Tri-states transport stream outputs (serial and parallel). 0: Outputs driven 1: Outputs tri-state	1	R/W
0	RS_Disable	Enables/Disables RS decoder. 0: Enables error correction 1: Passes data without correction	0	R/W

BB_PARAMS		Read/Write		RESET: 0xF0
Offset Address: 0x81				fec_param reset
Bit	Name	Description	Default	R/W
7	Tsvalid_Active_High	Determines the sense of TSVALID. 0: Active low 1: Active high	1	R/W
6	Tssync_Active_High	Determines the sense of TSSYNC. 0: Active low 1: Active high	1	R/W
5	Tserr_Active_High	Determines the sense of TSERR. 0: Active low 1: Active high	1	R/W
4	Latch_on_posedge	Selects whether TSDATA should be sampled on the positive or negative edge of TSCLK. 0: Negative edge 1: Positive edge	1	R/W
3	Tsclk_204	Determines the behavior of TSCLK in gated mode (when Tsclk_full is RESET). 0: TSCLK is active for only the first 188 bytes in the TS packet. 1: TSCLK is active for all 204 bytes in the TS packet.	0	R/W
2	Tssync_byte	Determines the behavior of the TSSYNC output in both parallel and serial mode. 0: Active only for the first bit in the sync byte (use only in serial mode) 1: Active for the entire sync byte (recommended for parallel or serial modes)	0	R/W
1	Tserr_full	Determines whether TSERR is valid for 204 bytes of the TS packet or for 188 bytes. Used only when bit 2 is not set. 0: 188 bytes 1: 204 bytes	0	R/W
0	Tsclk_full	Determines whether TSCLK is active continuously or is only active for valid data. 0: Gated 1: Continuous	0	R/W

Note) It may be necessary to set bit 2 for compatibility with standard MPEG-2 decoders.

BER_PERIOD		Read/Write		RESET: 0x04
Offset Address: 0x83				
Bit	Name	Description	Default	R/W
7:6	Reserved		00	R/W
5	Berest_test_mode	Used to configure BEREST block for test. 0: Normal mode 1: Test mode	0	R/W
4:0	Ber_Est_Period[4:0]	Bit error rate estimation/measurement period. Min. 0x01, Max. 0x15 Estim./measurement period = $2^{BER\_EST\_PERIOD} \times$ 204-byte packets	00100	R/W

FEC_STATUS Read Only Offset Address: 0x84				
Bit	Name	Description	Default	R/W
7	Ber_ses	1: When a severely errored second is detected, i.e. when n or more 204-byte packets are uncorrectable in a second. n is defined by the LT_QLTY_THRESHOLD register.	—	R
6	Ber_es	1: When 1 or more 204-byte packets are uncorrectable in a second. (Note: An uncorrectable error occurs when more than 8 error bytes are present in a single packet.)	—	R
5	Lck_Flag	1: When FEC locked. When n SYNC bytes have been detected (n is programmable and defined by the SET_SYNC_DETECT register).	—	R
4	Ts_Llck_Flag	1: When transport stream lock lost condition detected. This occurs when n SYNC bytes go undetected (n is programmable and defined by the SET_SYNC_DETECT register).	—	R
3	Ts_Synch_Lock	1: When transport stream lock condition detected. Valid MPEG2 data is generated by the device from this time.	—	R
2	Vtb_Sync	1: When viterbi synchronization condition detected. Viterbi synchronization operation controlled by VIT_SN and VIT_ST registers.	—	R
1	New_Ber_es	1: When new bit error rate value is available. This bit is cleared by a register read operation.	—	R
0	Reserved		—	R

SET_SYNC_DETECT Read/Write RESET: 0xD6 Offset Address: 0x86				
Bit	Name	Description	Default	R/W
7	Synch_Cntr_Mode	Controls whether the pre-RS decoder sync detect count is decremented or reset when a missing sync byte is detected while locking. 0: Reset 1: Decrement	1	R/W
6	Ts_Synch_Cntr_Mode	Controls whether the post-RS decoder sync detect count is decremented or reset when a missing sync byte is detected. 0: Reset 1: Decrement	1	R/W
5:3	Sync_Loss_Lddr_Length[2:0]	Sync byte counter threshold at which lock is lost (post-RS decoder only).	010	
2:0	Synch_Lddr_Lngth[2:0]	Sync byte counter threshold at which lock is achieved (pre- and post-RS decoder).	110	R/W

LT_QLTY_THRESHOLD	Read/Write	RESET: 0x04
Offset Address: 0x87		

Bit	Name	Description	Default	R/W
7:0	LT_QLTY_THRESHOLD[7:0]	Long term quality threshold. Used for detecting severely errored second flag.	04h	R/W

BER_ESTIMATE_0	Read Only
Offset Address: 0x88	

Bit	Name	Description	Default	R/W
7	BERCNT	Bits 7:0 of measured/estimated BER	—	R

BER_ESTIMATE_1	Read Only
Offset Address: 0x89	

Bit	Name	Description	Default	R/W
7	BERCNT	Bits 15:8 of measured/estimated BER	—	R

BER_ESTIMATE_2	Read Only
Offset Address: 0x8A	

Bit	Name	Description	Default	R/W
7	New_Estimate	Set at the end of the BER measurement period. This bit is reset by performing a read operation to the BER_ESTIMATE_2 register.	—	R
6:5	Reserved		—	R
4	BERCNT_overflow	1: Indicates that the internal bit error counter has overflowed.	—	R
3:0	BERCNT	Bits 19:16 of measured/estimated BER	—	R

CWRJCT_CNT_0	Read Only
Offset Address: 0x8B	

Bit	Name	Description	Default	R/W
7:0	CWRJCT_CNT	Bits 7:0 of number of rejected codewords (MPEG2 packets) in a second	—	R

CWRJCT_CNT_1	Read Only
Offset Address: 0x8C	

Bit	Name	Description	Default	R/W
7:0	CWRJCT_CNT	Bits 15:8 of number of rejected codewords (MPEG2 packets) in a second	—	R

VIT_CTRL		Read/Write		RESET: 0x11
Offset Address: 0x90				
Bit	Name	Description	Default	R/W
7	Rate_Sel	Selects puncturing rate from the register or from TPS data. 0: TPS data 1: Register value	0	R/W
6:4	Rate[2:0]	Sets the puncturing rate. 000: 1/2 001: 2/3 010: 3/4 011: 5/6 100: 7/8 101 to 111: Auto	001	R/W
3	Reserved		0	R/W
2:0	Bert[2:0]	Defines sampling period in I/Q samples for bit error rate in the Viterbi decoder. 000: 2^8 001: 2^{13} 010: 2^{14} 011: 2^{15} 100: 2^{16} 101: 2^{17} 110: 2^{18} 111: 2^{19}	001	R/W

Note) It is recommended that the value of VIT_CTRL bit 7 should be “0”.

VIT_SN		Read/Write		RESET: 0x1F
Offset Address: 0x91				
Bit	Name	Description	Default	R/W
7:5	Reserved		000	R/W
4:0	SN[9:5]	Sets threshold for estimation of Viterbi synchronization. Threshold = SN × 32 (Min. 32, Max. 992)	11111	R/W

VIT_ST		Read/Write		RESET: 0x00
Offset Address: 0x92				
Bit	Name	Description	Default	R/W
7:4	Reserved		0000	R/W
3:0	ST[12:9]	Sets the sampling period for Viterbi synchronization Sampling period = ST × 512 (Min. 512, Max. 6656)	0000	R/W

VIT_BER_1		Read Only		
Offset Address: 0x93				
Bit	Name	Description	Default	R/W
7:0	VBER	Bits 7:0 of Viterbi bit error count	—	R

VIT_BER_2		Read Only		
Offset Address: 0x94				
Bit	Name	Description	Default	R/W
7:0	VBER	Bits 15:8 of Viterbi bit error count	—	R

Miscellaneous Registers

CHIP_INFO	Read Only	RESET: 0x61
Offset Address: 0xA0		

Bit	Name	Description	Default	R/W
7:2	CHIP Ident	Chip identification number	011000	R
1:0	Version	Chip version number	01	R

Note) This register cannot be read back until the PLL has been enabled.

RST_REG	Read/Write	RESET: 0x04
Offset Address: 0xA2		

Bit	Name	Description	Default	R/W
7	adc_rst	ADC reset enable. 1: Enable ADC reset when cold reset is active.	0	R/W
6	cofdm_rst	COFDM demodulator core reset enable. 1: Enable COFDM demodulator reset when warm or cold reset is active.	0	R/W
5	Vit_rst	Viterbi reset enable. 1: Enable Viterbi reset when warm or cold reset is active or when the auto recovery mode is selected.	0	R/W
4	fec_rst	FEC (excluding Viterbi) reset. 1: Enable FEC (excluding Viterbi) reset when warm or cold reset is active or when the auto recovery mode is selected.	0	R/W
3	Reserved		0	R/W
2	Hard	Set when RESETN pin of device is driven active. 0: Release after power-on reset (after PLL is stable) 1: No effect	1	R/W
1	Cold	Cold reset. 1: Reset	0	R/W
0	Warm	Warm reset. 1: Reset	0	R/W

Note) Software must wait 500μs for the PLL to stabilize before setting RST_REG bit 2.

INTERRUPT_SOURCE	Read/Write	RESET: 0x00
Offset Address: 0xA3		

Bit	Name	Description	Default	R/W
7	Ts_if_int	1: TS smoothing buffer overflow or underflow detected.	0	R/W
6	Cofdm_Int	1: COFDM demodulator core Interrupt.	0	R/W
5	Ts_synch_Lock	1: Transport stream locked.	0	R/W
4	Ts_Llck_Flag	1: Transport stream lock lost.	0	R/W
3	Reserved		0	R/W
2	Ber_Es	1: Errored second detected.	0	R/W
1	Ber_Ses	1: Severely errored second detected.	0	R/W
0	Rs_cwrjct_Flag	1: More than 8 error bytes in current packet.	0	R/W

Note) Each bit may be cleared by writing a “1” to the appropriate bit location.

INTERRUPT_MASK		Read/Write		RESET: 0x00
Offset Address: 0xA4				
Bit	Name	Description	Default	R/W
7	Ts_if_int_En	1: Enable TS interface interrupts.	0	R/W
6	Cofdm_Int_En	1: Enable COFDM demodulator core interrupts.	0	R/W
5	Ts_synch_Lock_En	1: Enable TS lock interrupt.	0	R/W
4	Ts_Llck_Flag_En	1: Enable TS lost lock interrupt.	0	R/W
3	Reserved		0	R/W
2	Ber_Es_En	1: Enable second error interrupt.	0	R/W
1	Ber_Ses_En	1: Enable second severity error interrupt.	0	R/W
0	Rs_cwrjct_Flag_En	1: Enable codeword reject interrupt.	0	R/W

TIMEOUT_VAL		Read/Write		RESET: 0xFF
Offset Address: 0xA6				
Bit	Name	Description	Default	R/W
7:0	TIMEOUT_VAL[7:0]	Sets the time after which the CXD1968AR will timeout an I^2C access when waiting for an I^2C master response. The timeout period can be set to between approximately 2 and 500ms represented by 00h and FFh in this register.	FFh	R/W

PLL_FODR		Read/Write		RESET: 0x62
Offset Address: 0xA7				
Bit	Name	Description	Default	R/W
7	Reserved		0	R/W
6:5	OD[1:0]	00: Not allowed 01: 1 10: 2 11: 4	PLL output divider. Default value for OD[1:0] is 03h. Yielding a value of 4 for NO.	11	R/W
4:0	R[4:0]	PLL input divider. Controls comparison frequency F_{REF}. $F_{REF} = F_{IN} / NR$ – Valid range is 2MHz to 8MHz. $NR = 16 \times R4 + 8 \times R3 + 4 \times R2 + 2 \times R1 + R0$ Default value for R[4:0] is 0x02. Yielding a value of 2 for NR.		00010	R/W

Note) PLL output frequency $F_{OUT} = (F_{IN} \times NF / (NR \times NO)$
Where F_{IN} is the frequency of the clock signal present on the XTALI pin.

PLL_F	Read/Write	RESET: 0x52
Offset Address: 0xA8		

Bit	Name	Description	Default	R/W
7:0	F[7:0]	PLL feedback divider bits 7 to 0. $F_{VCO} = F_{REF} \times NF$ – Valid range is 200MHz to 400MHz. $NF = 2 \times (128 \times F7 + 64 \times F6 + 32 \times F5 + 16 \times F4 + 8 \times F3 + 4 \times F2 + 2 \times F1 + F0)$ Default value for F[7:0] is 0x52. Yielding a value of 164 for NF.	52h	R/W

The above register defaults are for 4MHz crystal operation.

The table below shows the suggested PLL settings when using other crystal frequencies.

Xtal Freq [MHz]	OD[1:0]	R[4:0]	F[7:0]	PLL_FODR	PLL_F
4.00	3	2	82 decimal	0x62	0x52
8.00	3	4	82 decimal	0x64	0x52
16.00	3	8	82 decimal	0x68	0x52
20.48	3	10 decimal	80 decimal	0x6A	0x50

PLL_CONTROL	Read/Write	RESET: 0x40
Offset Address: 0xA9		

Bit	Name	Description	Default	R/W
7	Reserved		0	R/W
6	PLL_power_down	1: Power down the PLL.	1	R/W
5	PLL_op_enable	1: Enable the PLL output clocks.	0	R/W
4	PLL_bypass	1: Bypass the PLL generated clock and use external clock source.	0	R/W
3	ext_clk_enable	1: Enables the external fast clock (instead of the PLL).	0	R/W
2	PLL_op_invert	1: Inverts the PLL output clocks.	0	R/W
1	PLL_test_mode	1: Puts the PLL in test mode.	0	R/W
0	clock_disable	1: Disables most of the clocks (for low noise ADC evaluation).	0	R/W

TUNER_CTRL5	Read/Write	RESET: 0x00
Offset Address: 0xAF		

Bit	Name	Description	Default	R/W
7	enable_quiet_I2C	0: Tuner Quiet I^2C bus disabled. 1: Tuner Quiet I^2C bus enabled.	0	
6	Reserved		0	
5	Reserved		0	
4	Reserved	NB: Do not set to “1”.	0	
3:2	Reserved		00	R/W
1	Reserved	NB: Do not set to “1”.	0	R/W
0	Reserved	NB: Do not set to “1”.	0	R/W

AUTO_RESET		Read/Write		RESET: 0x01
Offset Address: 0xB1				
Bit	Name	Description	Default	R/W
7:1	Reserved		00h	R/W
0	Disable	1: Disable auto reset of the FEC on code rate change.	1	R/W

RF_IFAGC_CTRL0		Read/Write		RESET: 0x11
Offset Address: 0xB2				
Bit	Name	Description	Default	R/W
7:6	RF_IFAGCQ_PWM	RF_AGC_PWM bits 1:0	00	R/W
5	Reserved		0	R/W
4	IF_AGC_EN	0: IF_AGC is tri-state. 1: IF_AGC is driven.	1	R/W
3:2	RF_IFAGCQ_MODE	00: Tri-state mode – RF_IFAGC_Q is a GPI pin. 01: Manual PWM mode for RF_IFAGC_Q output 10: GPO mode for RF_IFAGC_Q output set by bit 1 this reg 11: ZIF mode: Automatic PWM mode for Q channel AGC o/p	00	
1	RF_IFAGCQ_GPO	0: RF_IFAGC_Q output 0 when GPO mode selected 1: RF_IFAGC_Q output 1 when GPO mode selected	0	R/W
0	RF_IFAGCQ_GPI	Senses state of RF_IFAGC_Q input pin level. 0: RF_IFAGC_Q input at logic 0 1: RF_IFAGC_Q input at logic 1	1	R

RF_IFAGCQ_CTRL1		Read/Write		RESET: 0x00
Offset Address: 0xB3				
Bit	Name	Description	Default	R/W
7:0	RF_IFAGCQ_PWM	RF_AGC_PWM bits 9:2	00h	R/W

Note) 1. In the time interval between host writes to RF_IFAGCQ_CTRL0 and RF_IFAGCQ_CTRL1, the manual control to the AGC will have an intermediate value.

2. The ability to use the RFAGC output as a PWM output or a GPIO has been added to the CXD1968AR compared to the CXD1973Q. RF_AGC_CTRL0[2:1] that were previously reserved bits are now used for this purpose.

3. RF_IFAGCQ_PWM is a straight binary value.

SMOOTH_CTRL	Read/Write	RESET: 0x04
Offset Address: 0xB4		

Bit	Name	Description		Default	R/W
7:6	CHANNEL_WIDTH	00: 8MHz channel 01: 7MHz channel 10: 6MHz channel 11: Reserved	Channel width	00	R/W
5:3	Reserved			000	R/W
2	RESET	0: Smoothing circuit not in its reset state 1: Smoothing circuit is held in its reset state		1	R/W
1	DATA_PERIOD_AUTO	0: Data period value can be updated manually (via I^2C) or left at its default setting. 1: Update data period value automatically from received TPS information.		0	R/W
0	ENABLE	0: Disable smoothing circuit. When disabled, the input to the smoothing circuit is routed to the output without going through the smoothing FIFO. 1: Enable smoothing circuit.		0	R/W

SMOOTH_STAT	Read/Write	RESET: 0x00
Offset Address: 0xB5		

Bit	Name	Description	Default	R/W
7:2	Reserved		00h	R/W
1	UNDERFLOW	1: An underflow condition has been detected. An underflow condition is where data is requested but cannot be provided because the read FIFO is empty. Note that when data is requested but not provided because the next TS word is a sync-byte and the FIFO does not contain a complete TS packet, this condition is part of the smoothing blocks normal operation and is not classed as an underflow condition. Write a “1” to this location to clear this bit.	0	R/W
0	OVERFLOW	1: An overflow condition has been detected. Write a “1” to this location to clear this bit.	0	R/W

SMOOTH_DELAY	Read/Write	RESET: 0x14
Offset Address: 0xB6		

Bit	Name	Description	Default	Bit
7:0	DELAY	The value in this register represents the data path delay in transport stream packets between the COFDM core and the data smoothing block. This information is used by the smoothing circuit to determine the delay between TPS bit changes and the associated modification to the transport stream output data rate.	14h	R/W

SMOOTH_DP0		Read/Write		RESET: 0x80
Offset Address: 0xB7				
Bit	Name	Description	Default	R/W
7:0	DATA_PERIOD[7:0]	This part of the data period value represents the fractional number of clock periods per TS word. A read from the SMOOTH_DP0 register returns the current value of the fractional part of the data period value. A read from SMOOTH_DP0 also causes the current value of the integer part of the data period value to be stored in a holding register, which can be accessed by reading from SMOOTH_DP1. Writing to SMOOTH_DP0 only has an effect when the DATA_PERIOD_AUTO bit of the SMOOTH_CTRL register is set to “0”. In this case, writing to SMOOTH_DP0 has the effect of storing the 8-bit value in a holding register. Writing to SMOOTH_DP1 then has the effect of transferring data from the holding register to the SMOOTH_DP0 register proper. For these reasons SMOOTH_DP0 and SMOOTH_DP1 should be read from or written to in order, SMOOTH_DP0 first.	80h	R/W

SMOOTH_DP1		Read/Write		RESET: 0x09
Offset Address: 0xB8				
Bit	Name	Description	Default	R/W
7:0	DATA_PERIOD[15:8]	This part of the data period value represents the integer number of clock periods per TS word. A read from the SMOOTH_DP1 register returns the integer part of the data period value previously stored in a holding register when a read from the SMOOTH_DP0 register occurred (see SMOOTH_DP0 above). Writing to SMOOTH_DP1 only has an effect when the DATA_PERIOD_AUTO bit of the SMOOTH_CTRL register is set to “0”. In this case, writing to SMOOTH_DP1 has the expected effect of updating the SMOOTH_DP1 register value, and has the additional effect of transferring data from a holding register (updated during a SMOOTH_DP0 write operation) into the SMOOTH_DP0 register (see SMOOTH_DP0 above).	09h	R/W

ADC_CONTROL Read/Write RESET: 0xA2 Offset Address: 0xB9				
Bit	Name	Description	Default	R/W
7	REFPD_Q	Set to “1” to power down reference in Q channel ADC.	1	R/W
6	STDBY_Q	Set to “1” to put the Q channel ADC in standby mode.	0	R/W
5	RESET_Q	Q channel ADC is reset by writing a “0” or “1” sequence to this bit.	1	R/W
4	PWRDN_Q	Set to “1” to power down the Q channel ADC.	0	R/W
3	REFPD_I	Set to “1” to power down reference in I channel ADC.	0	R/W
2	STDBY_I	Set to “1” to put the ADC_I in standby mode.	0	R/W
1	RESET_I	I channel ADC is reset by writing a “0” or “1” sequence to this bit.	1	R/W
0	PWRDN_I	Set to “1” to power down the I channel ADC.	0	R/W

Note) 1. Both ADCs are reset on power-up.
2. Before powering-down an ADC, ensure its respective reference is first powered-down.

ADC_CONTROL2 Read/Write RESET: 0x47 Offset Address: 0xBA				
Bit	Name	Description	Default	R/W
7:6	REFSEL[1:0]	Selects reference voltage on ADC_I and ADC_Q. 00: refout = 0.35V → 0.7V full scale diff p-p input 01: refout = 0.50V → 1.0V full scale diff p-p input 10: refout = 0.75V → 1.5V full scale diff p-p input 11: refout = 1.00V → 2.0V full scale diff p-p input	01	R/W
5	Ext_A/D_Select	External A/D select. 0: Internal A/D selected 1: External A/D selected	0	R/W
4	ADC_Offset_2s_Comp	Selects internal ADC output type. 0: Offset binary: default for the CXD1968AR 1: 2’s complement	0	R/W
3	ADC_test_mode	Used for testing ADC. 0: Normal mode 1: Test mode	0	R/W
2	DCCEN	Enables ADC clock duty cycle correction.	1	R/W
1	CLKRCVEN	Sets pk-pk level of ADC sampling clock on ADC_I and ADC_Q. 0: 3.3V CMOS input level 1: 1.2V CMOS input level	1	R/W
0	ADC_DIRECT_CLKEN	Enables driving of the ADC clock directly from XTALI input. 0: Normal mode (ADC clocked from PLL) 1: Direct clock mode	1	

Note) When using external A/D, the direct clock mode must be used.

RAM_CONTROL		Read/Write		RESET: 0x00
Offset Address: 0xBC				
Bit	Name	Description	Default	R/W
7:1	Reserved		00h	R/W
0	RAM_ STANDBY	Set to put all RAMs in standby mode. Used for low-power standby mode.	0	R/W

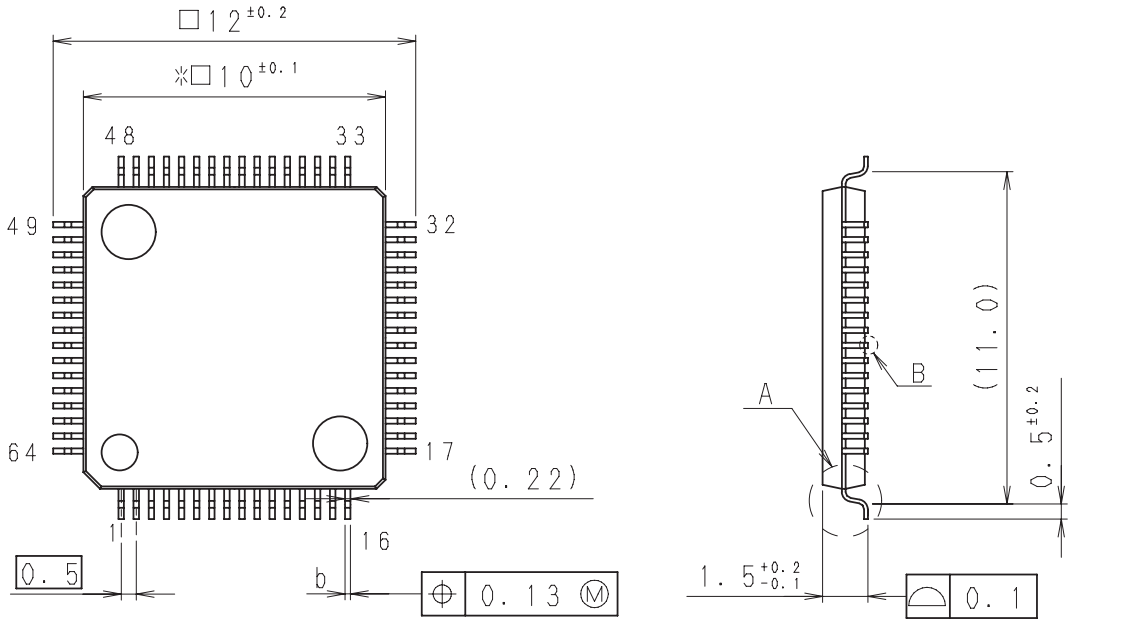
ADC_CONTROL3		Read/Write		RESET: 0xFF
Offset Address: 0xBD				
Bit	Name	Description	Default	R/W
7	RINTEN_Q	Enables internal bias current resistor for ADC_Q	1	R/W
6:4	RINTSEL_Q[2:0]	Selects value of internal bias current resistor if RINTEN_Q = 1. This can be used to optimize power consumption of ADC_Q according to max. sampling rate used. 000: 18k 001: 22k 010: 27.9k 011: 37.7k 100: 57.4 k 101: 77.1 k 110: 116.5k 111: 234.5k	111	R/W
3	RINTEN_I	Enables internal bias current resistor for ADC_I.	1	R/W
2:0	RINTSEL_I[2:0]	Selects value of internal bias current resistor if RINTEN_I = 1. This can be used to optimize power consumption of ADC_I according to max. sampling rate used. 000: 18k 001: 22k 010: 27.9k 011: 37.7k 100: 57.4 k 101: 77.1 k 110: 116.5k 111: 234.5k	111	R/W

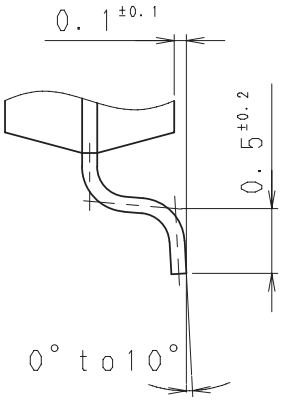
ADC_STATUS		Read Only		
Offset Address: 0xBE		This register is cleared on a Write access		
Bit	Name	Description	Default	R/W
7	OVF_Q	Indicates overflow condition on ADC_Q input. 0: No overflow 1: Overflow of input		R
6	UDF_Q	Indicates underflow condition on ADC_Q input. 0: No underflow 1: Underflow of input		R
5	OVF_I	Indicates overflow condition on ADC_I input. 0: No overflow 1: Overflow of input		R
4	UDF_I	Indicates underflow condition on ADC_I input. 0: No underflow 1: Underflow of input		R
3:0	Reserved			

Package Outline

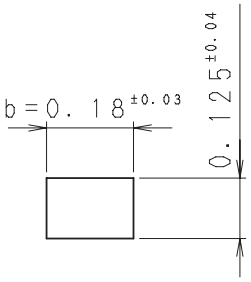
(Unit: mm)

64PIN LQFP (PLASTIC)





DETAIL A



DETAIL B:PALLADIUM

NOTE:Dimension"※"does not include mold protrusion.

SONY CODE	LQFP-64P-L01
JEITA CODE	P-LQFP64-10X10-0.5
JEDEC CODE	————

AP-4000-64003S3 Rev.1

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.3g