



Hex SPDT Data Switch

General Description

The MAX4947/MAX4948 analog switches operate from a single +1.8V to +5.5V supply. These switches feature a low 30pF (typ) capacitance for high-speed data switching applications.

The MAX4947 is a triple double-pole/double-throw (DPDT) switch, and the MAX4948 is a hex single-pole/double-throw (SPDT) switch with one control logic input. The MAX4947 has three logic inputs to control the switches in pairs. The MAX4948 has one logic input and an enable input ($\overline{EN}$) to disable the switches.

The MAX4947/MAX4948 are available in small 24-pin (4mm x 4mm) TQFN and 25-bump (2.5mm x 2.5mm) chip-scale packages (UCSP™).

Applications

USB Signal Switching Cell Phones
UART Signal Switching PDAs
SDIO/Memory Stick

UCSP is a trademark of Maxim Integrated Products, Inc.

Features

- ◆ Multiplex SDIO or Memory Stick Interfaces
- ◆ 1.8V to 5.5V Supply Voltage Range
- ◆ Low On-Resistance 4Ω (typ)
- ◆ Low-Capacitance Switches, 30pF (typ)
- ◆ Rail-to-Rail Signal Handling
- ◆ Small 25-Bump UCSP™ (2.5mm x 2.5mm) and 24-TQFN (4mm x 4mm)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX4947EBA+*	-40°C to +85°C	25 UCSP-25	B25-1
MAX4947ETG+	-40°C to +85°C	24 TQFN-EP	T2444-4
MAX4948EBA+*	-40°C to +85°C	25 UCSP-25	B25-1
MAX4948ETG+	-40°C to +85°C	24 TQFN-EP	T2444-4

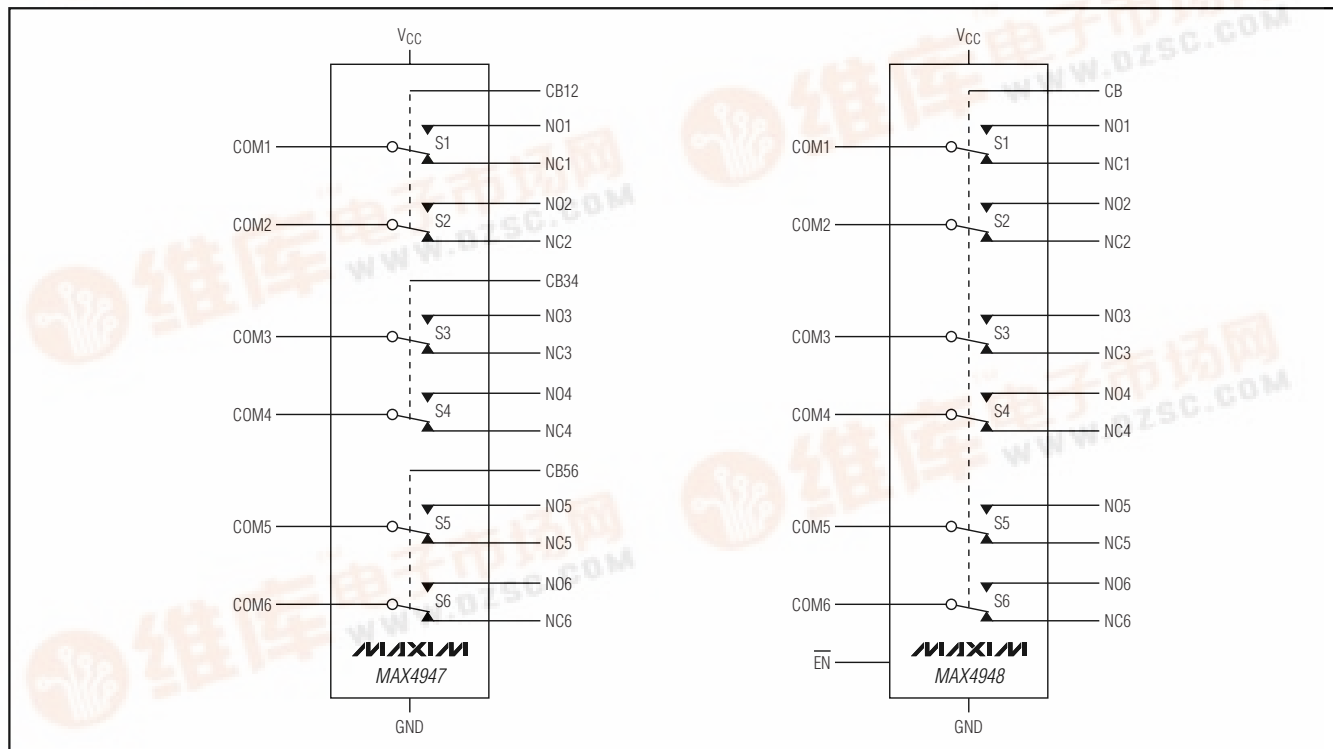
* Future product—contact factory for availability.

+ Denotes lead-free package.

EP = Exposed paddle.

Typical Operating Circuit appears at end of data sheet.

Functional Diagram



Hex SPDT Data Switch

ABSOLUTE MAXIMUM RATINGS

VCC to GND-0.3V to +6.0V
 All other pins to GND (Note 1)-0.3V to VCC + 0.3V
 Continuous Current
 NO_, NC_, COM_±100mA
 Peak Current NO_, NC_, COM_
 (pulsed at 1ms, 50% Duty Cycle).....±200mA
 (pulsed at 1ms, 10% Duty Cycle).....±300mA
 Continuous Power Dissipation (TA = +70°C)
 25-Bump UCSP (derate 12.2mW/°C above +70°C)976mW
 24-Pin TQFN (derate 20.8mW/°C above +70°C)1667mW

Operating Temperature Range-40°C to +85°C
 Junction Temperature150°C
 Storage Temperature Range-65°C to +150°C
 Bump Temperature (soldering)
 Infrared (15s)+220°C
 Vapor Phase (60s)+215°C
 Lead Temperature (soldering)+300°C

Note 1: Signals on CB_, NO_, NC_, COM_, $\overline{\text{EN}}$ exceeding VCC or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VCC = +2.7V to +5.5V, TA = -40°C to +85°C, unless otherwise noted. Typical values are at VCC = +3V, TA = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
POWER SUPPLY							
Power-Supply Range	V _{CC}		T _{MIN} to T _{MAX}	1.8		5.5	V
Power-Supply Current	I _{CC}	V _{CC} = 5.5V, V _{CB_} = 0V or V _{CC}	T _{MIN} to T _{MAX}			1.0	μA
		V _{CC} = 2.7V, V _{CB_} = 1.6V or 0.5V			5		
		V _{CC} = 5.5V, V _{CB_} = 1.6V or 0.5V			10		
ANALOG SWITCH							
Analog Signal Range	V _{NO_} , V _{NC_} , V _{COM_}		T _{MIN} to T _{MAX}	0		V _{CC}	V
On-Resistance (Note 4)	R _{ON}	V _{CC} = 2.7V, I _{COM_} = 10mA; V _{NC_} or V _{NO_} = 0 or V _{CC}	+25°C	4.0	5.5	Ω	
			T _{MIN} to T _{MAX}		6.5		
On-Resistance Match Between Channels (Notes 4, 5)	ΔR _{ON}	V _{CC} = 2.7V, I _{COM_} = 10mA; V _{NO_} or V _{NC_} = 0 or V _{CC}	+25°C	0.3	0.5	Ω	
			T _{MIN} to T _{MAX}		0.6		
On-Resistance Flatness (Notes 4, 6)	R _{FLAT}	V _{CC} = 2.7V, I _{COM_} = 10mA; V _{NC_} or V _{NO_} = 0 or V _{CC}	+25°C	0.5	1	Ω	
			T _{MIN} to T _{MAX}		1.2		
NO_ or NC_ Off-Leakage Current	I _{NO_(OFF)} or I _{NC_(OFF)}	V _{CC} = 3.6V; V _{COM_} = 3.6V, 0; V _{NO_} or V _{NC_} = 0, 3.6V	+25°C	-3	+3	nA	
			T _{MIN} to T _{MAX}	-10	+10		
COM_ On-Leakage Current	I _{NO_(ON)}	V _{CC} = 3.6V; V _{COM_} = 3.6V, 0; V _{NO_} or V _{NC_} = 3.6V, 0 or unconnected	+25°C	-6	+6	nA	
			T _{MIN} to T _{MAX}	-10	+10		

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MAX4947/MAX4948

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +2.7V$ to $+5.5V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $V_{CC} = +3V$, $T_A = +25^{\circ}C$.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
COM_ Off-Leakage Current	$I_{COM(OFF)}$	$V_{CC} = 3.6V$ (MAX4948); $V_{COM_} = 3.3V, 0.3V$; $V_{NO_}$ or $V_{NC_} = 0, 3V, 3.3V$	$+25^{\circ}C$ T_{MIN} to T_{MAX}	-6 -10		+6 +10	nA
DYNAMIC							
Turn-On Time	t_{ON}	$V_{CC} = 2.7V$; $V_{NO_}$ or $V_{NC_} = 1.5V$; $R_L = 50\Omega$; $C_L = 35pF$, Figure 1	$+25^{\circ}C$ T_{MIN} to T_{MAX}		400 800	800	ns
Turn-Off Time	t_{OFF}	$V_{CC} = 2.7V$; $V_{NO_}$ or $V_{NC_} = 1.5V$; $R_L = 50\Omega$; $C_L = 35pF$, Figure 1	$+25^{\circ}C$ T_{MIN} to T_{MAX}		300 800	800	ns
Break-Before-Make	t_{BBM}	$V_{CC} = 2.7V$; $V_{NO_}$ or $V_{NC_} = 1.5V$; $R_L = 50\Omega$; $C_L = 35pF$, Figure 2 (Note 7)	$+25^{\circ}C$ T_{MIN} to T_{MAX}		100 2		ns
HIGH-SPEED TIMING CHARACTERISTICS (rising time = 20ns)							
Skew	t_{SKEW}	$V_{CC} = 2.7V$; $R_S = 39\Omega$; $C_L = 50pF$, Figure 3	T_{MIN} to T_{MAX}		0.2		ns
Charge Injection	Q	$V_{GEN} = 0$, $R_{GEN} = 0$, $C_L = 1nF$, Figure 4	$+25^{\circ}C$		10		pC
-3dB Bandwidth	BW	Signal = 0dBm, $C_L = 5pF$, $R_L = 50\Omega$, Figure 5	$+25^{\circ}C$		300		MHz
Off-Isolation	V_{ISO}	$C_L = 5pF$; $R_L = 50\Omega$; $V_{COM_} = 1V_{P-P}$, $f = 1MHz$, Figure 5 (Note 8)	$+25^{\circ}C$		-70		dB
Crosstalk	V_{CT}	$C_L = 5pF$; $R_L = 50\Omega$; $f = 1MHz$, $V_{COM_} = 1V_{P-P}$, Figure 5 (Note 9)	$+25^{\circ}C$		-90		dB
NC_ or NO_ Off-Capacitance	$C_{NC(OFF)}$ $C_{NO(OFF)}$	$NC_ = NO_ = 0V$, $f = 1MHz$ Figure 6	$+25^{\circ}C$		15		pF
COM_ Off-Capacitance	$C_{COM(OFF)}$	$V_{COM} = GND$, $f = 1MHz$ (MAX4948), Figure 6	$+25^{\circ}C$		25		pF
COM_ On-Capacitance	$C_{COM(ON)}$	$COM_ = 0V$, $f = 1MHz$, Figure 6	$+25^{\circ}C$		30		pF
DIGITAL I/O ($\overline{EN}$, $CB_$)							
Input-Logic High	V_{IH}		T_{MIN} to T_{MAX}	1.6			V
Input-Logic Low	V_{IL}		T_{MIN} to T_{MAX}			0.5	V
Input Leakage Current	I_{CB}	$V_{CB_} = 0$ or V_{CC}	T_{MIN} to T_{MAX}			1	μA

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +2.7V$ to $+5.5V$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = +3V$, $T_A = +25^\circ C$.) (Notes 2, 3)

Note 2: The algebraic convention is used. The most negative value is shown in the minimum column.

Note 3: UCSP parts are 100% tested at $T_A = +25^\circ C$. Limits across the full temperature range are guaranteed by correlation and design. TQFN parts are guaranteed by correlation and design at $-40^\circ C$.

Note 4: R_{ON} and ΔR_{ON} matching specifications are guaranteed by design.

Note 5: $\Delta R_{ON} = R_{ON}(MAX) - R_{ON}(MIN)$.

Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

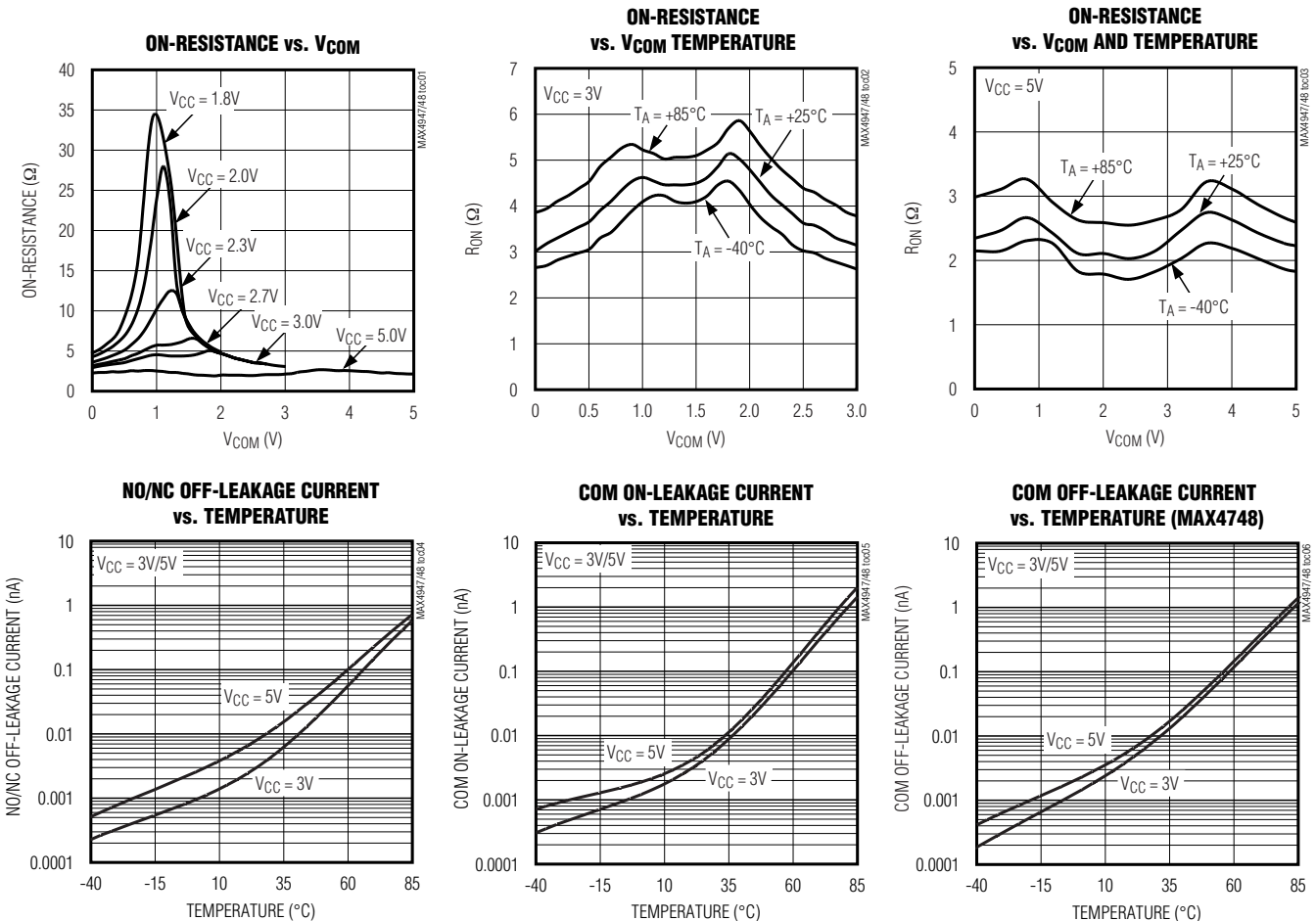
Note 7: Guaranteed by design, not production tested.

Note 8: Off-Isolation = $20\log_{10} [V_{COM_} / (V_{NO_} \text{ or } V_{NC_})]$, $V_{COM_}$ = output, $V_{NO_}$ or $V_{NC_}$ = input to off switch.

Note 9: Between any two switches.

Typical Operating Characteristics

($V_{CC} = 3V$, $T_A = +25^\circ C$, unless otherwise noted.)

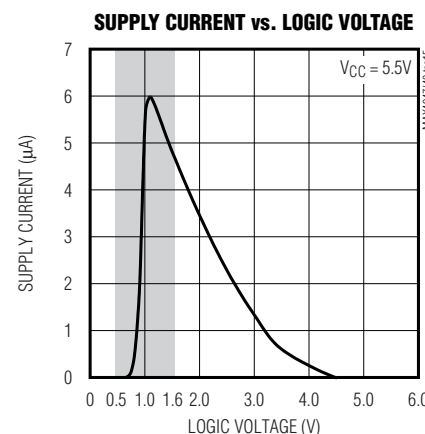
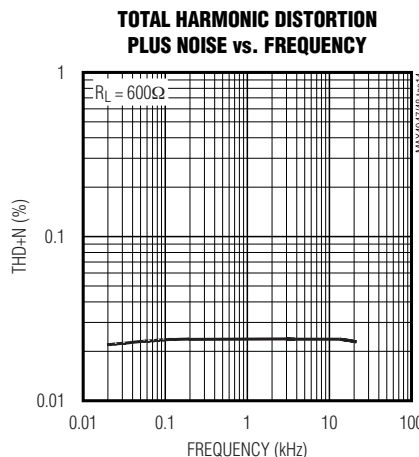
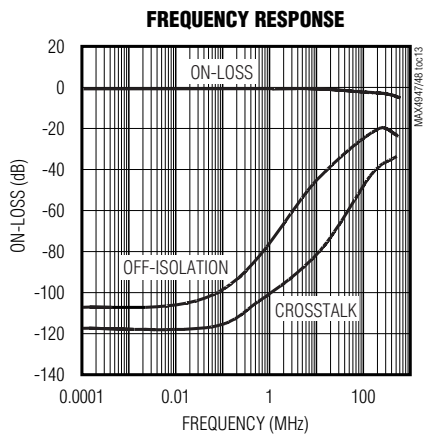
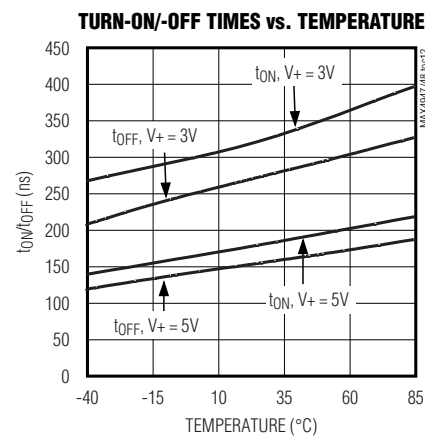
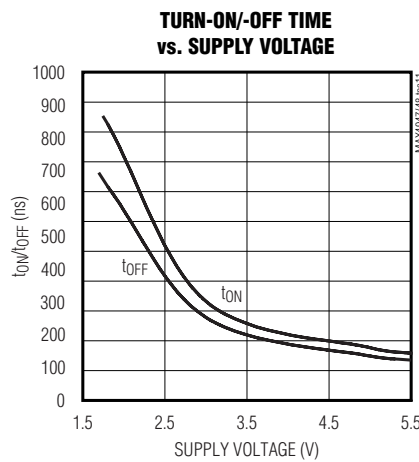
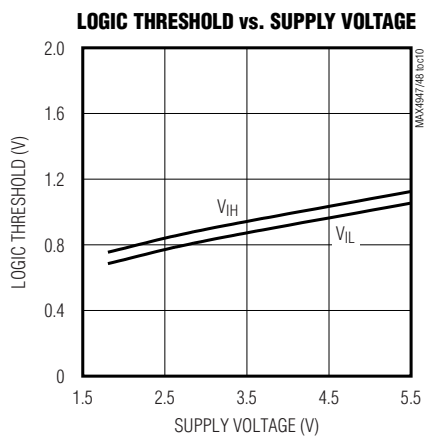
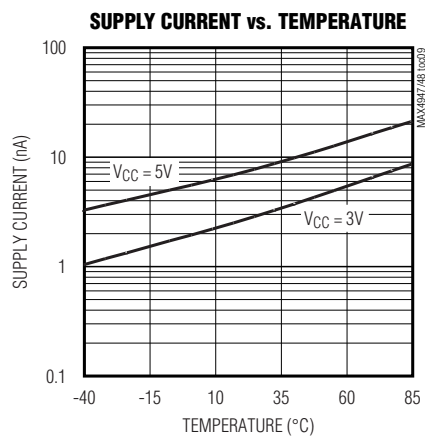
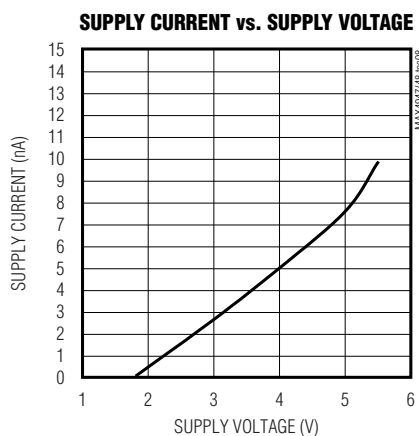
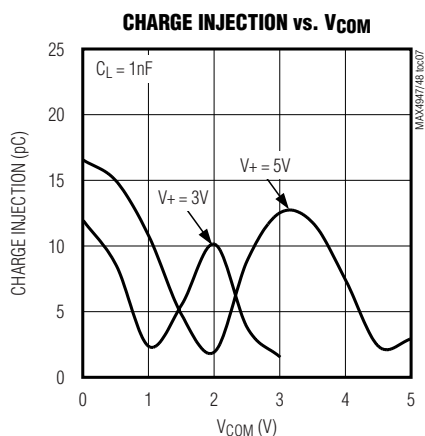


Hex SPDT Data Switch

Operating Characteristics (continued)

($V_{CC} = +3V$, $T_A = +25^\circ C$, unless otherwise noted.)

MAX4947/MAX4948



Hex SPDT Data Switch

MAX4947/MAX4948

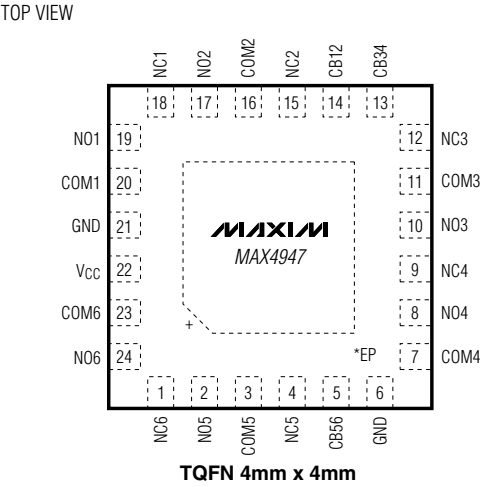
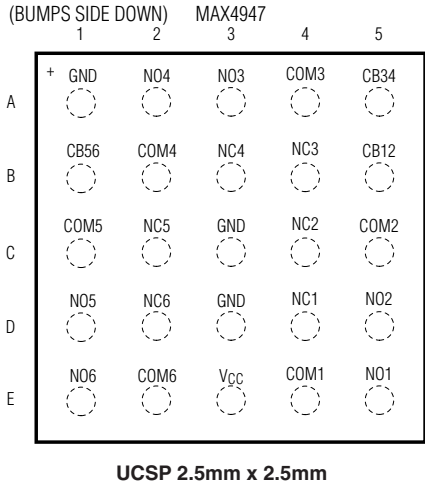
Pin Description

PIN				NAME	FUNCTION
MAX4947		MAX4948			
TQFN	UCSP	TQFN	UCSP		
1	D2	1	D2	NC6	Analog Switch 6. Normally Closed Terminal 6.
2	D1	2	D1	NO5	Analog Switch 5. Normally Open Terminal 5.
3	C1	3	C1	COM5	Analog Switch 5. Common Terminal 5.
4	C2	4	C2	NC5	Analog Switch 5. Normally Closed Terminal 5.
5	B1	—	—	CB56	Digital Control Input for Analog Switches 5 and 6
6, 21	A1, C3, D3	6, 21	A1, C3, D3	GND	Ground
7	B2	7	B2	COM4	Analog Switch 4. Common Terminal 4.
8	A2	8	A2	NO4	Analog Switch 4. Normally Open Terminal 4.
9	B3	9	B3	NC4	Analog Switch 4. Normally Closed Terminal 4.
10	A3	10	A3	NO3	Analog Switch 3. Normally Open Terminal 3.
11	A4	11	A4	COM3	Analog Switch 3. Common Terminal 3.
12	B4	12	B4	NC3	Analog Switch 3. Normally Closed Terminal 3.
13	A5	—	—	CB34	Digital Control Input for Analog Switches 3 and 4
14	B5	—	—	CB12	Digital Control Input for Analog Switches 1 and 2
15	C4	15	C4	NC2	Analog Switch 2. Normally Closed Terminal 2.
16	C5	16	C5	COM2	Analog Switch 2. Common Terminal 2.
17	D5	17	D5	NO2	Analog Switch 2. Normally Open Terminal 2.
18	D4	18	D4	NC1	Analog Switch 1. Normally Closed Terminal 1.
19	E5	19	E5	NO1	Analog Switch 1. Normally Open Terminal 1.
20	E4	20	E4	COM1	Analog Switch 1. Common Terminal 2.
22	E3	22	E3	VCC	Positive Supply Voltage
23	E2	23	E2	COM6	Analog Switch 6. Common Terminal 6.
24	E1	24	E1	NO6	Analog Switch 6. Normally Open Terminal 6.
—	—	5	B1	$\overline{\text{EN}}$	Enable-Logic In. Drive $\overline{\text{EN}}$ high to set all switches into high-impedance mode.
—	—	13	A5	N.C.	No Connection. Leave N.C. unconnected.
—	—	14	B5	CB	Digital Control Input for Analog Switches 1–6. Drive CB low to connect COM_ to NC_ for all six switches. Drive CB high to connect COM_ to NO_ for all six switches. CB is valid only when $\overline{\text{EN}}$ is driven low. If $\overline{\text{EN}}$ is driven high then all switches are high impedance.
EP	—	EP	—	EP	Exposed Pad. Connect exposed pad to ground.

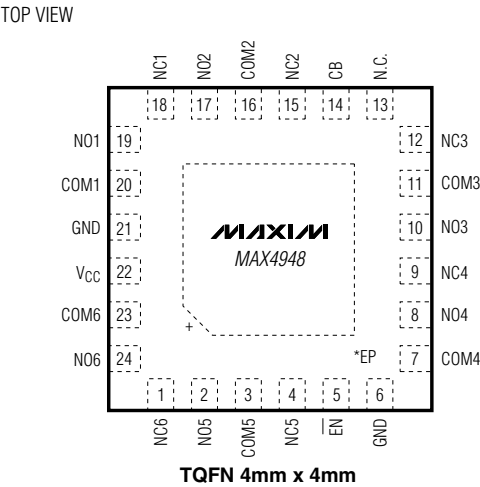
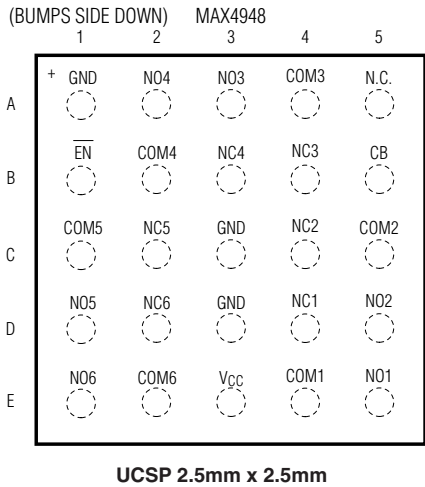
Hex SPDT Data Switch

Pin Configurations/Truth Tables

MAX4947/MAX4948



*EXPOSED PADDLE CONNECT TO GROUND



*EXPOSED PADDLE-CONNECT TO GROUND

MAX4947		
CB12	NO1/NO2	NC1/NC2
0	OFF	ON
1	ON	OFF
CB34	NO3/NO4	NC3/NC4
0	OFF	ON
1	ON	OFF
CB56	NO5/NO6	NC5/NC6
0	OFF	ON
1	ON	OFF

MAX4948			
$\overline{\text{EN}}$	CB	NO	NC
LOW	LOW	OFF	ON
LOW	HIGH	ON	OFF
HIGH	X	OFF	OFF

Hex SPDT Data Switch

Detailed Description

The MAX4947 triple DPDT and the MAX4948 hex SPDT analog switches operate from a single +1.8V to +5.5V supply. These devices are fully specified for +3V applications.

The MAX4947/MAX4948 have a guaranteed 4Ω (typ) on-resistance and a low 30pF (typ) capacitance that makes the switch ideal for data switching applications. The MAX4947 has three logic inputs to control two switches in pairs and the MAX4948 has one logic control input and an enable input ($\overline{EN}$) to disable the switches.

Applications Information

Digital Control Inputs

The MAX4947/MAX4948 provide a digital control logic input, CB_{-} . CB_{-} controls the position of the switches as shown in the *Pin Configurations/Truth Tables*. Driving CB_{-} rail-to-rail minimizes power consumption.

The MAX4948 features an $\overline{EN}$ input to turn all switches on or off. When $\overline{EN}$ is driven high, CB is disabled, and the analog inputs enter a high-impedance state. Drive $\overline{EN}$ low to turn the switches on and enable CB .

Analog Signal Levels

The on-resistance of the MAX4947/MAX4948 is very low and stable as the analog input signals are swept from ground to V_{CC} (see the *Typical Operating Characteristics*). These switches are bidirectional, allowing NO_{-} , NC_{-} , and COM_{-} to be configured as either inputs or outputs.

Power-Supply Biasing

Power-supply bypassing improves noise margin and prevents switching noise to propagate from V_{CC} supply to other components. A $0.1\mu F$ capacitor connected from V_{+} to GND is adequate for most applications.

Power-Supply Sequencing

CMOS devices require proper power-supply sequencing. Always apply V_{CC} before the analog signals, especially if the input signal is not current limited.

UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, printed circuit board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, go to the Maxim website at www.maxim-ic.com/ucsp for the Application Note: *UCSP-A Wafer-Level Chip-Scale Package*.

Timing Circuits/Timing Diagrams

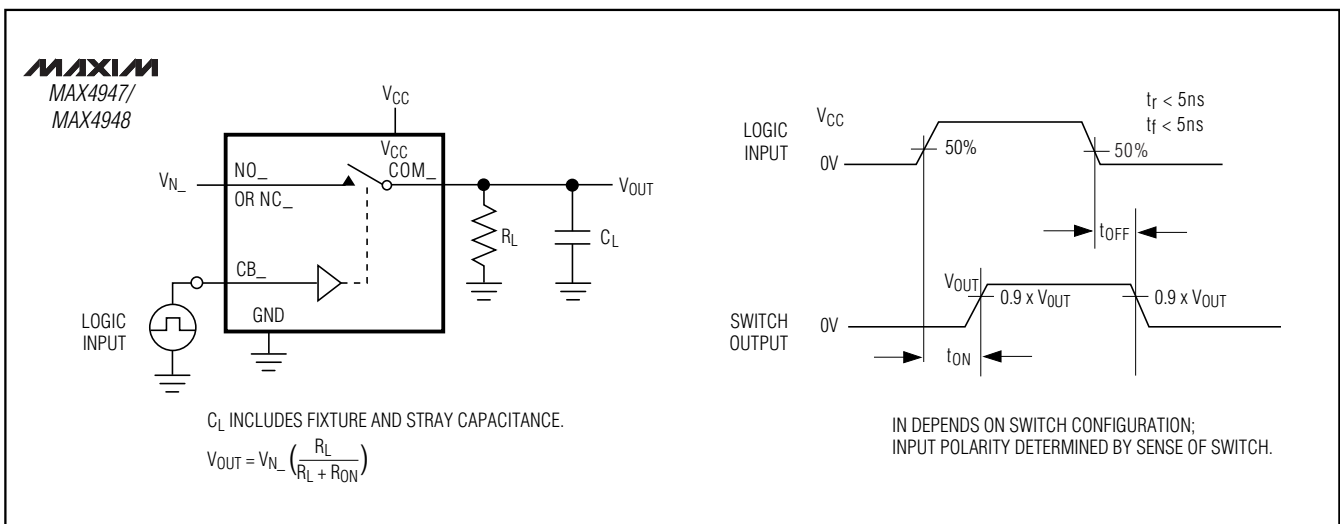


Figure 1. Switching Time

Hex SPDT Data Switch

MAX4947/MAX4948

Timing Circuits/Timing Diagrams (continued)

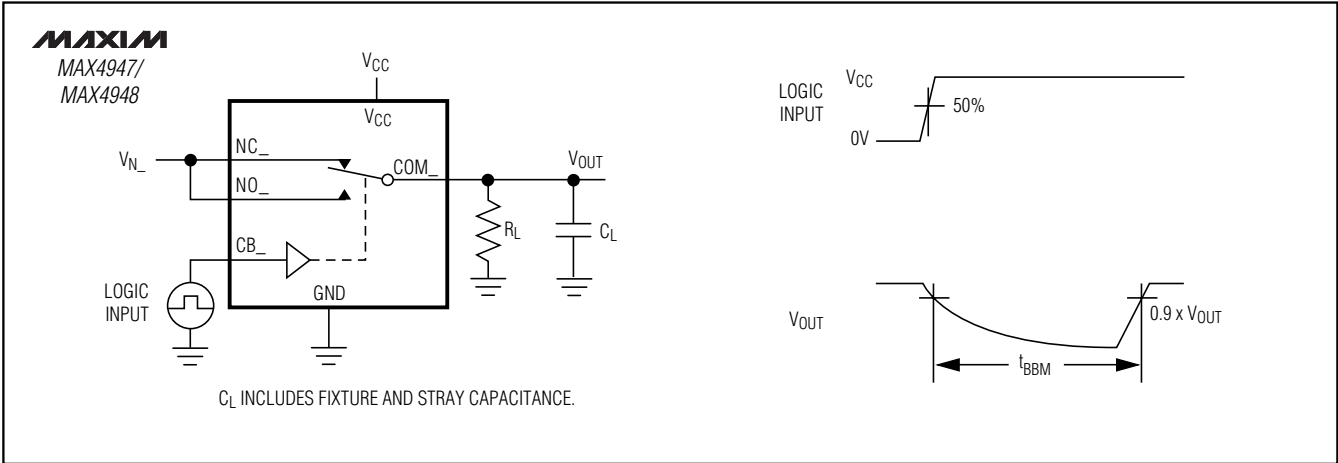


Figure 2. Break-Before-Make-Interval

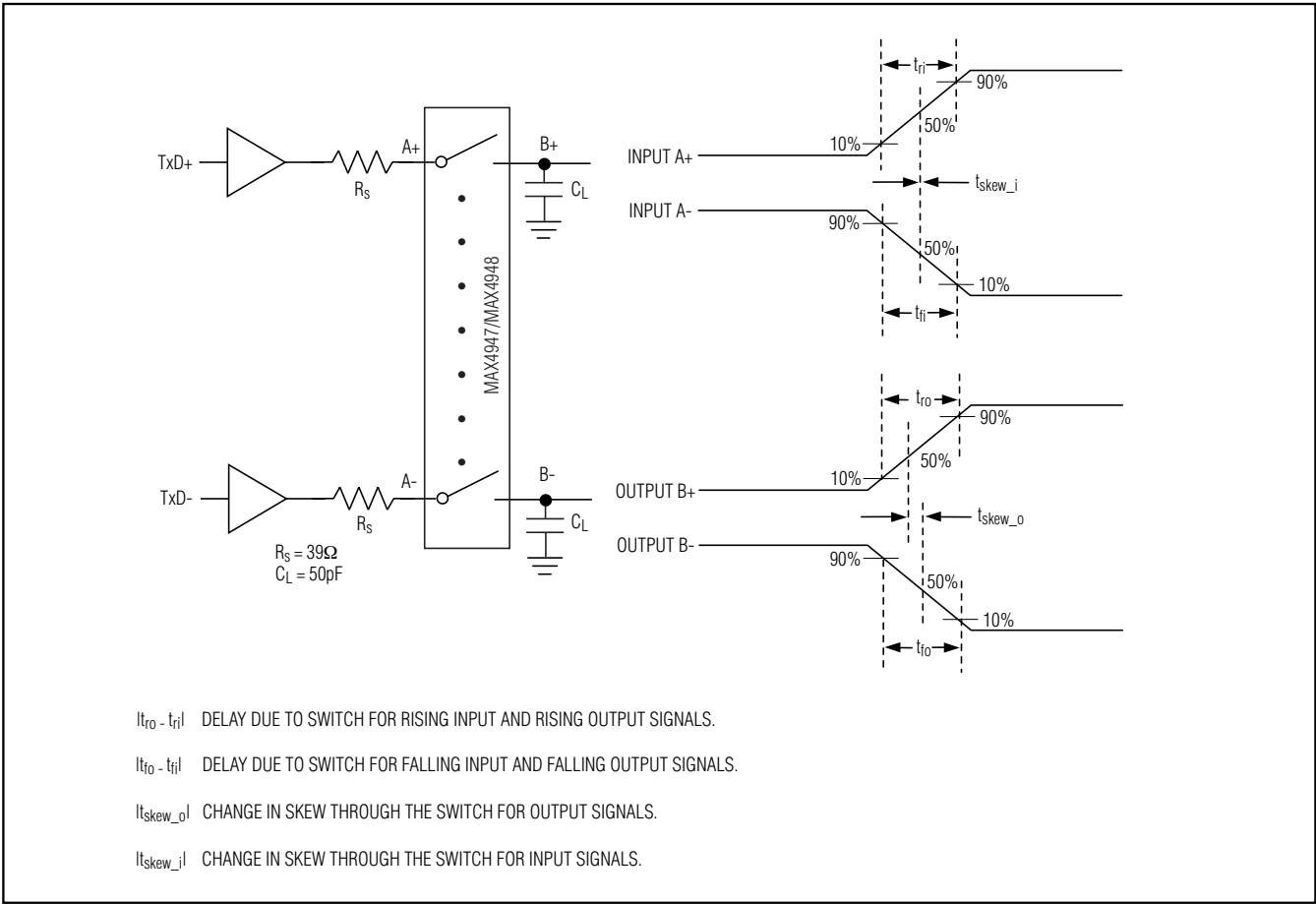


Figure 3. Input/Output Skew Timing Diagram

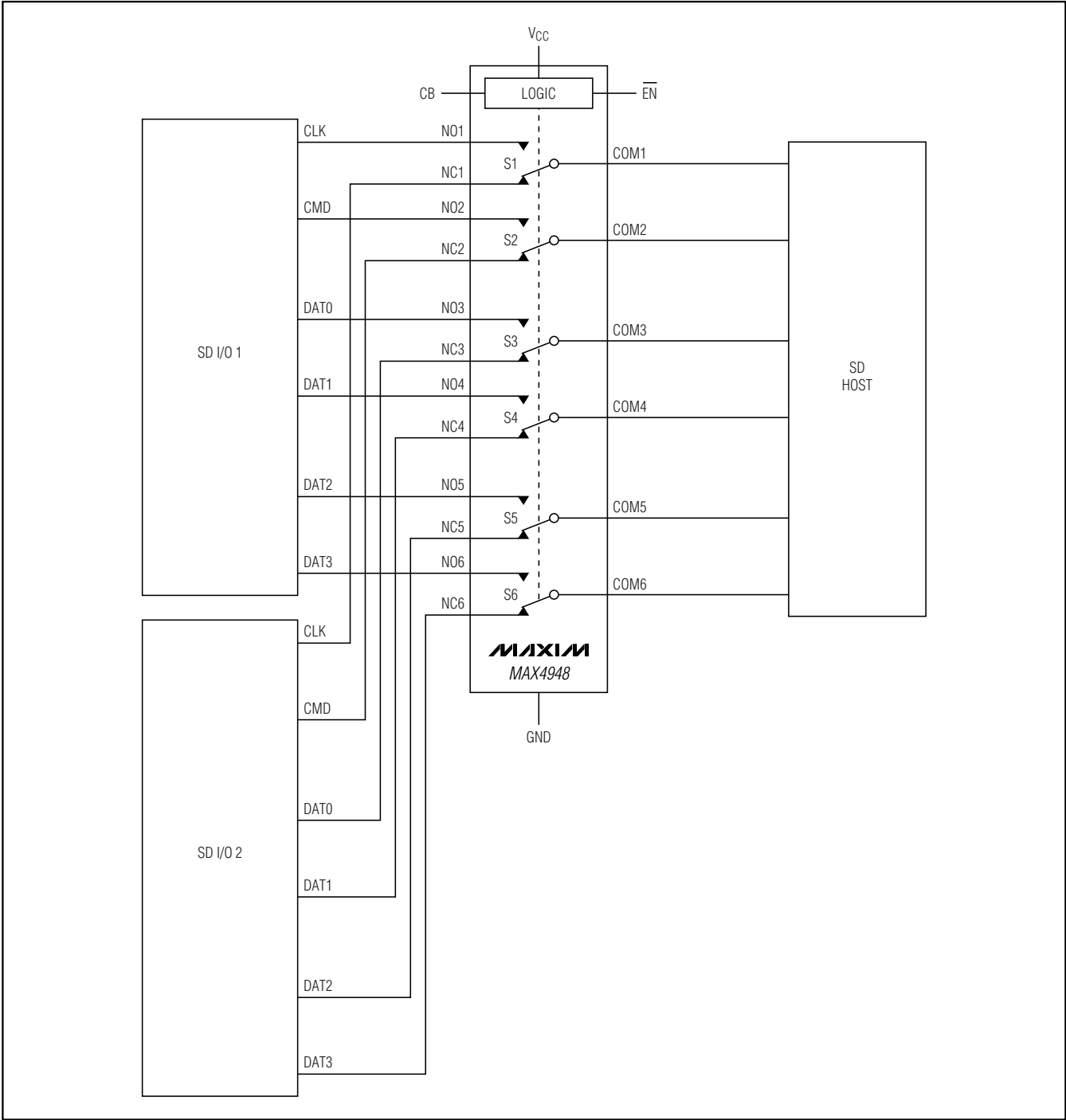
Timing Circuits/Timing Diagrams (continued)



Hex SPDT Data Switch

Typical Operating Circuit

MAX4947/MAX4948



Chip Information

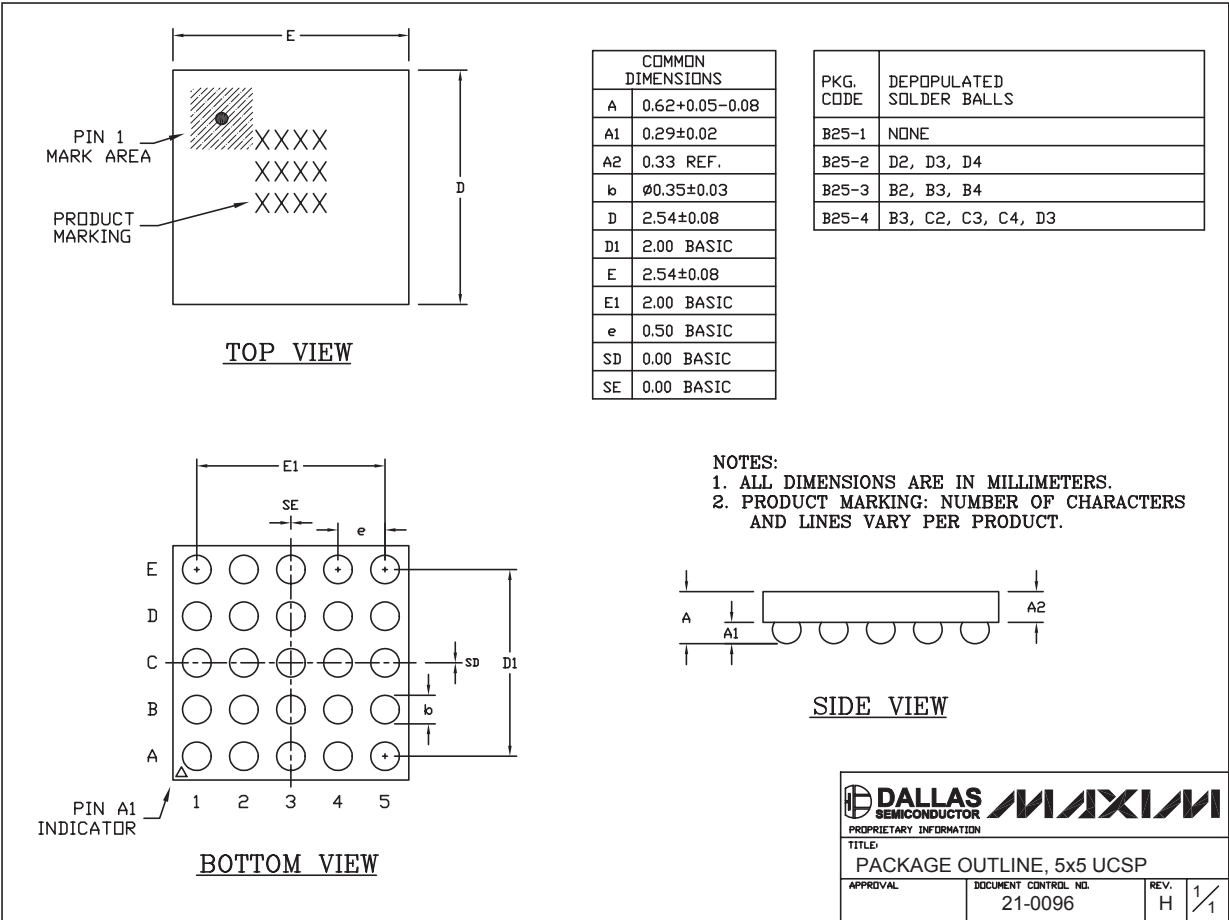
PROCESS: CMOS

[查询"MAX4947"供应商](#)

Hex SPDT Data Switch

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



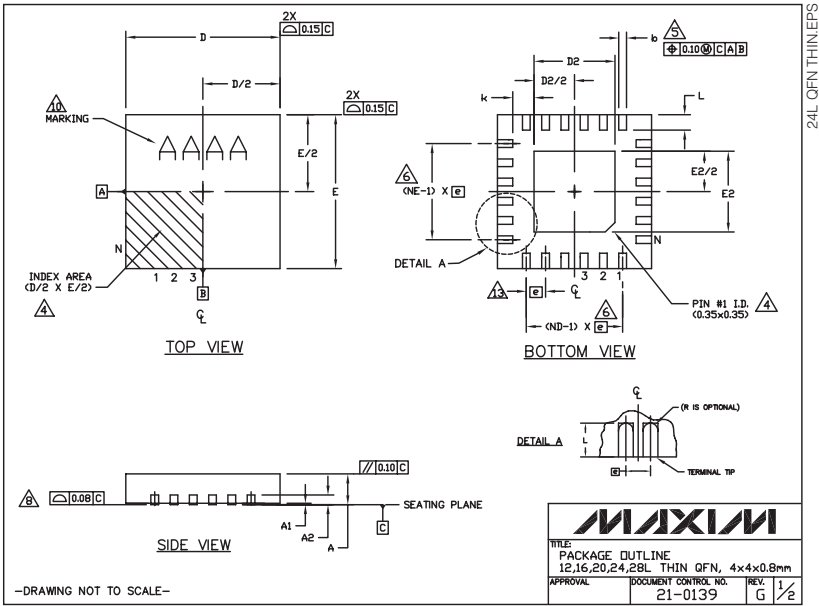
25L UCSP:EPS

Hex SPDT Data Switch

MAX4947/MAX4948

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



COMMON DIMENSIONS													EXPOSED PAD VARIATIONS												
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4			PKG	D2			E2					
REF.	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.	CODES	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.			
A	0.75	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	T1244-3	1.95	2.10	2.25	1.95	2.10	2.25			
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	T1244-4	1.95	2.10	2.25	1.95	2.10	2.25			
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF			T1644-3	1.95	2.10	2.25	1.95	2.10	2.25			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25	T1644-4	1.95	2.10	2.25	1.95	2.10	2.25			
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	T2044-2	1.95	2.10	2.25	1.95	2.10	2.25			
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	T2044-3	1.95	2.10	2.25	1.95	2.10	2.25			
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			T2444-2	1.95	2.10	2.25	1.95	2.10	2.25			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	T2444-3	2.45	2.60	2.63	2.45	2.60	2.63			
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	T2444-4	2.45	2.60	2.63	2.45	2.60	2.63			
N	12			16			20			24			28			T2844-1	2.50	2.60	2.70	2.50	2.60	2.70			
ND	3			4			5			6			7												
NE	3			4			5			6			7												
VDDIO	VGG8			VGGC			VGGD-1			VGGD-2			VGGG												

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MD220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
- MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
- COPLANARITY SHALL NOT EXCEED 0.08mm.
- VAPAGE SHALL NOT EXCEED 0.10mm.
- LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
- NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
- ALL DIMENSIONS ARE THE SAME FOR LEADED (-) & POFREE (++) PACKAGE CODES.

TITLE:
T1216,20,24,28L THIN QFN, 4x4x0.8mm

APPROVAL: _____ DOCUMENT CONTROL NO. _____ REV. G 2/

21-0139

Revision History

Pages changed at Rev 1: 1.

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