National Semiconductor

March 1993

54AC/74AC258 • 54ACT/74ACT258
Quad 2-Input Multiplexer with TRI-STATE® Outputs

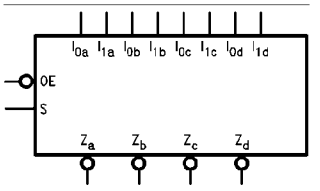
General Description

The 'AC/'ACT258 is a quad 2-input multiplexer with TRI-STATE outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus-oriented systems.

Features

- I_{CC} and I_{OZ} reduced by 50%
- Multiplexer expansion by tying outputs together
- Inverting TRI-STATE outputs
- Outputs source/sink 24 mA
- 'ACT258 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'ACT258: 5962-88704
  - — 'AC258: 5962-91604

Logic Symbols



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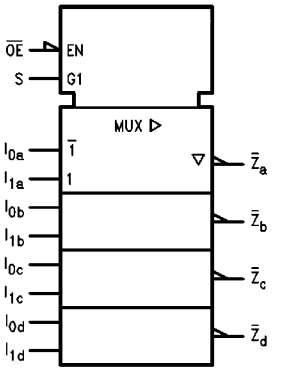
IEEE/IEC



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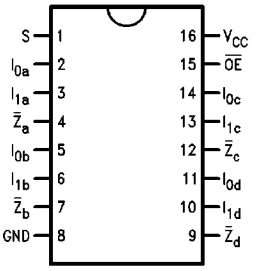
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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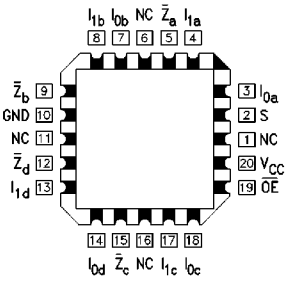
Pin Names	Description
S	Common Data Select Input
$\overline{OE}$	TRI-STATE Output Enable Input
I_{0a}–I_{0d}	Data Inputs from Source 0
I_{1a}–I_{1d}	Data Inputs from Source 1
$\overline{Z}_a$–$\overline{Z}_d$	TRI-STATE Inverting Data Outputs

Pin Assignment for LCC



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RRD-B30M75/Printed in U. S. A.

Functional Description

The 'AC/'ACT258 is a quad 2-input multiplexer with TRI-STATE outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The 'AC/'ACT258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{OE} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$\overline{Z}_b = \overline{OE} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$\overline{Z}_c = \overline{OE} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$\overline{Z}_d = \overline{OE} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

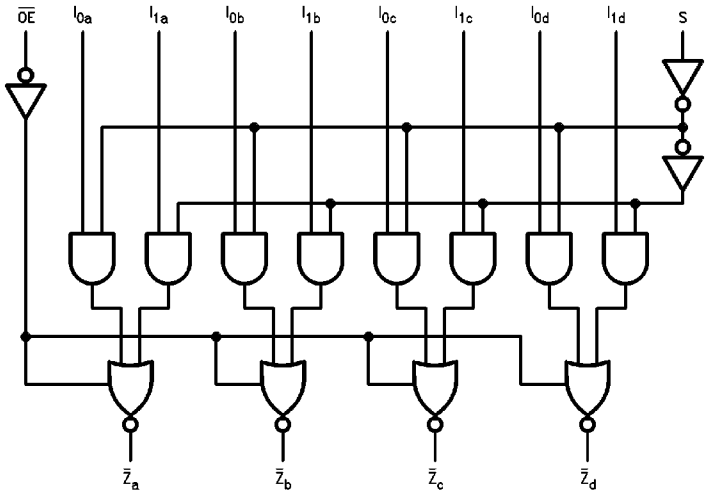
When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance state. If the outputs of the TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so there is no overlap.

Truth Table

Output Enable	Select Input	Data Inputs		Outputs
$\overline{OE}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	74AC T_A = −55°C to +125°C	54AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.4	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7		
		5.5		4.86	4.7		
		3.0			2.46		
		4.5			3.76		I_{OH} −24 mA
		5.5			4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.50	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50		
		5.5		0.36	0.50		
		3.0			0.44		
		4.5			0.44		I_{OL} 24 mA
		5.5			0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
I_{OZ}	Maximum TRI-STATE Current	5.5	±0.25	±5.0	±2.5	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5		50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5		−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	4.0	80.0	40.0	μA	V_{IN} = V_{CC} or GND

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Current	5.5		±0.25	±5.0	±2.5	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	3.3	2.0	6.0	9.5	1.0	12.0	1.5	11.0	ns
		5.0	1.5	4.5	7.5	1.0	9.5	1.0	8.5	
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	3.3	2.0	5.0	8.5	1.0	10.5	1.5	9.5	ns
		5.0	1.5	4.0	6.5	1.0	7.5	1.0	7.0	
t_{PLH}	Propagation Delay S to $\overline{Z}_n$	3.3	3.0	7.5	12.0	1.0	15.0	2.5	14.0	ns
		5.0	2.0	6.0	9.5	1.0	11.5	1.5	10.5	
t_{PHL}	Propagation Delay S to $\overline{Z}_n$	3.3	2.5	7.5	11.5	1.0	14.0	2.0	13.0	ns
		5.0	1.5	5.5	9.0	1.0	10.5	1.5	10.0	
t_{PZH}	Output Enable Time	3.3	2.5	6.0	9.5	1.0	11.5	2.0	10.5	ns
		5.0	1.5	4.5	7.5	1.0	9.0	1.5	8.5	
t_{PZL}	Output Enable Time	3.3	2.0	5.5	9.0	1.0	10.5	1.5	10.0	ns
		5.0	1.5	5.5	7.0	1.0	8.5	1.0	8.0	
t_{PHZ}	Output Disable Time	3.3	2.5	5.5	10.0	1.0	11.5	2.0	11.0	ns
		5.0	2.0	5.5	8.5	1.0	9.5	1.5	9.0	
t_{PLZ}	Output Disable Time	3.3	2.0	5.5	9.0	1.0	10.5	2.0	10.0	ns
		5.0	1.5	5.0	7.0	1.0	8.5	1.5	8.0	

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	5.0	2.0	6.5	8.5	1.0	10.5	1.5	9.5	ns
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	5.0	2.0	5.5	7.5	1.0	9.0	1.5	8.0	ns
t_{PLH}	Propagation Delay S to $\overline{Z}_n$	5.0	3.0	7.5	10.5	1.0	13.0	2.0	11.5	ns
t_{PHL}	Propagation Delay S to $\overline{Z}_n$	5.0	1.5	7.0	9.5	1.0	12.0	1.5	11.0	ns
t_{PZH}	Output Enable Time	5.0	2.0	6.5	8.5	1.0	10.5	1.5	9.5	ns
t_{PZL}	Output Enable Time	5.0	2.0	6.5	8.5	1.0	10.0	1.5	9.5	ns
t_{PHZ}	Output Disable Time	5.0	1.5	7.0	9.0	1.0	10.5	1.0	10.0	ns
t_{PLZ}	Output Disable Time	5.0	2.0	6.0	8.0	1.0	10.0	1.5	9.0	ns

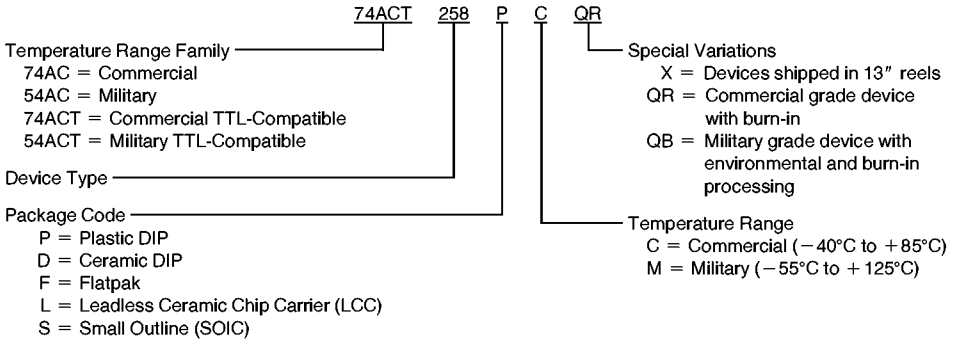
*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

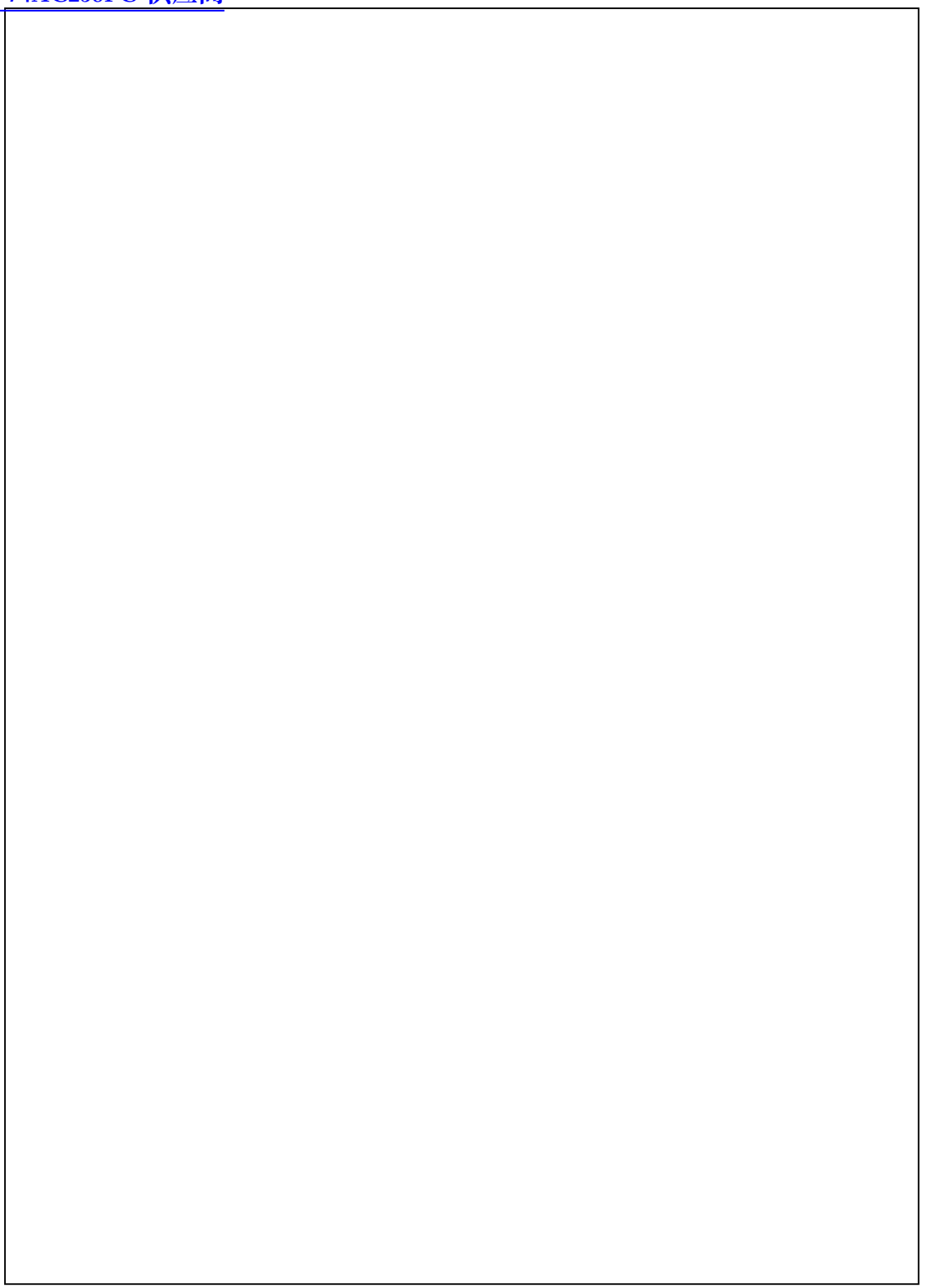
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	55.0	pF	V_{CC} = 5.0V

Ordering Information

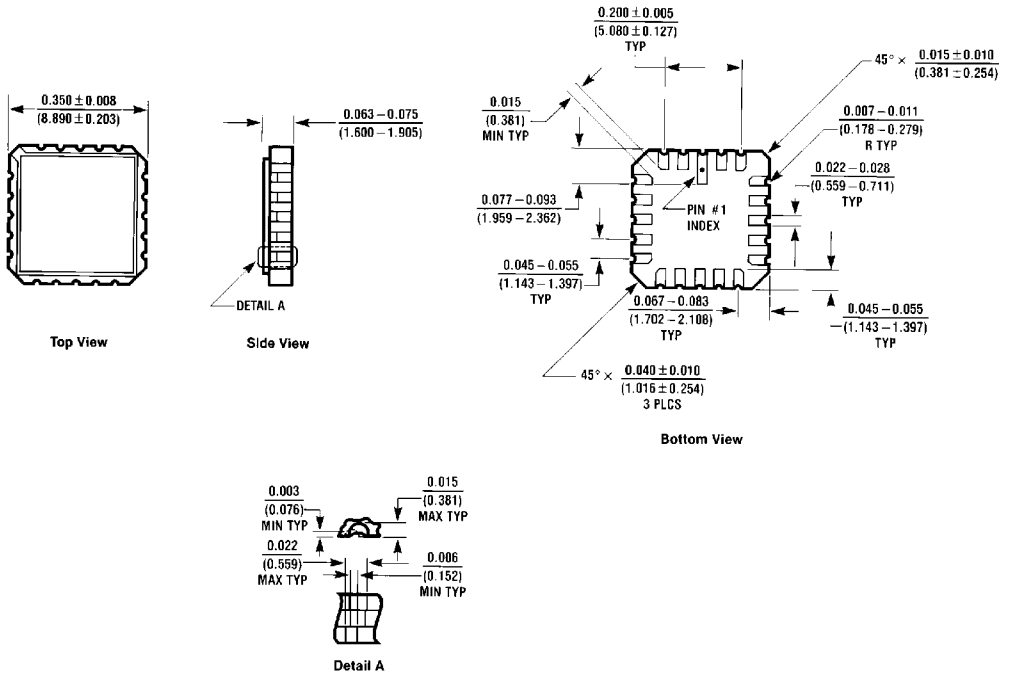
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



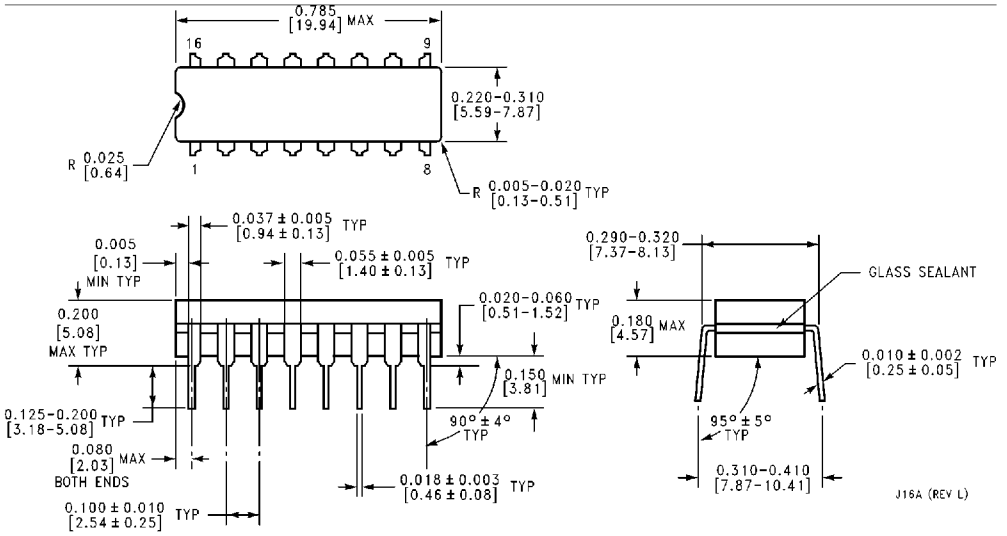
查询"74AC258PC"供应商



Physical Dimensions inches (millimeters)

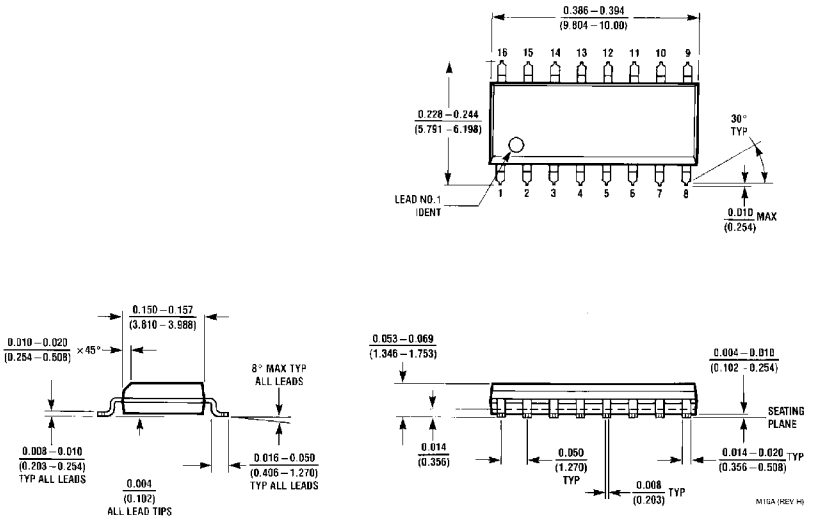


20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

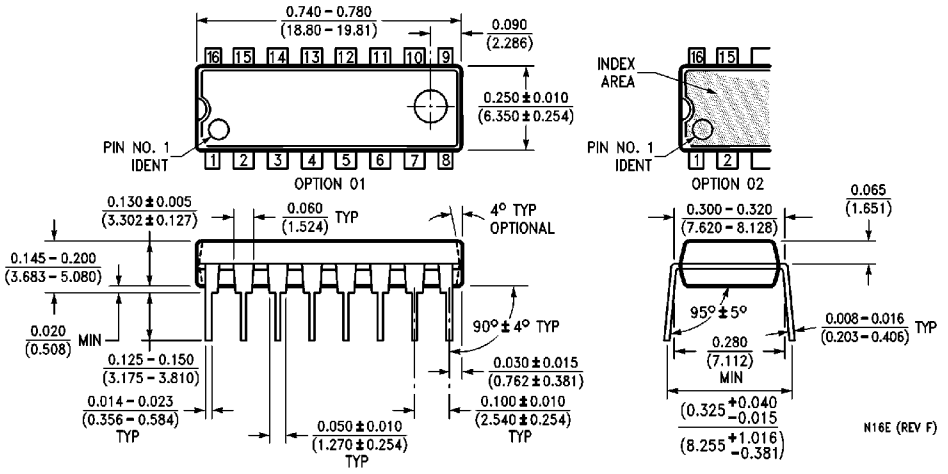


16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)

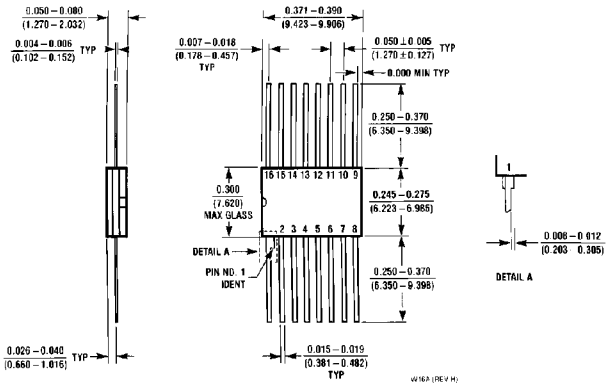


16-Lead Small Outline Integrated Circuit (S)
NS Package Number M16A



16-Lead Plastic Dual-In-Line Package (P)
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flatpak (F)
NS Package Number W16A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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