31.5 dB Range, 0.5 dB Step Size Programmable VGA

Preliminary Technical Data

ADL5202

FEATURES

- Dual independent digitally controlled VGAs
- −11.5 to 20 dB Gain Range
- 0.5 dB step size ±0.1 dB
- 150 Ω differential input and output
- 6 dB noise figure @ maximum gain
- OIP3 of 50 dBm at 200 MHz
- −3 dB bandwidth of 700 MHz
- Multiple control interface options
  - Parallel 6-bit control interface
  - Serial peripheral interface
  - Gain step up/down interface
- Wide input dynamic range
- High performance power mode
- Power-down control
- Single 5 V supply operation
- 40-Lead LFCSP 6 x 6 mm package

APPLICATIONS

- Differential ADC drivers
- High IF sampling receivers
- High output power IF amplification
- Instrumentation

FUNCTIONAL BLOCK DIAGRAM

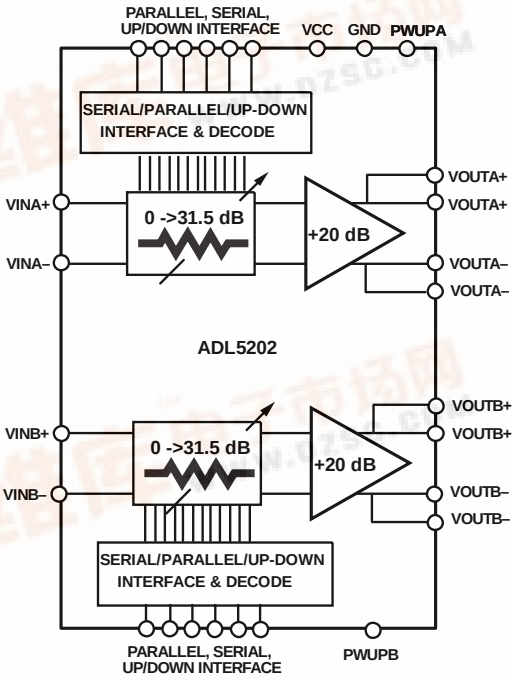


Figure 1.

GENERAL DESCRIPTION

The ADL5202 is a digitally controlled, variable gain wide bandwidth amplifier that provides precise gain control, high IP3 and low noise figure. The excellent distortion performance and high signal bandwidth makes the ADL5202 an excellent gain control device for a variety of receiver applications.

For wide input dynamic range applications, the ADL5202 provides a broad 31.5 dB gain range with 0.5 dB resolution. The gain is adjustable through multiple gain control interface options: parallel, serial peripheral interface, or gain step up/down.

Using a high speed SiGe process and incorporating proprietary distortion cancellation techniques, the ADL5202 achieves better than 50 dBm output IP3 at frequencies approaching 200 MHz for all gain settings. The ADL5202 is powered on by applying the appropriate logic level to the PWUP pin. The quiescent current of the ADL5202 is typically 160 mA. It may be configured for higher quiescent current of 220 mA, in high performance power mode, for more demanding applications. When powered down, the ADL5202 consumes less than 18 mA and offers excellent input to output isolation. The gain setting is preserved when powered down.

Fabricated on an ADI's high speed SiGe process, the ADL5202 provides precise gain adjustment capabilities with good distortion performance. The ADL5202 amplifier comes in a compact, thermally enhanced 6 x 6mm 40-lead LFCSP package and operates over the temperature range of −40°C to +85°C

Rev. PrD

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

10/10—Rev. PrD

10/10—Rev. PrC

9/10—Rev. PrB

9/10—Rev. PrA

SPECIFICATIONS

V_S = 5 V, T = 25°C, Z_S = Z_L = 150Ω at 100MHz, PM = 0 V, 2 V p-p differential output unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} < 2 V p-p (5.2dBm)		700		MHz
Slew Rate			TBD		V/nsec
INPUT STAGE	Pins VIN+ and VIN-				
Maximum Input Swing	Gain Code = 111111		8		V p-p
Differential Input Resistance	Differential		150		Ω
Common-Mode Input Voltage			1.5		V
CMRR	Gain Code = 000000		TBD		dB
GAIN					
Maximum Voltage Gain	Gain Code = 000000		20		dB
Minimum Voltage Gain	Gain Code = 111111		−11.5		dB
Gain Step Size			0.5		dB
Gain Flatness	30 MHz < f_C < 200MHz		TBD		dB
Gain Temperature Sensitivity	Gain Code = 000000		TBD		mdB/°C
Gain Step Response	For V_{IN} = 0.2V, Gain Code 111111to 000000		15		ns
Gain Conformance Error	Normalized to 10dB gain step		±0.03		dB
Phase Conformance Error	Normalized to 10dB gain step		1.0		deg
OUTPUT STAGE	Pins OUT+ and OUT-				
Output Voltage Swing	At P1dB, Gain Code = 000000		10		V p-p
Differential Output Resistance	Differential		150		Ω
NOISE/HARMONIC PERFORMANCE					
46 MHz [High Performance Power Mode]	Gain Code = 000000, LP = Low				
Noise Figure			6		dB
Second Harmonic	V_{OUT} = 2 V p-p		−90		dBc
Third Harmonic	V_{OUT} = 2 V p-p		−100		dBc
Output IP3			TBD		dBm
Output 1 dB Compression Point			18.6		dBm
46 MHz [Nominal Power Mode]	Gain Code = 000000, PM = High				
Noise Figure			TBD		dB
Second Harmonic	V_{OUT} = 2 V p-p		-90		dBc
Third Harmonic	V_{OUT} = 2 V p-p		-100		dBc
Output IP3			TBD		dBm
Output 1 dB Compression Point			TBD		dBm
NOISE/HARMONIC PERFORMANCE					
70 MHz [High Performance Power Mode]	Gain Code = 000000, LP = Low				
Noise Figure			6		dB
Second Harmonic	V_{OUT} = 2 V p-p		−88		dBc
Third Harmonic	V_{OUT} = 2 V p-p		−100		dBc
Output IP3			46.4		dBm
Output 1 dB Compression Point			19.7		dBm

Parameter	Conditions	Min	Typ	Max	Unit
70 MHz [Nominal Power Mode]	Gain Code = 000000, PM = High				
Noise Figure			TBD		dB
Second Harmonic	V_{OUT} = 2 V p-p		-88		dBc
Third Harmonic	V_{OUT} = 2 V p-p		-100		dBc
Output IP3			40		dBm
Output 1 dB Compression Point			TBD		dBm
NOISE/HARMONIC PERFORMANCE					
140 MHz [High Performance Power Mode]	Gain Code = 000000, LP = Low				
Noise Figure			6.4		dB
Second Harmonic	V_{OUT} = 2 V p-p		–88		dBc
Third Harmonic	V_{OUT} = 2 V p-p		–97		dBc
Output IP3			TBD		dBm
Output 1 dB Compression Point			19.7		dBm
140 MHz [Nominal Power Mode]	Gain Code = 000000, PM = High				
Noise Figure			TBD		dB
Second Harmonic	V_{OUT} = 2 V p-p		-88		dBc
Third Harmonic	V_{OUT} = 2 V p-p		-97		dBc
Output IP3			TBD		dBm
Output 1 dB Compression Point			TBD		dBm
NOISE/HARMONIC PERFORMANCE					
170 MHz [High Performance Power Mode]	Gain Code = 000000, LP = Low				
Noise Figure			6.5		dB
Second Harmonic	V_{OUT} = 2 V p-p		–82		dBc
Third Harmonic	V_{OUT} = 2 V p-p		–97		dBc
Output IP3			46.7		dBm
Output 1 dB Compression Point			19.7		dBm
170 MHz [Nominal Power Mode]	Gain Code = 000000, PM = High				
Noise Figure			TBD		dB
Second Harmonic	V_{OUT} = 2 V p-p		-77		dBc
Third Harmonic	V_{OUT} = 2 V p-p		-95		dBc
Output IP3			39.7		dBm
Output 1 dB Compression Point			TBD		dBm
NOISE/HARMONIC PERFORMANCE					
240 MHz [High Performance Power Mode]	Gain Code = 000000, LP = Low				
Noise Figure			6.9		dB
Second Harmonic	V_{OUT} = 2 V p-p		–78		dBc
Third Harmonic	V_{OUT} = 2 V p-p		–93		dBc
Output IP3			TBD		dBm
Output 1 dB Compression Point			19.7		dBm
240 MHz [Nominal Power Mode]	Gain Code = 000000, PM = High				
Noise Figure			TBD		dB
Second Harmonic	V_{OUT} = 2 V p-p		-73		dBc
Third Harmonic	V_{OUT} = 2 V p-p		-93		dBc
Output IP3			TBD		dBm
Output 1 dB Compression Point			TBD		dBm

Parameter	Conditions	Min	Typ	Max	Unit
NOISE/HARMONIC PERFORMANCE					
300 MHz [High Performance Power Mode]	Gain Code = 000000, LP = Low				
Noise Figure			7.3		dB
Second Harmonic	V_{OUT} = 2 V p-p		−70		dBc
Third Harmonic	V_{OUT} = 2 V p-p		−88		dBc
Output IP3			TBD		dBm
Output 1 dB Compression Point			19.5		dBm
300 MHz [Nominal Power Mode]	Gain Code = 000000, PM = High				
Noise Figure			TBD		dB
Second Harmonic	V_{OUT} = 2 V p-p		-68		dBc
Third Harmonic	V_{OUT} = 2 V p-p		-88		dBc
Output IP3			TBD		dBm
Output 1 dB Compression Point			TBD		dBm
NOISE/HARMONIC PERFORMANCE					
380 MHz [High Performance Power Mode]	Gain Code = 000000, LP = Low				
Noise Figure			7.8		dB
Second Harmonic	V_{OUT} = 2 V p-p		−67		dBc
Third Harmonic	V_{OUT} = 2 V p-p		−80		dBc
Output IP3			TBD		dBm
Output 1 dB Compression Point			18.4		dBm
380 MHz [Nominal Power Mode]	Gain Code = 000000, PM = High				
Noise Figure			TBD		dB
Second Harmonic	V_{OUT} = 2 V p-p		-65		dBc
Third Harmonic	V_{OUT} = 2 V p-p		-80		dBc
Output IP3			TBD		dBm
Output 1 dB Compression Point			TBD		dBm
ENABLE INTERFACE	Pin PWUP				
Enable Threshold	Minimum voltage to enable the device			1.4	V
PWUP Input Bias Current			TBD		nA
GAIN CONTROL INTERFACE	Digital pins				
V_{IH}	Minimum voltage for a logic high	1.4			V
V_{IL}	Maximum voltage for a logic low			0.8	
Maximum Input Bias Current			TBD		nA
POWER-INTERFACE					
Supply Voltage		4.5		5.5	V
Quiescent Current	PM = Low (High Performance Power Mode)		220		mA
	PM = High (Nominal Power Mode)		160		mA
Power Down Current	PWUP Low		18		mA

ABSOLUTE MAXIMUM RATINGS

Table Summary

Table 2.

Parameter	Rating
Supply Voltage, V_{POS}	5.5 V
PWUP, Digital Pins	-0.6 to (V_{POS} + 0.6V)
Input Voltage, V_{IN+} ,V_{IN-}	-0.6 to +3.1V
Internal Power Dissipation	TBD mW
θ_{JA} (Exposed paddle soldered down)	TBD°C/W
θ_{JA} (Exposed paddle not soldered down)	TBD°C/W
θ_{JC} (At exposed paddle soldered down)	TBD°C/W
Maximum Junction Temperature	TBD°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

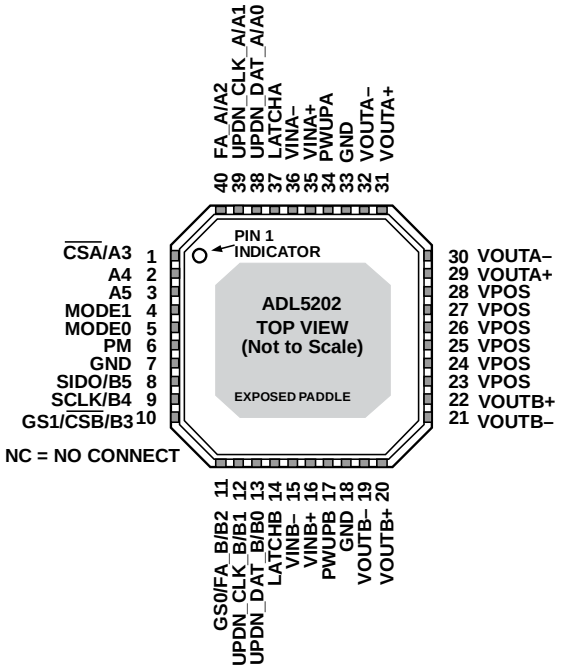


Figure 2. 40 Lead LFCSP

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{CSA}}$/A3	Multi function pin: When Serial mode is enabled, a logic low on this pin selects Channel A. In Parallel mode, this bit 3 for the gain control interface.
2	A4	Bit 4 for channel A parallel gain control interface.
3	A5	Bit 5, (MSB) for channel A parallel gain control interface.
4	MODE1	MSB for the mode control parallel, SPI, up/down interface.
5	MODE0	LSB for the mode control parallel, SPI, up/down interface.
6	PM	A logic high on this pin enables high performance mode. A logic low enables nominal performance mode.
7, 18, 33, EP[1]	GND	Ground
8	SDIO/B5	Multi function pin: When $\overline{\text{CSA}}$ or $\overline{\text{CSB}}$ is pulled low, SDIO is used for reading and writing to the SPI port. In parallel mode, This bit is 5 (MSB) for the channel B parallel gain control interface.
9	SCLK/B4	Multi function pin: When SPI mode is selected this pin is the serial clock input. In parallel mode this pin is bit 4 for channel B gain interface.
10	GS1/$\overline{\text{CSB}}$/B3	Multi function pin: When the UP/DOWN mode is enabled, this pin is the MSB for the gain step size control. When serial mode is enabled, a logic low on this pin selects channel B. In parallel mode, this is bit 3 of the gain control interface.
11	GS0 FA_B/B2	Multi function pin: When the UP/DOWN mode is enabled, this pin is the LSB for the gain step size control. A logic high enables the channel B SPI port fast attack mode. In parallel mode this pin is bit 2 for channel B gain interface.
12	UPDN_CLK_B/B1	Multi function pin: this pin is the clock interface for channel B UPDN function. In Parallel mode this pin is bit1 for channel B gain interface.
13	UPDN_DAT_B/B0	Multi function pin: this pin is the data pin for channel B UPDN function. In parallel mode this is bit 0 for channel B gain interface.
14	LATCHB	Latch, a low input results in gain change. A high input results in no gain change.
15	VINB–	Channel B negative input.
16	VINB+	Channel B positive input.

Pin No.	Mnemonic	Description
17	PWUPB	Channel B power up. A logic high on this pin enables the part.
19, 21	VOUTB+	Channel B positive output.
20, 22	VOUTB–	Channel B negative output.
23, 24, 25, 26, 27, 28,	VPOS	Positive power supply.
29, 31	VOUTA+	Channel A positive output
30, 32	VOUTA–	Channel A negative output
34	PWUPA	Channel A power up. A logic high on this pin enables the part.
35	VINA+	Channel A positive input.
36	VINA–	Channel A negative input.
37	LATCHA	Latch, a low input results in gain change. A high input results in no gain change.
38	UPDN_DAT_A/A0	Multi function pin: this pin is the data pin for channel A UPDN function. In parallel mode this is bit 0 for channel A gain interface.
39	UPDN_CLK_A/A1	Multi function pin: this pin is the clock interface for channel A UPDN function. In Parallel mode this pin is bit1 for channel A gain interface.
40	GS0 FA_B/B2	Multi function pin: When the UP/DOWN mode is enabled, this pin is the LSB for the gain step size control. A logic high enables the channel A SPI port fast attack mode. In parallel mode this pin is bit 2 for channel A gain interface.

[1] Exposed Paddle

DIGITAL INTERFACE OVERVIEW

The ADL5202 DVGA has three digital control interface options:

- Parallel Control Interface
- Serial Peripheral Interface
- Gain Step Up/Down Interface

The digital control interface selection is made via 2 digital pins, MODE1 and MODE0, as shown in Table 5. There are two common digital control pins, PM and PWUP. PM selects between two power modes. PWUP is a power up pin. The gain code used is 6 bit binary.

Physical pins are shared between 3 interfaces resulting in as many as 3 different functions per digital pin (see Table 4)

Table 5. Digital control interface selection truth table

MODE1	MODE0	Interface
0	0	Parallel
0	1	Serial (SPI)
1	0	Up/Down
1	1	Up/Down

Parallel Digital Interface

The parallel digital interface uses 6 gain control bits and a latch pin per amplifier. The latch pin controls whether the input data latch is transparent or latched. In transparent mode, gain changes as input gain control bits change. In latched mode, gain is determined by the latched gain setting and does not change with changing input gain control bits.

Serial Peripheral Interface (SPI)

The SPI uses 3 pins (SDIO, SCLK, and /CSA or /CSB). The SPI data register consists of 2 bytes: 6 gain control bits, 2 attenuation step size address bits, 1 read/write bit, and 7 do not care bits.

The SPI uses a bidirectional pin, SDIO, for writing to the SPI register and for reading from the SPI register. In order to write to the SPI register, $\overline{CSA}$ or $\overline{CSB}$ needs to be pulled low and 16 clock pulses must be applied. Individual channel SPI registers can be selected by pulling low $\overline{CSA}$ or $\overline{CSB}$. By simultaneously pulling low the $\overline{CSA}$ and $\overline{CSB}$ pins, the same data can be written to both SPI registers.

In order to read the SPI register value, the R/W bit needs to be set high, $\overline{CSA}$ or $\overline{CSB}$ needs to be pulled low, and the part clocked. Once the register has been read out the R/W bit needs to be set low and SPI put in write mode. Note that there is only one SDIO pin. Read back from the registers should be done individually.

SPI fast attack mode is controlled by FA_A or FA_B. A logic high on the FA pin results in an attenuation selected by FA1 and FA0 bits in the SPI register.

Table 6. SPI 2-bit attenuation step size truth table

FA1	FA0	Step Size (dB)
0	0	2
0	1	4
1	0	8
1	1	16

UP/DOWN Interface

The UP/DOWN interface uses two digital pins to control the gain. Gain is increased by a clock pulse on UPDN_CLK (rising and falling edges) when UPDN_DAT is high. Gain is decreased by a clock pulse on UPDN_CLK when UPDN_DAT is low. Reset is detected by a rising edge latching data having one polarity with the falling edge latching the opposite polarity. Reset results in minimum gain code 111111_{bin}.

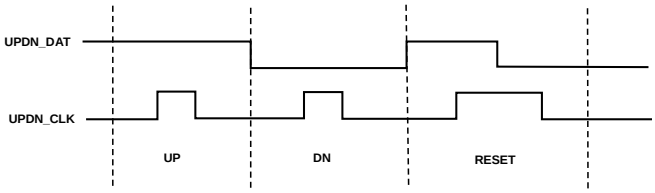


Figure 3. UP/DOWN Timing

The step size is selectable by pins GS1 and GS0. The default step size is 0.5dB. The gain code count will rail at the top and bottom of the control range.

Table 7. Step size control truth table

GS1	GS0	Step Size (dB)
0	0	0.5
0	1	1
1	0	2
1	1	4

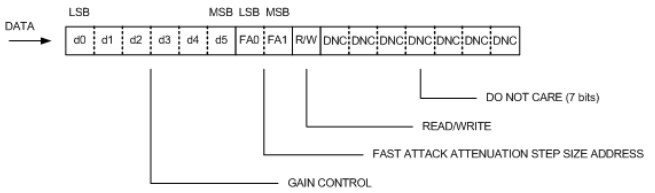


Figure 4. 16- bit SPI Register

TYPICAL PERFORMANCE CHARACTERISTICS

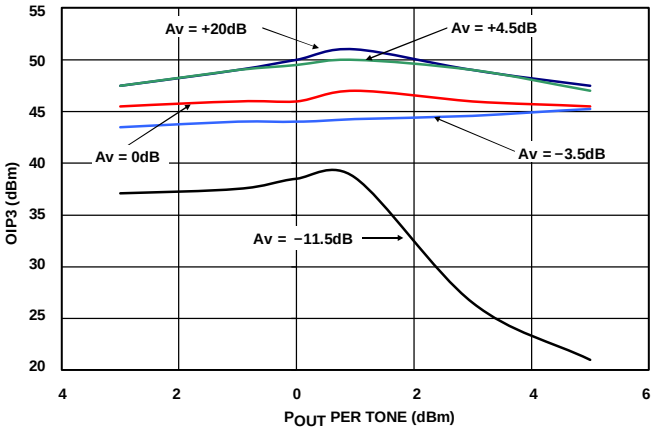


Figure 5. OIP3 vs. Power @ 5 Gains

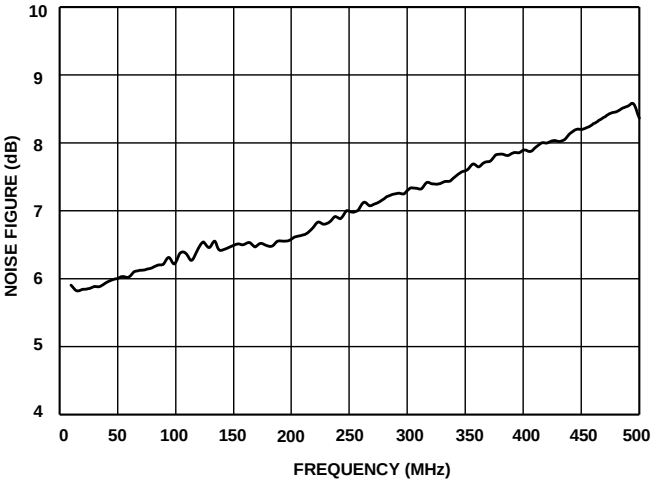


Figure 8. Noise Figure Vs. Frequency at Max Gain

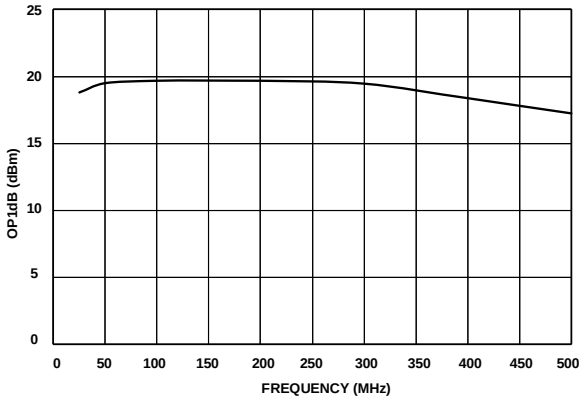


Figure 6. P1dB Vs. Frequency at Max Gain

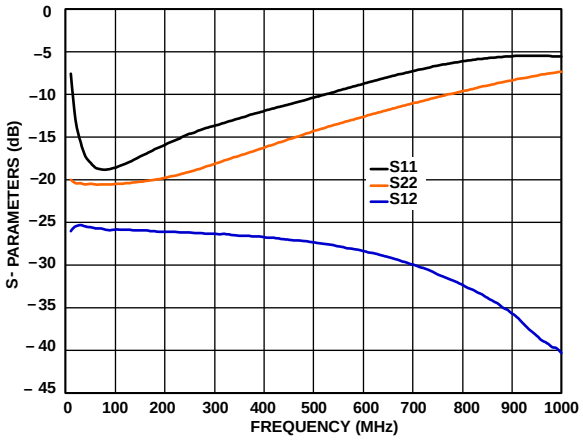


Figure 9. S11, S12 and S22 Vs. Frequency

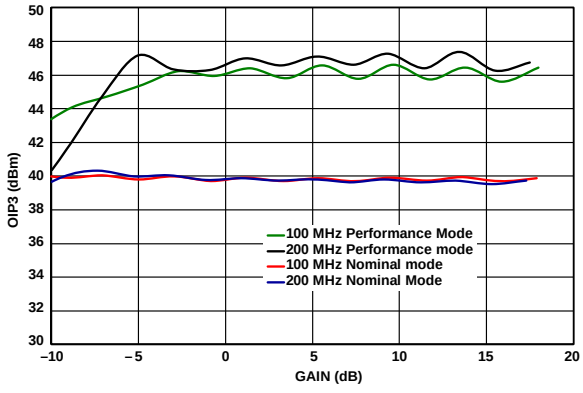


Figure 7. OIP3 Vs. Gain

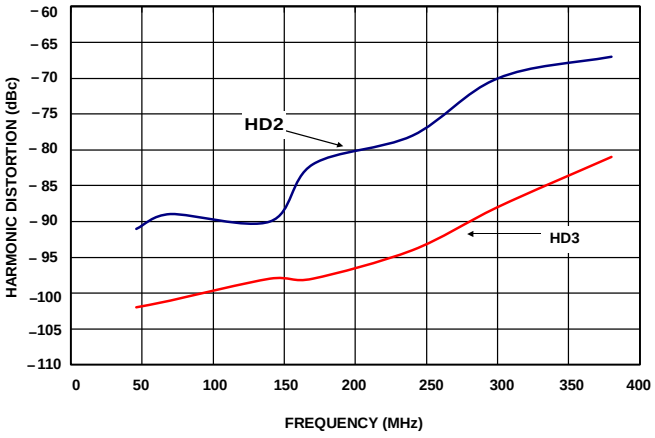
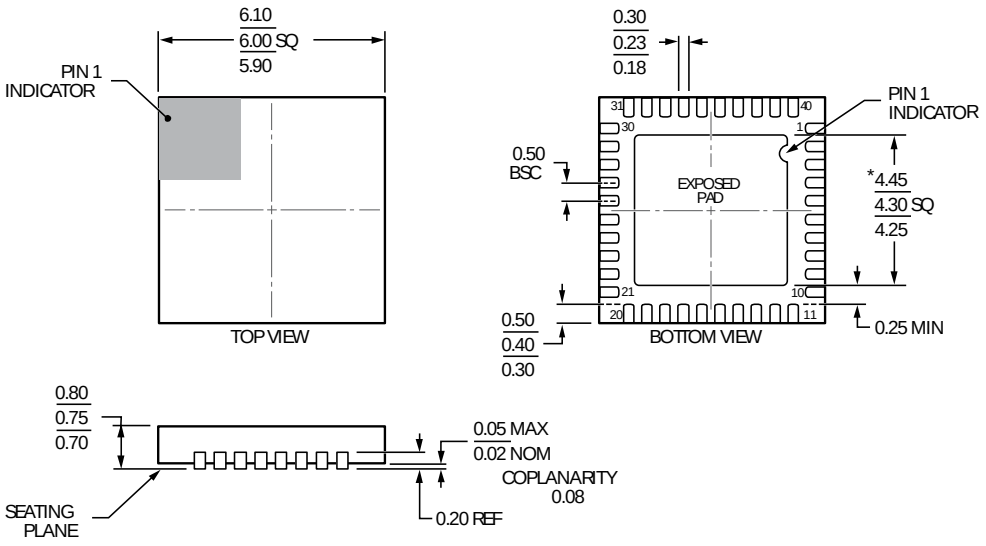


Figure 10. Harmonic Distortion Vs. Frequency 2Vp-p Out

OUTLINE DIMENSIONS

40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
6 x 6 mm Body, Very Very Thin Quad
(CP-40-10)
Dimensions shown in millimeters



*COMPLIANT TO JEDEC STANDARDS MO-220-WJJD-6
WITH EXCEPTION TO EXPOSED PAD DIMENSION.

110708-A

Figure 11. 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
6 mm × 6 mm Body, Very Thin Quad
(CP-40-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADL5202XCPZ-R7[1]	−40°C to +85°C	40 Lead LFCSP_WQ, 7″ Reel	CP-40-10
ADL5202XCPZ-WP[1]	−40°C to +85°C	40 Lead LFCSP_WQ, Waffle Pack	CP-40-10
ADL5202-EVALZ[1]	−40°C to +85°C	Evaluation Board	

[1] Z = RoHS Compliant Part

PR09387-0-10/10(PRD)