LT1193

Video Difference Amplifier

FEATURES

- Differential or Single-Ended Gain Block (Adjustable)
- −3dB Bandwidth, $A_V = \pm 2$ 80MHz
- Slew Rate 500V/μs
- Low Cost
- Output Current ±50mA
- Settling Time 180ns to 0.1%
- CMRR @ 10MHz >40dB
- Differential Gain Error 0.2%
- Differential Phase Error 0.08°
- Single +5V Operation
- Drives Cables Directly
- Output Shutdown

APPLICATIONS

- Line Receivers
- Video Signal Processing
- Cable Drivers
- Oscillators
- Tape and Disc Drive Systems

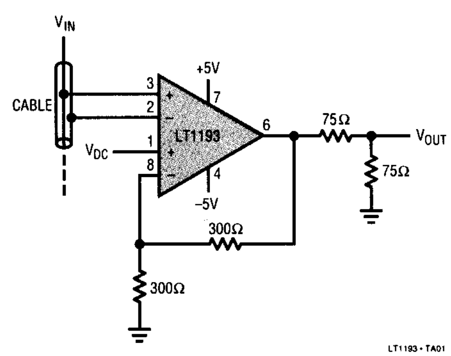
DESCRIPTION

The LT1193 is a video difference amplifier optimized for operation on ±5V, and a single +5V supply. This versatile amplifier features uncommitted high input impedance (+) and (−) inputs, and can be used in differential or single-ended configurations. Additionally, a second set of inputs give gain adjustment and DC control to the differential amplifier.

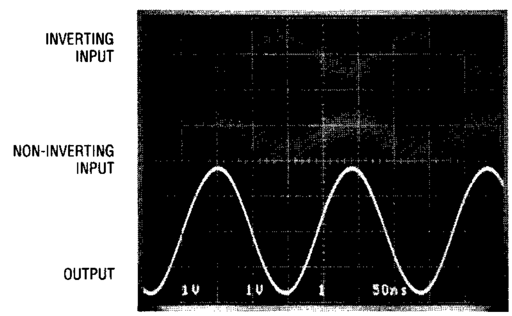
The LT1193's high slew rate, 500V/μs, wide bandwidth, 80MHz, and ±50mA output current, make it ideal for driving cables directly. The shutdown feature reduces the power dissipation to a mere 15mW, and allows multiple amplifiers to drive the same cable.

The LT1193 is available in 8-pin miniDIPs and SO packages.

Cable Sense Amplifier for Loop Through Connections with DC Adjust



Recovered Signal from Common Mode Noise

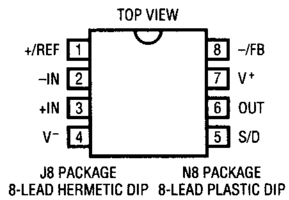


5MHz SINE WAVE RECOVERED FROM COMMON MODE NOISE, $A_V = +2$

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Differential Input Voltage .... ± 6V
Input Voltage .... $\pm V_S$
Output Short Circuit Duration (Note 1) .... Continuous
Operating Junction Temperature Range
  LT1193M .... −55°C to 150°C
  LT1193C .... 0°C to 150°C
Max. Junction Temperature .... See Pkg. Descriptions
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1193MJ8
LT1193CJ8
LT1193CN8
LT1193CS8

ELECTRICAL CHARACTERISTICS

$V_S = \pm 5V$, $V_{REF} = 0V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to ground, $R_L = R_{FB1} + R_{FB2} = 1k$ (Note 2), $T_A = 25°C$, $C_L \leq 10pF$, pin 5 open circuit, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1193M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Both Inputs, (Note 3)		2.0	12.0	mV
I_{OS}	Input Offset Current	Either Input		0.2	3.0	µA
I_B	Input Bias Current	Either Input		±0.5	±3.5	µA
e_n	Input Noise Voltage	$f_O = 10kHz$		50		$nV/\sqrt{Hz}$
i_n	Input Noise Current	$f_O = 10kHz$		4.0		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	Either Input		100		kΩ
C_{IN}	Input Capacitance	Either Input		2.0		pF
$V_{IN\ LIM}$	Input Voltage Limit	(Note 4)		1.3		V
	Input Voltage Range		−2.5		+3.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = -2.5V$ to $+3.5V$	60	75		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.375V$ to $\pm 8V$	60	75		dB
V_{OUT}	Output Voltage Swing	$V_S = \pm 5V$, $R_L = 1k$	±3.8	±4.0		V
		$V_S = \pm 8V$, $R_L = 1k$	±6.8	±7.0		
		$V_S = \pm 8V$, $R_L = 100\Omega$	6.4	6.6		
G_E	Gain Error	$V_O = \pm 3V$, $R_L = 1k$		0.1	1.0	%
		$R_L = 100\Omega$		0.1	1.2	
SR	Slew Rate	$V_O = \pm 2V$, $R_L = 300\Omega$, (Note 5, 10)	350	500		V/µs
FPBW	Full Power Bandwidth	$V_O = 6Vp\text{-}p$, (Note 6)	18.5	26.5		MHz
BW	Small Signal Bandwidth			9.0		MHz
t_r, t_f	Rise Time, Fall Time	$A_V = +50$, $V_O = \pm 1.5V$, 20% to 80% (Note 10)	110	160	210	ns
t_{PD}	Propagation Delay	$R_L = 1k$, $V_O = \pm 125mV$, 50% to 50%		15		ns
	Overshoot	$V_O = \pm 50mV$		0		%
t_s	Settling Time	3V Step, 0.1%, (Note 7)		180		ns
Diff A_V	Differential Gain	$R_L = 150\Omega$, $A_V = +2$, (Note 8)		0.2		%
Diff Ph	Differential Phase	$R_L = 150\Omega$, $A_V = +2$, (Note 8)		0.08		Deg. p-p
I_S	Supply Current			35	43	mA
	Shutdown Supply Current	Pin 5 at V^-		1.3	2.0	mA

ELECTRICAL CHARACTERISTICS

$V_S = \pm 5V$, $V_{REF} = 0V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to ground, $R_L = R_{FB1} + R_{FB2} = 1k$ (Note 2), $T_A = 25°C$, $C_L \le 10pF$, pin 5 open circuit, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1193M/C MIN	TYP	MAX	UNITS
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-		20	50	µA
t_{on}	Turn On Time	Pin 5 from V^- to Ground, $R_L = 1k$		300		ns
t_{off}	Turn Off Time	Pin 5 from Ground to V^-, $R_L = 1k$		200		ns

ELECTRICAL CHARACTERISTICS

$V_S+ = +5V$, $V_S- = 0V$, $V_{REF} = +2.5V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to V_{REF}, $R_L = R_{FB1} + R_{FB2} = 1k$ (Note 2), $T_A = 25°C$, $C_L \le 10pF$, pin 5 open circuit, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1193M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Both Inputs, (Note 3)			3.0	15	mV
I_{OS}	Input Offset Current	Either Input			0.2	3.0	µA
I_B	Input Bias Current	Either Input			±0.5	±3.5	µA
	Input Voltage Range			+2.0		+3.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = +2.0V$ to $+3.5V$		55	70		dB
V_{OUT}	Output Voltage Swing	$R_L = 100\Omega$ to Ground	V_{OUT} High	3.6	3.8		V
			V_{OUT} Low		0.25	0.4	
SR	Slew Rate	$V_O = +1V$ to $+3V$			250		V/µs
BW	Small Signal Bandwidth				8.0		MHz
I_S	Supply Current				32	40	mA
	Shutdown Supply Current	Pin 5 at V^-			1.3	2.0	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-			20	50	µA

ELECTRICAL CHARACTERISTICS

$V_S = \pm 5V$, $V_{REF} = 0V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to ground, $R_L = R_{FB2} = 1k$ (Note 2), $T_A = -55°C \le T_A \le 125°C$, $C_L \le 10pF$, pin 5 open circuit, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1193M MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		●		2.0	16	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift		●		20		µV/°C
I_{OS}	Input Offset Current		●		0.8	5.0	µA
I_B	Input Bias Current		●		±1.0	±5.5	µA
	Input Voltage Range		●	−2.5		+3.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = -2.5V$ to $+3.5V$	●	53	70		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.375V$ to $\pm 5.0V$	●	53	70		dB
V_{OUT}	Output Voltage Swing	$R_L = 1k$	●	3.6	4.0		V
		$V_S = \pm 8V$, $R_L = 100\Omega$	●	6.0	6.5		
G_E	Gain Error	$V_O = \pm 3V$, $R_L = 1k$	●		0.2	1.2	%
I_S	Supply Current		●		35	43	mA
	Shutdown Supply Current	Pin 5 at V^-, (Note 9)	●		1.3	2.2	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-	●		20		µA

ELECTRICAL CHARACTERISTICS

$V_S = \pm5V$, $V_{REF} = 0V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to ground, $R_L = R_{FB1} + R_{FB2} = 1k$ (Note 2), $T_A = 0°C \le T_A \le 70°C$, $C_L \le 10pF$, pin 5 open circuit, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1193C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		●		2.0	14	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift		●		20		µV/°C
I_{OS}	Input Offset Current		●		0.2	3.5	µA
I_B	Input Bias Current		●		±0.5	±4.0	µA
	Input Voltage Range		●	−2.5		+3.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = -2.5V$ to $+3.5V$	●	55	70		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.375V$ to $\pm5.0V$	●	55	70		dB
V_{OUT}	Output Voltage Swing	$R_L = 1k$	●	3.7	4.0		V
		$R_L = 100\Omega$	●	6.2	6.6		
G_E	Gain Error	$V_O = \pm3V$, $R_L = 1k$	●		0.2	1.2	%
I_S	Supply Current		●		35	43	mA
	Shutdown Supply Current	Pin 5 at V^-, (Note 9)	●		1.3	2.1	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-	●		20		µA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.

Note 2: When $R_L = 1k$ is specified, the load resistor is $R_{FB1} + R_{FB2}$, but when $R_L = 100\Omega$ is specified, then an additional 100Ω is added to the output.

Note 3: V_{OS} measured at the output (pin 6) is the contribution from both input pair, and is input referred.

Note 4: $V_{IN\ LIM}$ is the maximum voltage between $-V_{IN}$ and $+V_{IN}$ (pin 2 and pin 3) for which the output can respond.

Note 5: Slew rate is measured between ±2V on the output, with a ±1V input step, $A_V = +3$.

Note 6: Full power bandwidth is calculated from the slew rate measurement: $FPBW = SR/2\pi Vp$.

Note 7: Settling time measurement techniques are shown in "Take the Guesswork Out of Settling Time Measurements," EDN, September 19, 1985.

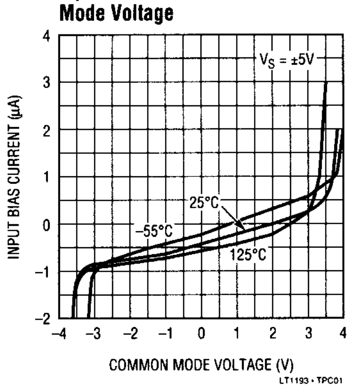
Note 8: NTSC (3.58MHz).

Note 9: See Applications section for shutdown at elevated temperatures. Do not operate the shutdown above $T_J > 125°C$.

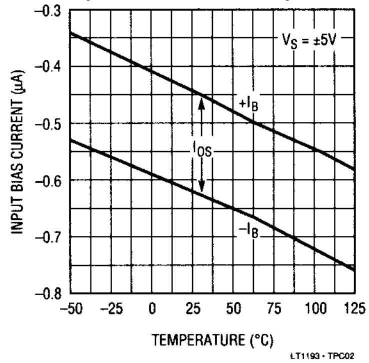
Note 10: AC parameters are 100% tested on the ceramic and plastic DIP packaged parts (J and N suffix) and are sample tested on every lot of the SO packaged parts (S suffix).

TYPICAL PERFORMANCE CHARACTERISTICS

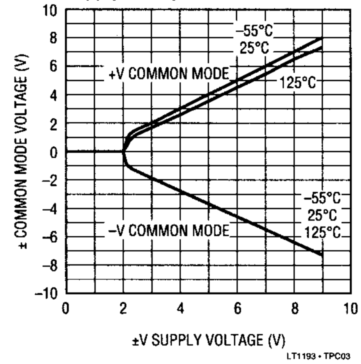
Input Bias Current vs Common Mode Voltage



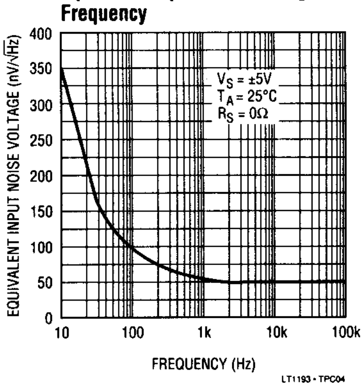
Input Bias Current vs Temperature



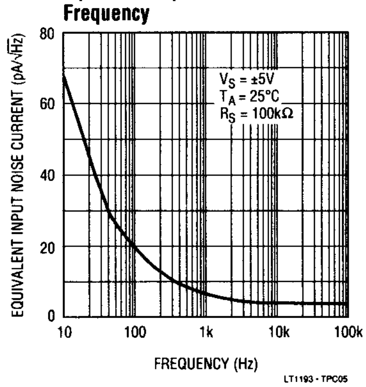
Common Mode Voltage vs Supply Voltage



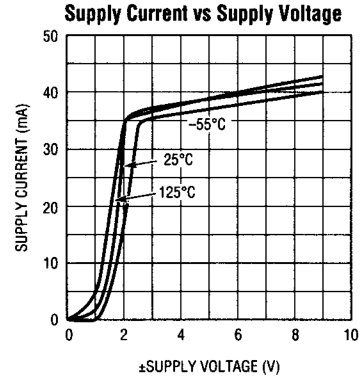
Equivalent Input Noise Voltage vs Frequency



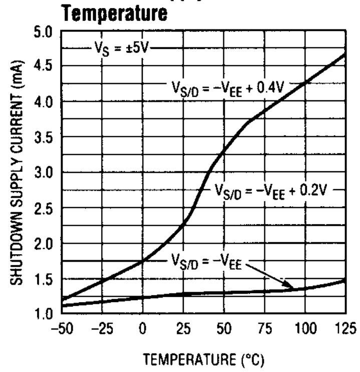
Equivalent Input Noise Current vs Frequency



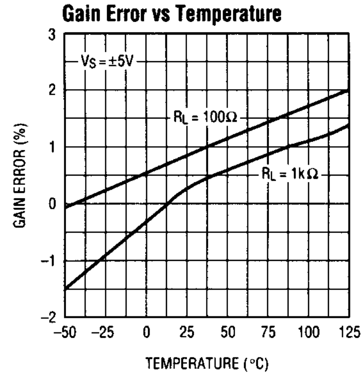
Supply Current vs Supply Voltage



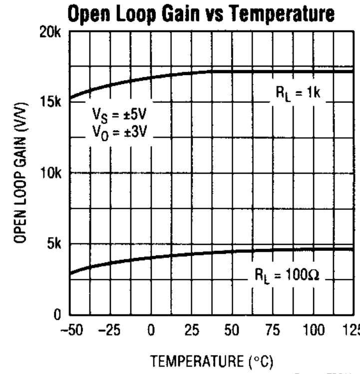
Shutdown Supply Current vs Temperature



Gain Error vs Temperature

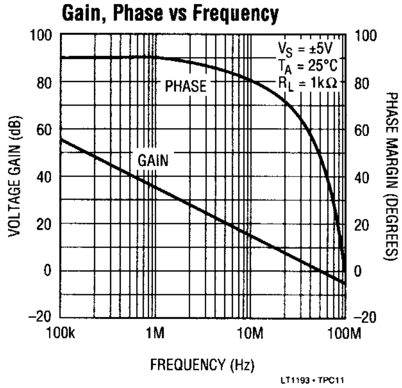


Open Loop Gain vs Temperature

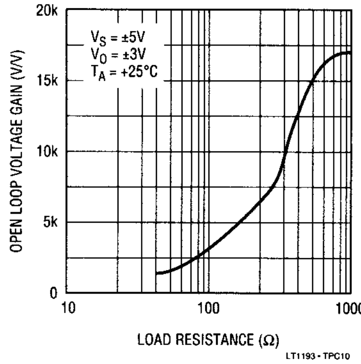


TYPICAL PERFORMANCE CHARACTERISTICS

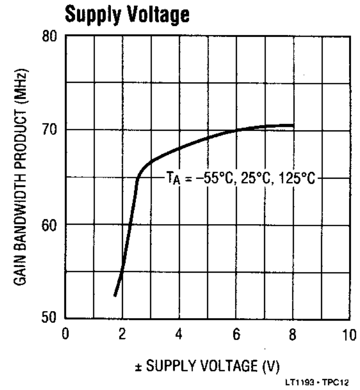
Gain, Phase vs Frequency



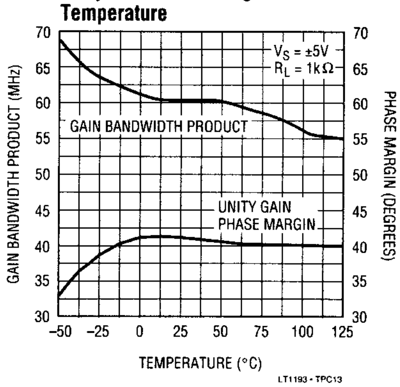
Open Loop Voltage Gain vs Load Resistance



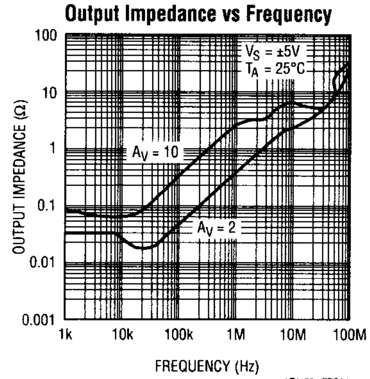
Gain Bandwidth Product vs Supply Voltage



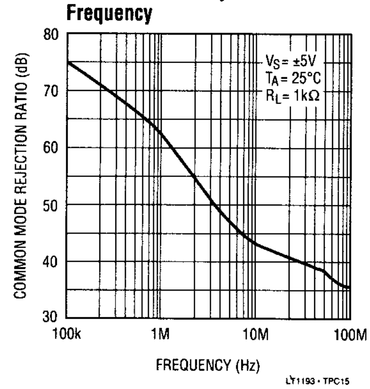
Gain Bandwidth Product and Unity Gain Phase Margin vs Temperature



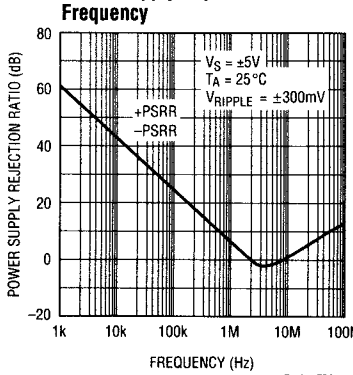
Output Impedance vs Frequency



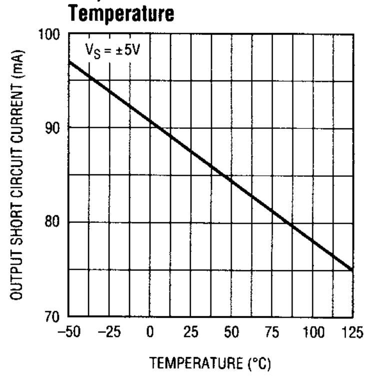
Common Mode Rejection Ratio vs Frequency



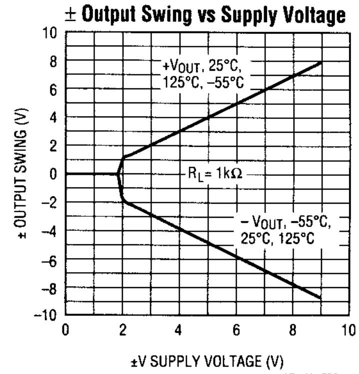
Power Supply Rejection Ratio vs Frequency



Output Short Circuit Current vs Temperature

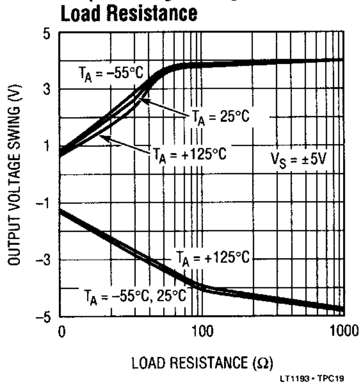


± Output Swing vs Supply Voltage

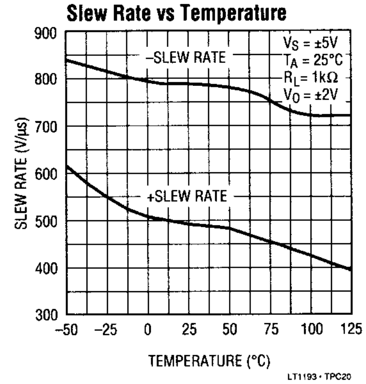


TYPICAL PERFORMANCE CHARACTERISTICS

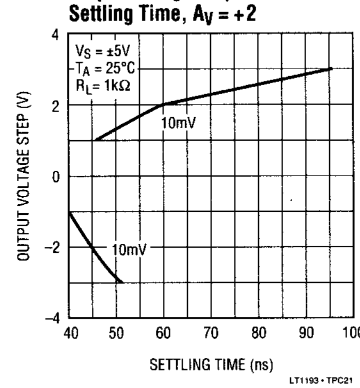
Output Voltage Swing vs Load Resistance



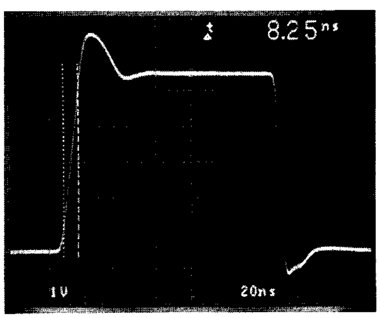
Slew Rate vs Temperature



Output Voltage Step vs Settling Time, A_V = +2



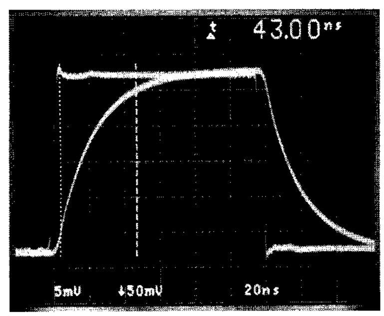
Large Signal Transient Response



A_V = +2, R_L = 150Ω, R_{FB} = 300Ω, R_G = 300Ω

LT1193 • TPC22

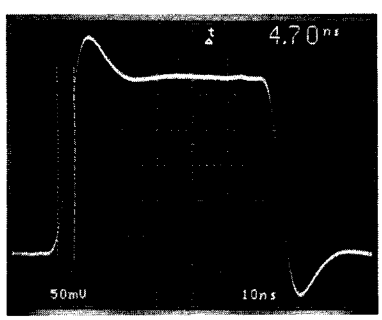
Small Signal Transient Response



A_V = −10, SMALL SIGNAL RISE TIME = 43ns

LT1193 • TPC23

Small Signal Transient Response

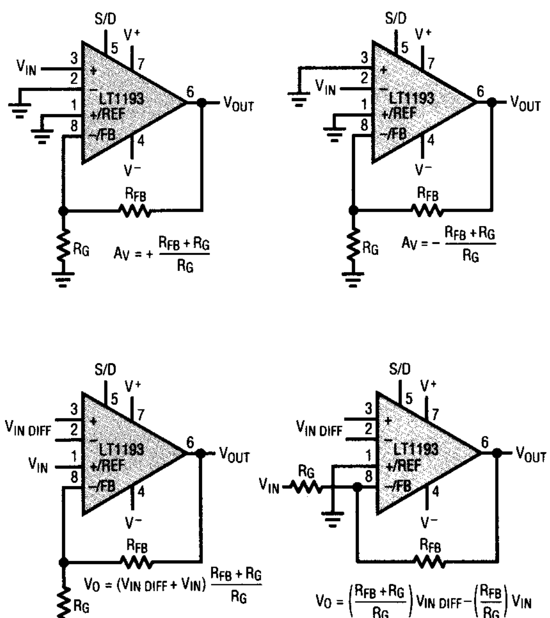


A_V = +2, R_{FB} = 300Ω, R_G = 300Ω, OVERSHOOT = 25%,
RISE TIME = 4.7ns

LT1193 • TPC24

APPLICATIONS INFORMATION

The LT1193 is a video difference amplifier which has two uncommitted high input impedance (+) and (–) inputs. The amplifier has one set of inputs which can be used for reference and feedback. Additionally, this set of inputs give gain adjust, and DC control to the differential amplifier. The voltage gain of the LT1193 is set like a conventional operational amplifier. Feedback is applied to pin 8, and it is optimized for gains of 2 or greater. The amplifier can be operated single-ended by connecting either the (+) or (–) inputs to the +/Reference pin 1. The voltage gain is set by the resistors: $(R_{FB} + R_G)/R_G$.

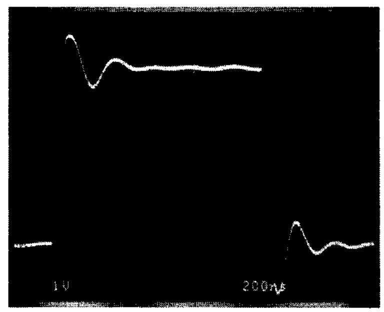


The primary usefulness of the LT1193 is in converting high speed differential signals to a single-ended output. The amplifier has common mode rejection beyond 50MHz, and a full power bandwidth of 40MHz at 4Vp-p. Like the single-ended case, the differential voltage gain is set by the external resistors: $(R_{FB} + R_G)/R_G$. The maximum input differential signal for which the output will respond is approximately ±1.3V.

Power Supply Bypassing

The LT1193 is quite tolerant of power supply bypassing. In some applications a 0.1µF ceramic disc capacitor placed 1/2 inch from the amplifier is all that is required. A scope photo of the amplifier output with no supply bypassing is used to demonstrate this bypassing tolerance, $R_L = 1k\Omega$.

No Supply Bypass Capacitors

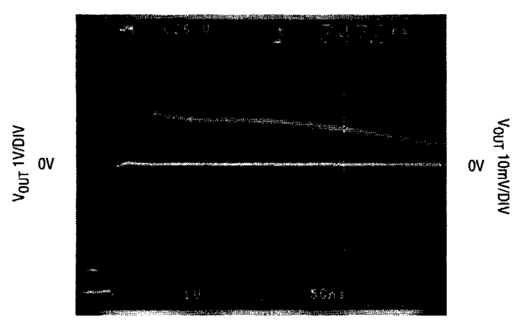


$A_V = +10$, IN DEMO BOARD, $R_L = 1k\Omega$

LT1193 • TA04

In many applications and those requiring good settling time it is important to use multiple bypass capacitors. A 0.1µF ceramic disc in parallel with a 4.7µF tantalum is recommended. Two oscilloscope photos with different bypass conditions are used to illustrate the settling time characteristics of the amplifier. Note that although the output waveform looks acceptable at 1V/div, when

Settling Time Poor Bypass

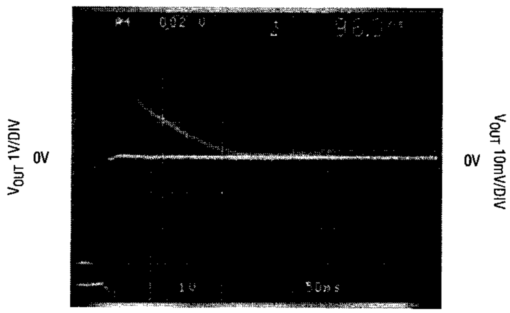


SETTLING TIME TO 10mV, $A_V = 2$
SUPPLY BYPASS CAPACITORS = 0.1µF

LT1193 • TA05

APPLICATIONS INFORMATION

Settling Time Good Bypass



SETTLING TIME TO 10mV, A_V = 2
SUPPLY BYPASS CAPACITORS = 0.1µF + 4.7µF TANTALUM

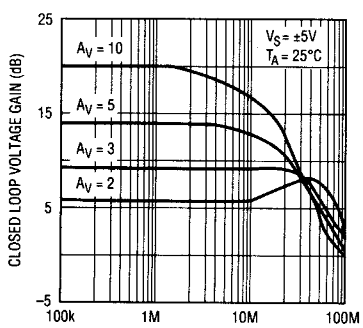
LT1193 • TA06

amplified to 10mV/div the settling time to 10mV is 347ns for the 0.1µF bypass; the time drops to 96ns with multiple bypass capacitors.

Operating With Low Closed Loop Gains

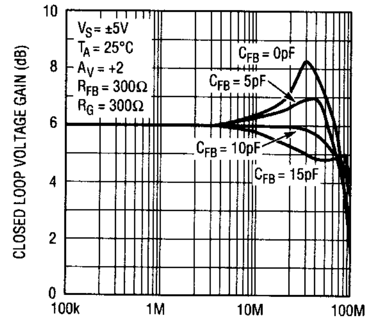
The LT1193 has been optimized for closed loop gains of 2 or greater; the frequency response illustrates the obtainable closed loop bandwidths. For a closed loop gain of 2 the response peaks about +2dB. Peaking can be minimized by keeping the feedback elements below 1kΩ, and can be eliminated by placing a capacitor across the feedback resistor, (feedback zero). This peaking shows up as time domain overshoot of about 40%. With the feedback capacitor it is eliminated.

Closed Loop Voltage Gain vs Frequency



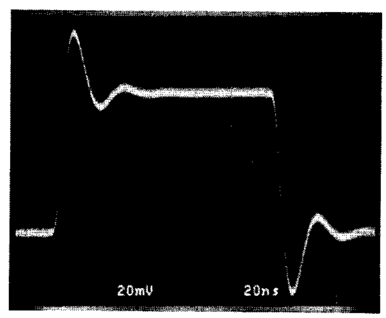
LT1193 • TA07

Closed Loop Voltage Gain vs Frequency



LT1193 • TA08

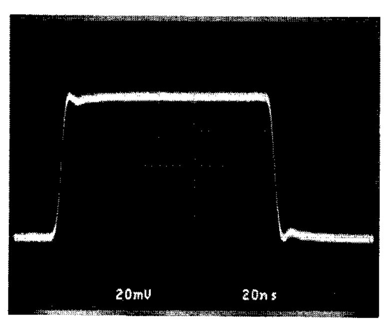
Small Signal Transient Response



A_V = +2, OVERSHOOT = 40%, R_{FB} = 1k, R_G = 1k

LT1193 • TA09

Small Signal Transient Response



A_V = +2, WITH 8pF FEEDBACK CAPACITOR
RISE TIME = 3.75ns, R_{FB} = 1k, R_G = 1k

LT1193 • TA10

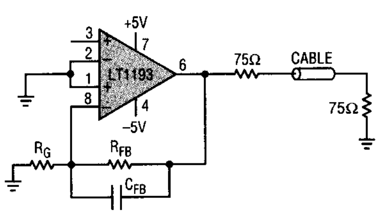
APPLICATIONS INFORMATION

Cable Terminations

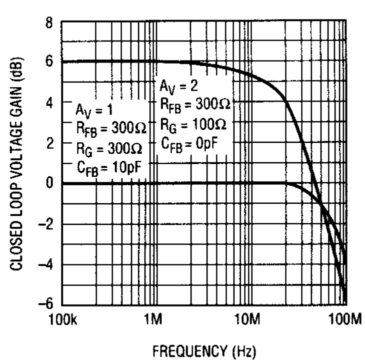
The LT1193 video difference amplifier has been optimized as a low cost cable driver. The ±50mA guaranteed output current enables the LT1193 to easily deliver 7.5Vp-p into 100Ω, while operating on ±5V supplies, and gains >3. On a single 5V supply the LT1193 can swing 2.6Vp-p for gains ≥2.

When driving a cable it is important to terminate the cable to avoid unwanted reflections. This can be done in one of two ways: single termination or double termination. With single termination, the cable must be terminated at the receiving end (75Ω to ground) to absorb unwanted energy. The best performance can be obtained by double termination (75Ω in series with the output of the amplifier, and 75Ω to ground at the other end of the cable). This termination is preferred because reflected energy is absorbed at each end of the cable. When using the double termination technique it is important to note that the signal is attenuated by a factor of 2, or 6dB. The cable driver has a –3dB bandwidth of 80MHz while driving a 150Ω load.

Double Terminated Cable Driver



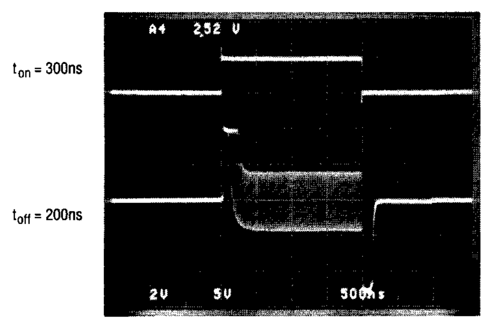
Closed Loop Voltage Gain vs Frequency



Using the Shutdown Feature

The LT1193 has a unique feature that allows the amplifier to be shutdown for conserving power, or for multiplexing several amplifiers onto a common cable. The amplifier will shutdown by taking pin 5 to V^-. In shutdown, the amplifier dissipates 15mW while maintaining a true high impedance output state of 15kΩ in parallel with the feedback resistors. The amplifiers may be connected inverting, non-inverting or differential for MUX applications. When the output is loaded with as little as 1kΩ from the amplifier's feedback resistors, the amplifier shuts off in 200ns. This shutoff can be under the control of HC CMOS operating between 0V and –5V.

Output Shutdown



1MHz SINE WAVE GATED OFF WITH SHUTDOWN PIN, $A_V = +3$, $R_{FB} = 1k\Omega$, $R_G = 500\Omega$

LT1193 • TA12

The ability to maintain shutoff is shown on the curve Shutdown Supply Current vs Temperature in the Typical Performance Characteristics section. At very high elevated temperatures it is important to hold the shutdown pin close to the negative supply to keep the supply current from increasing.

APPLICATIONS INFORMATION

Murphy Circuits

There are several precautions the user should take when using the LT1193 in order to realize its full capability. Although the LT1193 can drive a 30pF in gains as low as 2, isolating the capacitance with 10Ω can be helpful. Precautions primarily have to do with driving large capacitive loads.

Other precautions include:

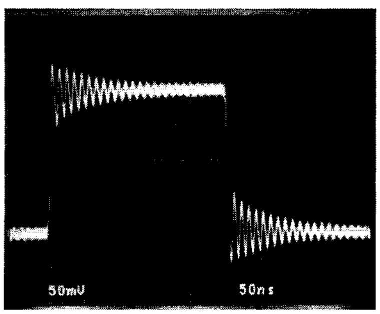
1. Use a ground plane (see Design Note 50, High Frequency Amplifier Evaluation Board).

2. Do not use high source impedances. The input capacitance of 2pF, and R_S = 10kΩ for instance, will give an 8MHz –3dB bandwidth.

3. PC board socket may reduce stability.

4. A feedback resistor of 1kΩ or lower reduces the effects of stray capacitance at the inverting input. (For instance, closed loop gain of ±2 can use R_{FB} = 300Ω and R_G = 300Ω.)

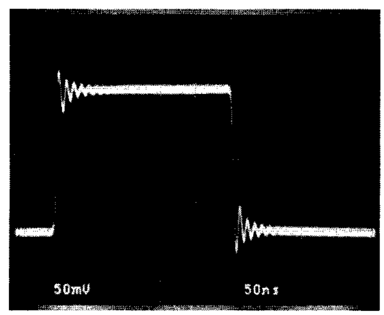
Driving Capacitive Load



A_V = +2, IN DEMO BOARD, C_L = 30pF
R_{FB} = 1k, R_G = 1k

LT1193 • TA14

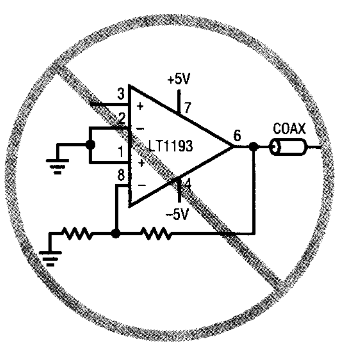
Driving Capacitive Load



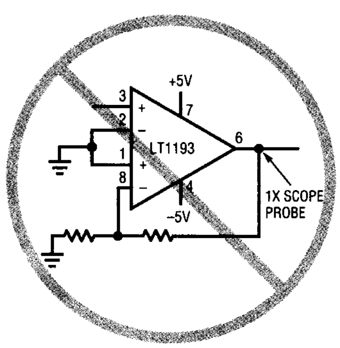
A_V = +2, IN DEMO BOARD, C_L = 30pF
WITH 10Ω ISOLATING RESISTOR

LT1193 • TA15

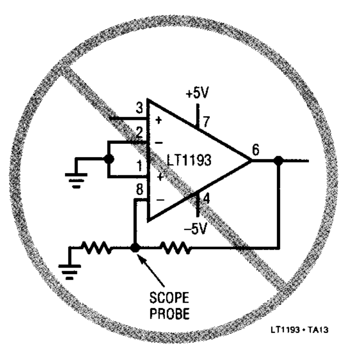
Murphy Circuits



An Unterminated Cable Is a Large Capacitive Load



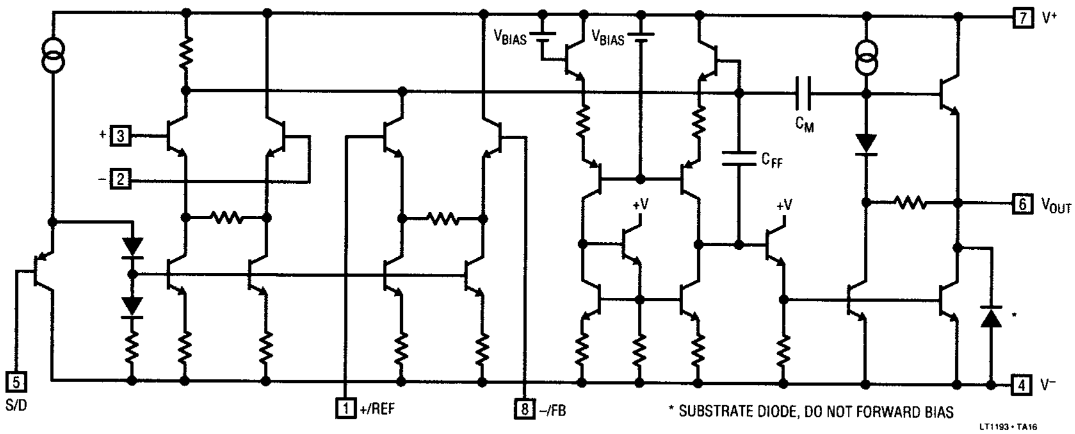
A 1X Scope Probe Is a Large Capacitive Load



LT1193 • TA13

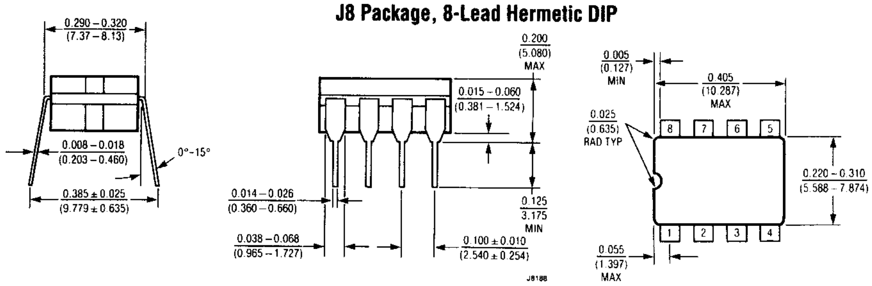
A Scope Probe on the Inverting Input Reduces Phase Margin

SIMPLIFIED SCHEMATIC



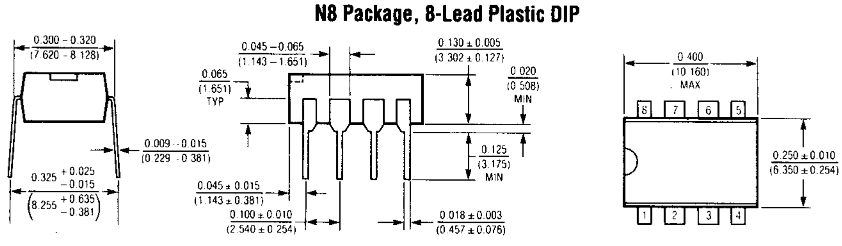
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J8 Package, 8-Lead Hermetic DIP



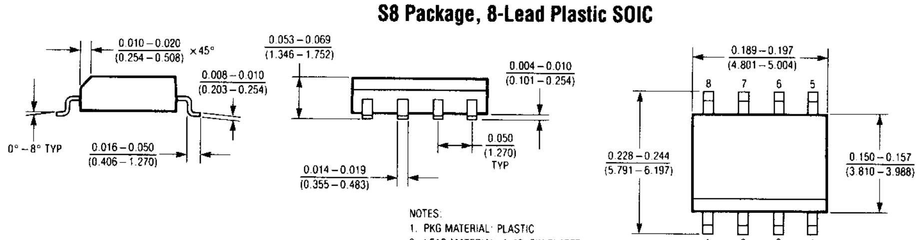
T_J MAX	θ_{JA}
150°C	100°C/W

N8 Package, 8-Lead Plastic DIP



T_J MAX	θ_{JA}
150°C	100°C/W

S8 Package, 8-Lead Plastic SOIC



NOTES:
1. PKG MATERIAL: PLASTIC
2. LEAD MATERIAL: A-42, TIN PLATED

S8188

T_J MAX	θ_{JA}
150°C	150°C/W

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7487
(408) 432-1900 • FAX: (408) 434-0507 • TELEX: 499-3977

BA/GP 1191 10K REV 0