

December 1995

54AC/74AC163 • 54ACT/74ACT163 Synchronous Presettable Binary Counter

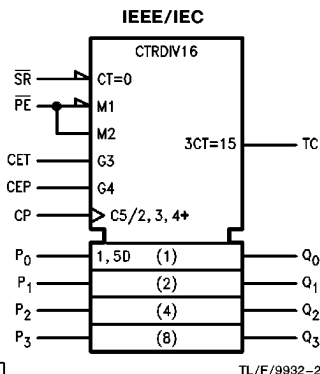
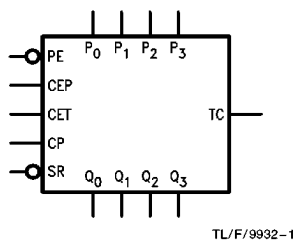
General Description

The 'AC/'ACT163 are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'AC/'ACT163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

Features

- I_{CC} reduced by 50%
- Synchronous counting and loading
- High-speed synchronous expansion
- Typical count rate of 125 MHz
- Outputs source/sink 24 mA
- 'ACT163 has TTL-compatible inputs
- Standard Military Drawing (SMD)
 - 'AC163: 5962-89582
 - 'ACT163: 5962-90575

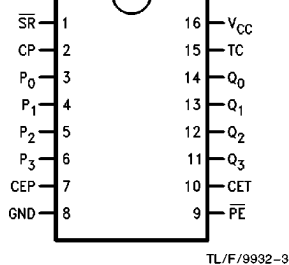
Logic Symbols



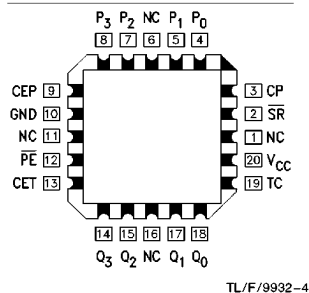
Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
SR	Synchronous Reset Input
P ₀ -P ₃	Parallel Data Inputs
PE	Parallel Enable Input
Q ₀ -Q ₃	Flip-Flop Outputs
TC	Terminal Count Output

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC



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Functional Description

The 'AC/ACT163 counts in modulo-16 binary sequence. From state 15 (HHHH) it increments to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: synchronous reset, parallel load, count-up and hold. Four control inputs—Synchronous Reset ($\overline{SR}$), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{SR}$ HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'AC/ACT163 uses D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 15. To implement synchronous multi-stage counters, the TC outputs can be used with the CEP and CET inputs in two different ways.

Figure 1 shows the connections for simple ripple carry, in which the clock period must be longer than the CP to TC delay of the first stage, plus the cumulative CET to TC delays of the intermediate stages, plus the $\overline{CET}$ to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in Figure 2 are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle takes 16 clocks to complete,

there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to TC delay of the first stage plus the $\overline{CET}$ to CP setup time of the last stage. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters.

$$\text{Logic Equations: Count Enable} = \text{CEP} \cdot \text{CET} \cdot \overline{\text{PE}}$$

$$\text{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \text{CET}$$

Mode Select Table

$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge ($\nearrow$)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram

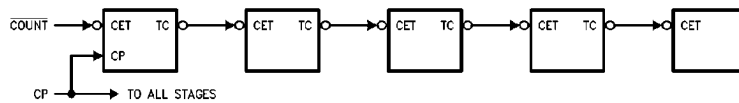
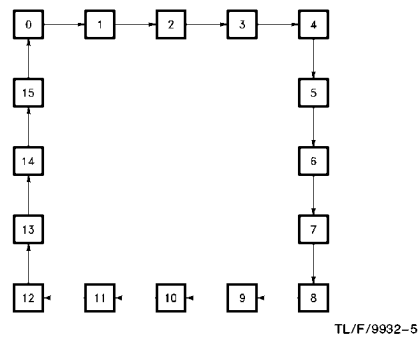


FIGURE 1

TL/F/9932-8

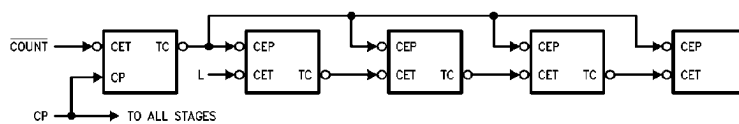
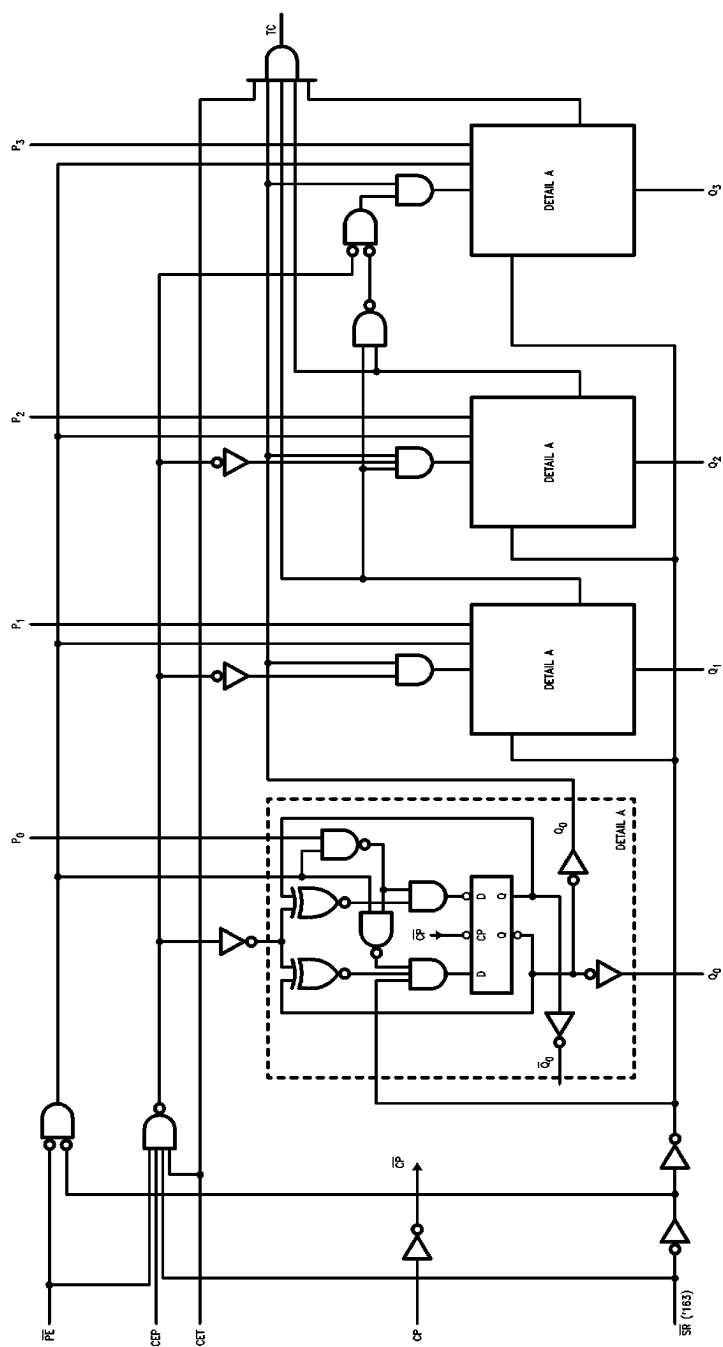


FIGURE 2

TL/F/9932-9

Block Diagram



TL/F/9832-6

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V _{CC} (V)	74AC		54AC	74AC	Units	Conditions
			T _A = +25°C		T _A = −55°C to +125°C	T _A = −40°C to +85°C		
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I _{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA
		4.5		3.86	3.7	3.76		
		5.5		4.86	4.7	4.76		
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
		4.5		0.36	0.50	0.44		
		5.5		0.36	0.50	0.44		
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V _I = V _{CC} , GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	74AC		54AC	74AC	Units	Conditions
			T _A = +25°C		T _A = −55°C to +125°C	T _A = −40°C to +85°C		
			Typ	Guaranteed Limits				
I _{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5			−50	−75	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	V _{IN} = V _{CC} or GND

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V _{CC} (V)	74ACT		54ACT	74ACT	Units	Conditions
			T _A = +25°C		T _A = −55°C to +125°C	T _A = −40°C to +85°C		
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V _I = V _{CC} , GND
I _{CC} T	Maximum I _{CC} /Input	5.5	0.6		1.6	1.5	mA	V _I = V _{CC} − 2.1V
I _{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5			−50	−75	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} * (V)	74AC			54AC		74AC		Units
			T _A = +25°C C _L = 50 pF			T _A = −55°C to +125°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
t _{max}	Maximum Clock Frequency	3.3 5.0	70 110	95 140		55 90		60 95		MHz
t _{PLH}	Propagation Delay, CP to Q _n (PE Input HIGH or LOW)	3.3 5.0	2.0 1.5	7.5 5.5	12.5 9.0	1.0 1.5	13.5 9.5	1.5 1.0	13.5 9.5	ns
t _{PHL}	Propagation Delay, CP to Q _n (PE Input HIGH or LOW)	3.3 5.0	1.5 1.5	8.5 6.0	12.0 9.5	1.0 1.5	12.5 9.5	1.5 1.5	13.0 10.0	ns
t _{PLH}	Propagation Delay CP to TC	3.3 5.0	3.0 2.0	9.5 7.0	15.0 10.5	1.0 1.5	16.5 11.0	2.5 1.5	16.5 11.5	ns
t _{PHL}	Propagation Delay CP to TC	3.3 5.0	3.5 2.0	11.0 8.0	14.0 11.0	1.0 1.5	15.0 11.0	2.5 2.0	15.5 11.5	ns
t _{PLH}	Propagation Delay CET to TC	3.3 5.0	2.0 1.5	7.5 5.5	9.5 6.5	1.0 1.5	11.0 7.5	1.5 1.0	11.0 7.5	ns
t _{PHL}	Propagation Delay CET to TC	3.3 5.0	2.5 2.0	8.5 6.0	11.0 8.5	1.0 1.5	12.0 9.0	2.0 1.5	12.5 9.5	ns

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V _{CC} * (V)	74AC		54AC		74AC		Units
			T _A = +25°C C _L = 50 pF		T _A = −55°C to +125°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum					
t _s	Setup Time, HIGH or LOW P _n to CP	3.3 5.0	5.5 4.0	13.5 8.5	17.0 11.0	16.0 10.5	ns		
t _h	Hold Time, HIGH or LOW P _n to CP	3.3 5.0	−7.0 −5.0	−1.0 0	−0.5 0	−0.5 0	ns		
t _s	Setup Time, HIGH or LOW SR to CP	3.3 5.0	5.5 4.0	14.0 9.5	17.0 12.0	16.5 11.0	ns		
t _h	Hold Time, HIGH or LOW SR to CP	3.3 5.0	−7.5 −5.5	−1.0 −0.5	−0.5 0	−0.5 0	ns		
t _s	Setup Time, HIGH or LOW PE to CP	3.3 5.0	5.5 4.0	11.5 7.5	16.0 9.5	14.0 8.5	ns		
t _h	Hold Time, HIGH or LOW PE to CP	3.3 5.0	−7.5 −5.0	−1.0 −0.5	−0.5 0	−0.5 0	ns		
t _s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.5 2.5	6.0 4.5	8.0 5.5	7.0 5.0	ns		
t _h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	−4.5 −3.0	0 0	0 0.5	0 0.5	ns		
t _w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	3.0 2.0	3.5 2.5	5.0 5.0	4.0 3.0	ns		
t _w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	3.0 2.0	4.0 3.0	5.0 5.0	4.5 3.5	ns		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

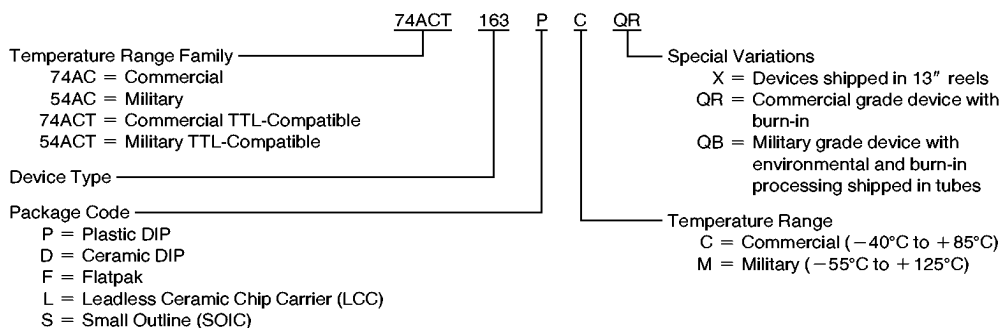
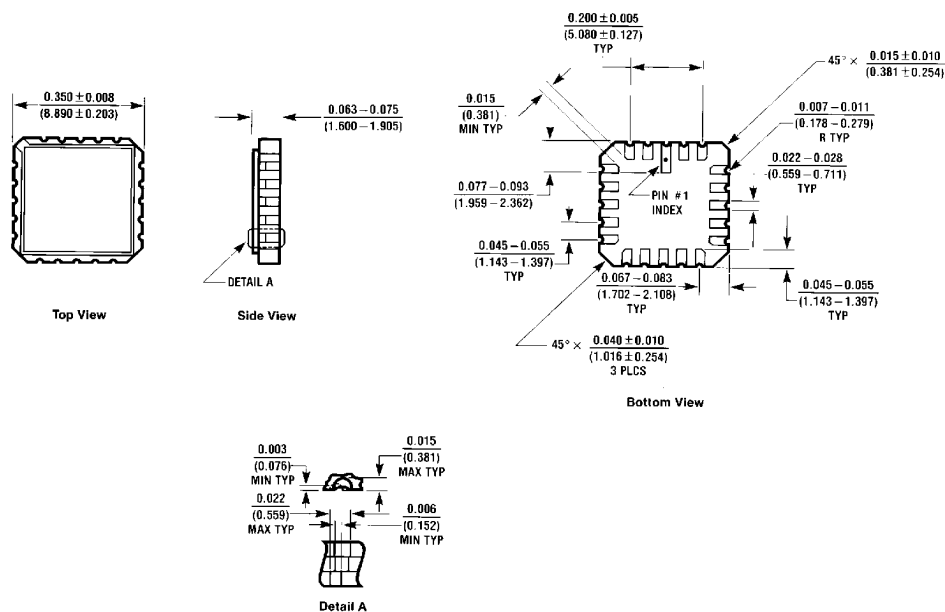
AC Electrical Characteristics										
Symbol	Parameter	V _{CC} * (V)	74ACT			54ACT		74ACT		Units
			T _A = +25°C C _L = 50 pF			T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	5.0	120	140		90		10.5		MHz
t _{PLH}	Propagation Delay, CP to Q _n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	5.5	10.0	1.5	10.5	1.5	11.0	ns
t _{PHL}	Propagation Delay, CP to Q _n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	6.0	11.0	1.5	10.5	1.5	12.0	ns
t _{PLH}	Propagation Delay CP to TC	5.0	2.5	7.0	11.5	1.5	12.5	2.0	13.5	ns
t _{PHL}	Propagation Delay CP to TC	5.0	3.0	8.0	13.5	1.5	13.0	2.0	15.0	ns
t _{PLH}	Propagation Delay CET to TC	5.0	2.0	5.5	9.0	1.5	9.5	1.5	10.5	ns
t _{PHL}	Propagation Delay CET to TC	5.0	2.0	6.0	10.0	1.5	9.5	2.0	11.0	ns
*Voltage Range 5.0 is 5.0V ±0.5V										
AC Operating Requirements										
Symbol	Parameter	V _{CC} * (V)	74ACT		54ACT		74ACT		Units	
			T _A = +25°C C _L = 50 pF		T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum						
t _s	Setup Time, HIGH or LOW P _n to CP	5.0	4.0	10.0		13.5		12.0	ns	
t _h	Hold Time, HIGH or LOW P _n to CP	5.0	-5.0	0.5		0.5		0.5	ns	
t _s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	5.0	4.0	10.0		13.5		11.5	ns	
t _h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	5.0	-5.5	-0.5		0.0		-0.5	ns	
t _s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	5.0	4.0	8.5		11.5		10.5	ns	
t _h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	5.0	-5.5	-0.5		0.0		0	ns	
t _s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5	5.5		7.0		6.5	ns	
t _h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	-3.0	0		0.5		0.5	ns	
t _w	Clock Pulse Width (Load) HIGH or LOW	5.0	2.0	3.5		5.0		3.5	ns	
t _w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	3.5		5.0		3.5	ns	
*Voltage Range 5.0 is 5.0V ±0.5V										

Capacitance

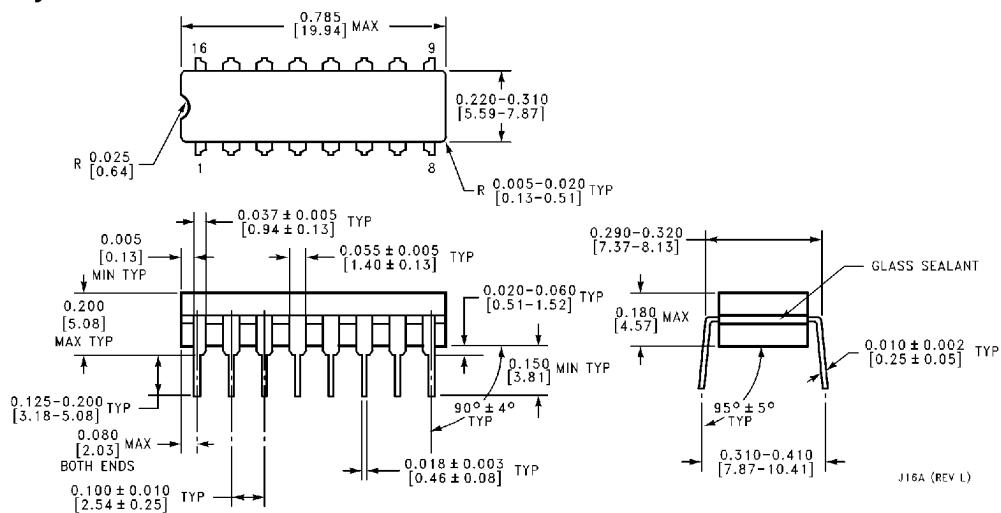
Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	45.0	pF	V _{CC} = 5.0V

Ordering Information

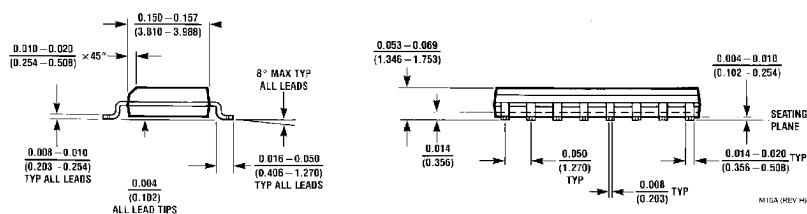
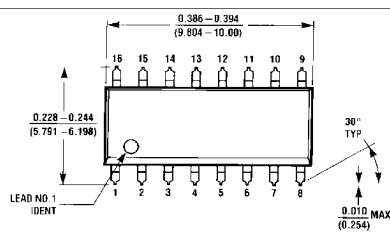
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

**Physical Dimensions** inches (millimeters)

**20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A**

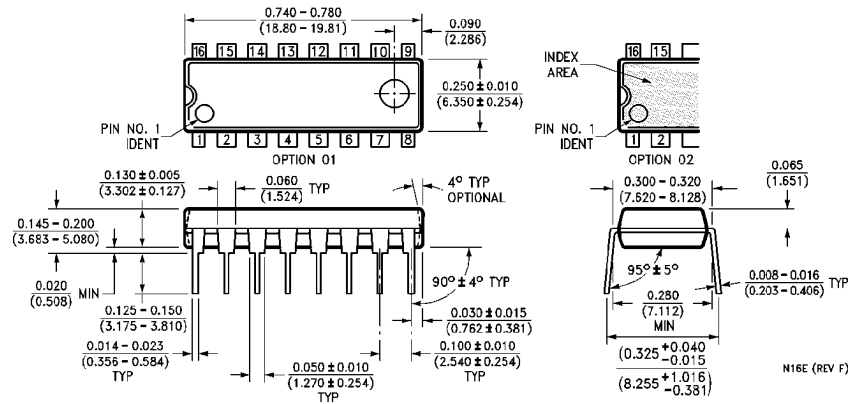
Physical Dimensions inches (millimeters) (Continued)

16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

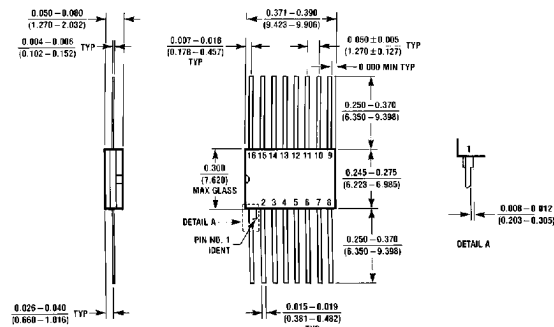


16-Lead Small Outline Integrated Circuit (S)
NS Package Number M16A

Physical Dimensions inches (millimeters) (Continued)



16-Lead Plastic Dual-In-Line Package (P)
NS Package Number N16E



16-Lead Ceramic Flatpak (F)
NS Package Number W16A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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