19-4994; Rev 0; 10/09

EVALUATION KIT AVAILABLE

76V, APD, Bias Output Stage with Current Monitoring

General Description

The DS1842A integrates the discrete high-voltage components necessary for avalanche photodiode (APD) bias and monitor applications. A switch FET and precision voltage-divider network are used in conjunction with an external DC-DC controller to create a boost DC-DC converter. A current clamp limits current through the APD and also features an external shutdown. The precision voltage-divider network is provided for precise control of the APD bias voltage. The device also includes a dual current mirror to monitor the APD current.

Applications

APD Biasing

GPON ONU and OLT

Features

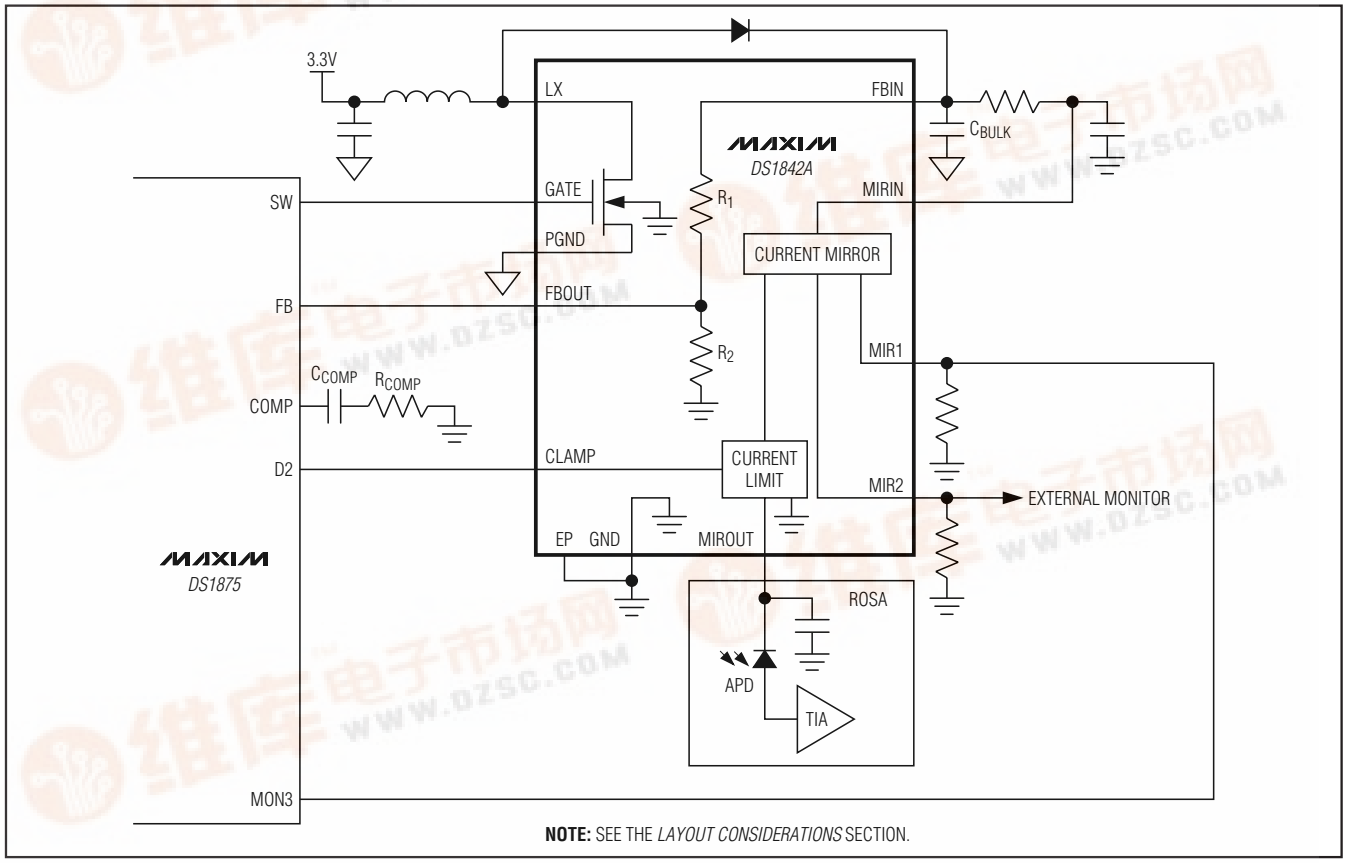
- ♦ 76V Maximum Boost Voltage
- ♦ Switch FET
- ♦ Current Monitor with a Wide 1µA to 2mA Range, Fast 50ns Time Constant, and 10:1 and 5:1 Ratio
- ♦ 2mA Current Clamp with External Shutdown
- ♦ Precision Voltage Feedback
- ♦ Multiple External Filtering Options
- ♦ 3mm x 3mm, 14-Pin TDFN Package with Exposed Pad

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1842AN+	-40°C to +85°C	14 TDFN-EP*
DS1842AN+T&R	-40°C to +85°C	14 TDFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.
**EP = Exposed pad.*

Typical Application Circuit



NOTE: SEE THE *LAYOUT CONSIDERATIONS* SECTION.

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on GATE and CLAMP Relative to GND .....-0.3V to +12V
Voltage Range on MIRIN, MIROUT, FBIN MIR1, and MIR2 Relative to GND .....-0.3V to +80V
Voltage Range on FBOUT Relative to GND .....-0.3V to +6.0V
Voltage Range on LX Relative to GND .....-0.3V to +85V
Operating Junction Temperature Range .....-40°C to +150°C
Storage Temperature Range .....-55°C to +135°C
Soldering Temperature .....Refer to the IPC JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switching Frequency	f_{SW}		0		1.2	MHz
FET Capacitance	C_{GATE}	V_{GS} = 0V, V_{DS} = 25V		40		pF
	C_{LX}	f_{SW} = 1MHz		90		
FET Gate Resistance	R_G			22		Ω
FET On-Resistance	R_{DSON}	V_{GS} = 3V, I_D = 170mA		1	2	Ω
		V_{GS} = 10V, I_D = 170mA		0.75	1.4	
GATE Voltage	V_{GS}		0		11	V
Switching Current	I_{LX}	Duty cycle = 10%, f_{SW} = 100kHz			680	mA
LX Voltage	V_{LX}				80	V
LX Leakage	$I_{IL(LX)}$	V_{GATE} = 0V, V_{LX} = 76V	-1		+1	µA
CLAMP Voltage	V_{CLAMP}		0		11	V
CLAMP Threshold	V_{CLT}		1.25	1.8	2.35	V
Maximum MIROUT Current	I_{MIROUT}	CLAMP = low	1.8	2.75	3.85	mA
		CLAMP = high			10	µA
MIR1 to MIROUT Ratio	K_{MIR1}	15V < V_{MIRIN} < 76V, I_{MIROUT} > 1µA	0.096	0.100	0.104	A/A
MIR2 to MIROUT Ratio	K_{MIR2}	15V < V_{MIRIN} < 76V, I_{MIROUT} > 1µA	0.192	0.200	0.208	A/A
MIR1, MIR2 Rise Time (20%/80%)	t_{RC}	(Note 1)		30		ns
Shutdown Temperature	T_{SHDN}	(Note 2)		+150		°C
Hysteresis Temperature	T_{HYS}	(Note 2)		5		°C
Leakage on GATE and CLAMP	I_{IL}		-1		+1	µA
Resistor-Divider Ratio (R_1/R_2)	K_R	T_A = +25°C, V_{FBIN} = 76V	59.5		60.25	
Resistor-Divider Tempco				±50		ppm/°C
Resistor-Divider End-to-End Resistance	R_{RES}	T_A = +25°C, V_{FBIN} = 76V	308	385	481	kΩ

Note 1: Rising MIROUT transition from 10µA to 1mA; V_{MIRIN} = 40V, 2.5kΩ load.
Note 2: Not production tested. Guaranteed by design.

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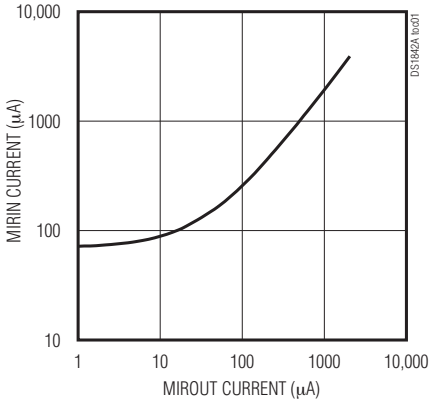
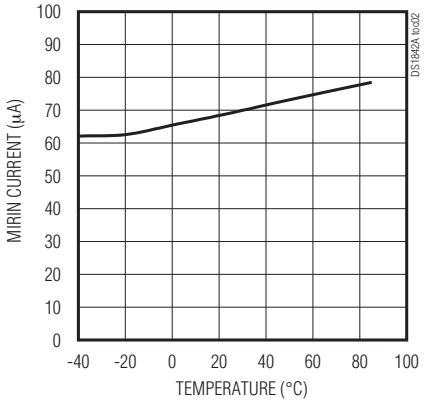
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

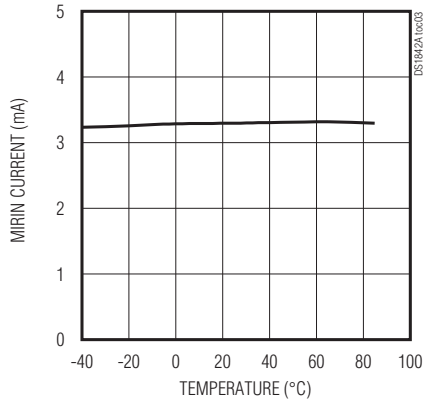
MIRIN CURRENT vs. MIROUT CURRENT
(V_{MIRIN} = 40V)



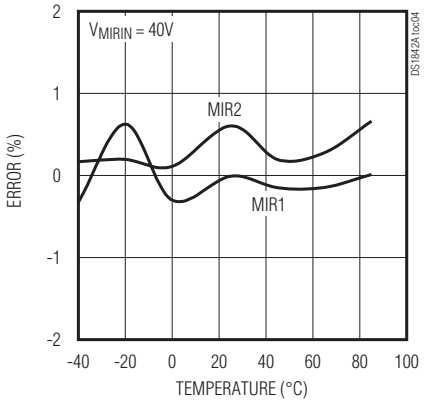
MIRIN CURRENT vs. TEMPERATURE
(V_{MIRIN} = 40V, I_{MIROUT} = 250nA)



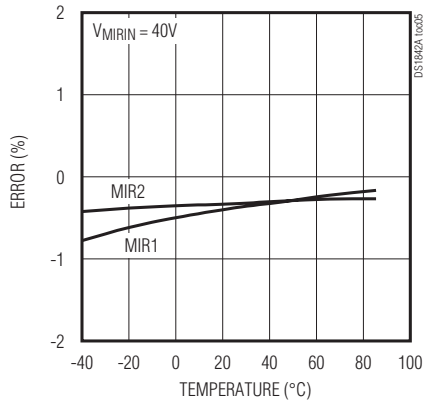
MIRIN CURRENT vs. TEMPERATURE
(V_{MIRIN} = 40V, I_{MIROUT} = 2mA)



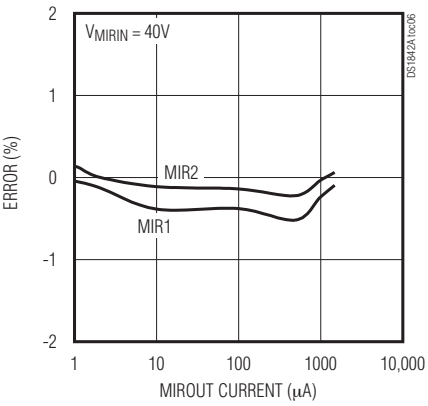
MIR ERROR vs. TEMPERATURE
(I_{MIROUT} = 1µA)



MIR ERROR vs. TEMPERATURE
(I_{MIROUT} = 1mA)



MIR ERROR vs. MIROUT CURRENT

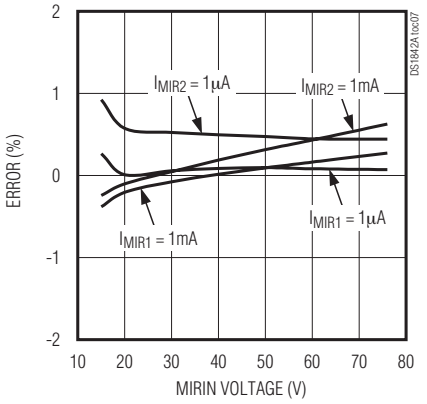


76V, APD, Bias Output Stage with Current Monitoring

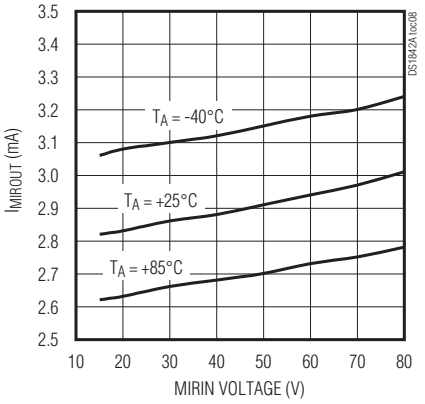
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

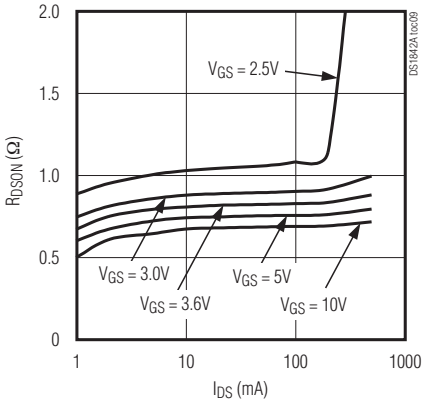
MIR ERROR vs. MIRIN VOLTAGE



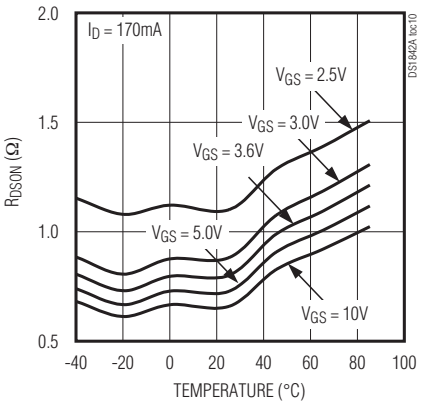
MIROUT CLAMP CURRENT vs. MIRIN VOLTAGE



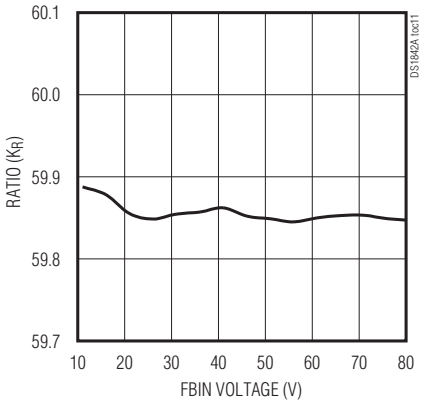
FET ON-RESISTANCE vs. DRAIN CURRENT



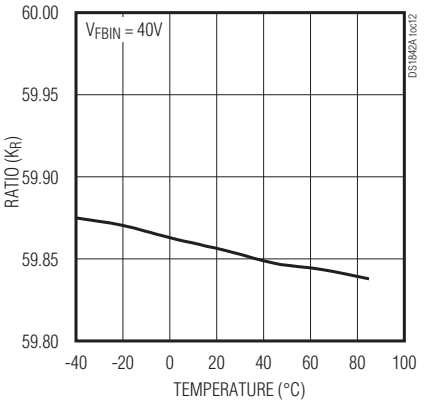
FET ON-RESISTANCE vs. TEMPERATURE



RESISTOR-DIVIDER RATIO vs. FBIN VOLTAGE

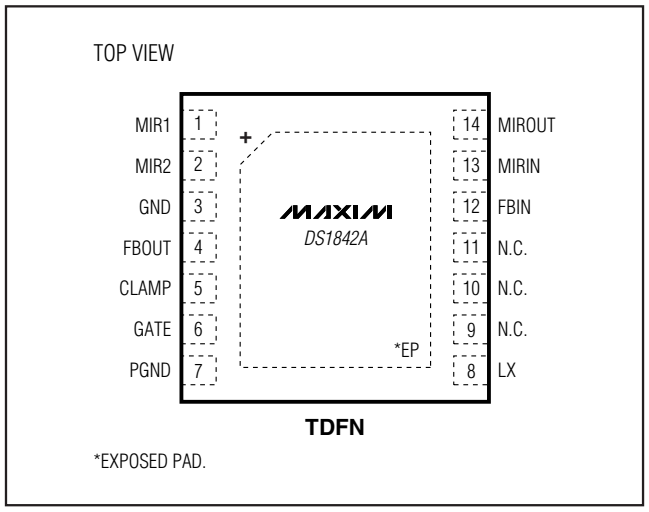


RESISTOR-DIVIDER RATIO vs. TEMPERATURE

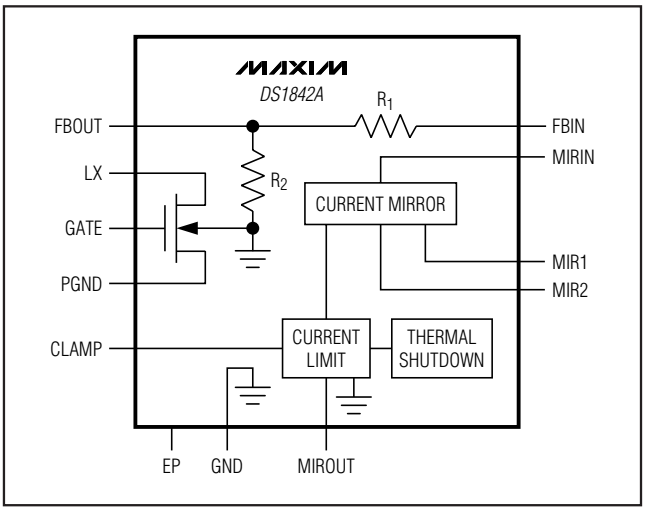


76V, APD, Bias Output Stage with Current Monitoring

Pin Configuration



Block Diagram



Pin Description

PIN	NAME	FUNCTION
1	MIR1	Current Mirror Monitor Output, 10:1 Ratio
2	MIR2	Current Mirror Monitor Output, 5:1 Ratio
3	GND	Ground Connection for Device. Connect directly to ground plane. Connect GND to PGND at a single point. See the *Layout Considerations* section for more information.
4	FBOUT	Feedback Output. Resistor-divider output.
5	CLAMP	Clamp Input. Disables the current mirror output (MIROUT).
6	GATE	FET Gate Connection
7	PGND	Source of Switch FET. Also connect to boost converter's input and output capacitors. Connect PGND to GND at a single point. See the *Layout Considerations* section for more information.
8	LX	FET Drain Connection. Connect to switching inductor.
9, 10, 11	N.C.	No Connection
12	FBIN	Feedback Input. Resistor-divider input.
13	MIRIN	Current Mirror Input
14	MIROUT	Current Mirror Output. Connect to APD bias pin.
—	EP	Exposed Pad. Connect directly to the same ground plane as GND.

Detailed Description

The DS1842A contains discrete high-voltage components required to create an APD bias voltage and to monitor the APD bias current. The device's mirror outputs are a current that is a precise ratio of the output current across a large dynamic range. The mirror response time is fast enough to comply with GPON Rx burst-mode monitoring requirements. The device has a built-in current-limiting feature to protect APDs. The APD current can also be shut down by CLAMP or thermal shutdown. The internal FET and resistor-divider are used in conjunction with a DC-DC boost controller to precisely create the APD bias voltage.

Current Mirror

The DS1842A has two current mirror outputs. One is a 10:1 mirror connected at MIR1, and the other is a 5:1 mirror connected to MIR2.

76V, APD, Bias Output Stage with Current Monitoring

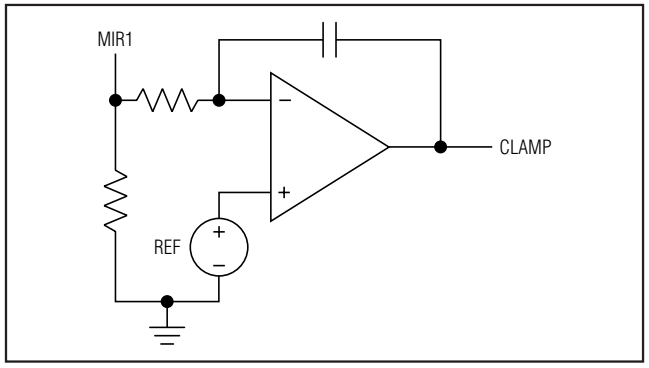


Figure 1. Current Clamp from Current Feedback

The mirror output is typically connected to an ADC using a resistor to convert the mirrored current into a voltage. The resistor to ground should be selected such that the maximum full-scale voltage of the ADC is reached when the maximum mirrored current is reached. For example, if the maximum monitored current through the APD is 2mA with a 1V ADC full scale, and the 10:1 mirror is used, then the correct resistor is approximately 5kΩ. If both MIR1 and MIR2 are connected together, the correct resistor is 1.6kΩ.

The mirror response time is dominated by the amount of capacitance placed on the output. For burst-mode Rx systems where the fastest response times are required (approximately a 50ns time constant), a 3.3pF capacitor and external op amp should be used to buffer the signal sent to the ADC. For continuous mode applications, a 10nF capacitor is all that is required on the output.

Current Clamp

The DS1842A has a current clamping circuit to protect the APD by limiting the amount of current from MIROUT. There are three methods of current clamping available:

1) Internally Defined Current Limit

The device's current clamp circuit automatically clamps the current when it exceeds the maximum MIROUT current.

2) External Shutdown Signal

The CLAMP pin can completely shut down the current from MIROUT. The CLAMP pin is active high.

3) Precise Level Set by External Feedback Circuit

A feedback circuit is used to control the level applied to the CLAMP pin. Figure 1 shows an example feedback circuit.

Thermal Shutdown

As a safety feature, the DS1842A has a thermal-shutdown circuit that turns off the MIROUT and MIRIN currents when the internal die temperature exceeds T_{SHDN}. These currents resume after the device has cooled.

Switch FET

The DS1842A switching FET is designed to complement the DS1875 controller's built-in DC-DC boost controller. APD biasing of 16V to 76V can be achieved using the DS1842A.

Precision Voltage-Divider

The DS1842A includes a resistor-divider to use as the feedback network for the boost converter. The DS1842A resistor-divider ratio, K_R (R_1/R_2), is tightly controlled, allowing the boost converter output to be set with very high precision. K_R can pair with the DS1875's internal DC-DC boost controller. K_R can also be easily modified by adding external series/parallel resistors; however, the temperature coefficient of the external resistors must be considered.

Applications Information

Layout Considerations

Proper PCB layout helps reduce switching noise in the system. PGND is the connection of the switching FET and thus carries high current pulses. PGND should also be connected to the boost converter's input capacitor and output bulk capacitor. Ensure that the PGND trace is low impedance and able to carry the high current from the FET. To keep the switching noise on PGND isolated from GND, a star ground configuration should be used. PGND and GND should only be connected together at one point on the PCB. This point can be either the ground side of the output bulk capacitor or the common ground point of the PCB. Keeping all PCB traces as short as possible reduces radiated noise, stray capacitance, and trace resistance.

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
14 TDFN-EP	T1433+2	21-0137