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REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

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PMIC N/A

STANDARDIZED MILITARY DRAWING

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AMSC N/A

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APPROVED BY: [signature]

DRAWING APPROVAL DATE: 4 JANUARY 1989

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, CMOS
COUNTER/TIMER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-89515

SHEET 1 OF 21

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1145

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1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-89515	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Clock frequency	Circuit function
01	Z84C3006	6.17 MHz	Counter/timer unit

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	D-10 (28-lead, 1.490" x .610" x .232"), dual-in-line package

1.3 Absolute maximum ratings.

V_{CC} supply voltage range (referenced to ground)	-0.3 V dc to +7 V dc
Voltage on any pin (referenced to ground)	-0.3 V dc to +7 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) per device	1.0 W
Lead temperature (soldering, 10 seconds)	+270°C
Maximum junction temperature (T_J):	
at T_C = +125°C	+180°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Supply voltage range	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH}):	
Logic inputs	2.2 V dc
Clock input	V_{CC} -0.6 V dc
Maximum low level input voltage (V_{IL}):	
Logic inputs	0.8 V dc
Clock input	0.45 V dc
Frequency of operation	DC to 6.17 MHz
Case operating temperature range (T_C)	-55°C to +125°C
Clock rise time	20 ns maximum
Clock fall time	20 ns maximum

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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

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TABLE I. Electrical performance characteristics.

Parameter	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5.0\ V \pm 10\%$, Unless otherwise specified 1/	Group A sub-groups	Reference no. 2/	Device types	Limits Min	Limits Max	Unit
Clock input high voltage	V_{IH1}		1,2,3		All	V_{CC} -0.6 V	V_{CC} +0.3 V 3/	V
Clock input low voltage	V_{IL1}		1,2,3			-0.3 3/	0.45	V
Logic input high voltage	V_{IH2}		1,2,3			2.2	V_{CC}	V
Logic input low voltage	V_{IL2}		1,2,3			-0.3 3/	0.8	V
Logic output low voltage	V_{OL}	$I_{OL} = 2.0$ mA	1,2,3				0.4	V
Logic output high voltage	V_{OH1}	$I_{OH} = -1.6$ mA	1,2,3			2.4		V
Logic output high voltage	V_{OH2}	$I_{OH} = -250\ \mu A$	1,2,3			V_{CC} -.8		V
Power supply current	I_{CC1}	$V_{CC} = 5.0$ V; $C_L = 100$ pF, $V_{IH} = V_{CC}$ -0.2 V, $V_{IL} = 0.2$ V, CLK = 6 MHz	1,2,3				10	mA
Power supply current	I_{CC2}	$V_{CC} = 5.0$ V; CLK = 0 MHz	1,2,3				100	µA
Output leakage current low, open drain outputs	I_{LOL}	$V_{OUT} = 0.4$ V	1,2,3			-10	+10	µA
Output leakage current high, open drain outputs	I_{LOH}	$V_{OUT} = 2.4$ V	1,2,3			-10	+10	µA
Darlington drive current 3/	I_{OHD}	$V_{OH} = 1.5$ V, $R_{EXT} = 1.1$ kΩ	1,2,3			-1.5	-5.0	mA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Conditions $-55°C < T_C < +125°C$ $V_{CC} = 5.0$ V ±10% Unless otherwise specified 1/	Group A sub-groups	Reference no. 2/	Device types	Limits Min	Limits Max	Unit
Input low current (input and bi-directional)	I_{IL}	$V_{IN} = 0.4$ V	1,2,3		All	-10	+10	µA
Input high current (input and bi-directional)	I_{IH}	$V_{IN} = 2.4$ V	1,2,3			-10	+10	µA
Clock capacitance	C_{CLK}	$T_C = +25°C$ see 4.3.1c f = 1 MHz Unmeasured pins returned to ground	4				20	pF
Input capacitance	C_I						5	pF
Output capacitance	C_O						15	pF
Maximum frequency 3/	f_{MAX}	$C_L = 100$ pF ±10%	9,10,11			6.17		MHz
Clock cycle time 3/ 4/	t_{cyc1}	$C_L = 100$ pF ±10%	9,10,11	1		162		ns
CLK/TRG cycle time (counter mode)	t_{cyc2}		9,10,11	21		$2t_{cyc1}$		ns
Clock time 3/ rise	t_{rC1}		9,10,11	5			20	ns
fall	t_{fC1}		9,10,11	4			20	ns
CLK/TRG time rise	t_{rC2}		9,10,11	22			40	ns
fall	t_{fC2}		9,10,11	23			40	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Conditions $-55°C < T_C < +125°C$ $V_{CC} = 5.0$ V ±10% Unless otherwise specified 1/	Group A sub-groups	Reference no. 2/	Device types	Limits Min	Limits Max	Unit
Clock width high	t_{PWH1} 5/	C_L = 100 pF ±10%	9,10,11	2	All	65 3/		ns
low	t_{PWL1} 6/		9,10,11	3		65 3/		ns
CLK/TRG width 3/ high	t_{PWH2} 7/		9,10,11	25		120		ns
low	t_{PWL2} 8/		9,10,11	24		120		ns
CS0, CS1 to clock setup 3/	t_{SLH1}		9,10,11	7		160		ns
	t_{SHL1}		9,10,11	7		160		ns
$\overline{CE}$ to clock ↑ setup	t_{SLH2}		9,10,11	8		100		ns
$\overline{IORQ}$ ↓ to clock ↑ setup	t_{SHL3}		9,10,11	9		70		ns
$\overline{RD}$ ↓ to clock ↑ setup	t_{SHL4}		9,10,11	10		70		ns
Data in to clock ↑ setup	t_{SLH5}		9,10,11	13		40		ns
	t_{SHL5}		9,10,11	13		50		ns
$\overline{MI}$ ↓ to clock ↑ setup	t_{SHL6}		9,10,11	14		70		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Conditions $-55°C < T_C < +125°C$, $V_{CC} = 5.0$ V ±10% Unless otherwise specified 1/	Group A sub-groups	Reference no. 2/	Device types	Limits Min	Limits Max	Unit
CLK/TRG + to clock + (time for enabling of prescaler on following clock + timer mode)	t_{SLH7}	C_L = 100 pF ±10%	9,10,11	27	All	150		ns
CLK/TRG + to clock + (setup time for immediate count counter mode)	t_{SLH8}		9,10,11	26		150		ns
All hold times 3/	t_{HHL1}		9,10,11	6		0		ns
	t_{HLH1}		9,10,11	6		0		ns
Clock + to data out delay	t_{PLH1}		9,10,11	11			130	ns
	t_{PHL1}		9,10,11	11			200	ns
Clock + to data out float delay 3/	t_{PLZ1}		9,10,11	12			110	ns
	t_{PHZ1}		9,10,11	12			110	ns
$\overline{MI}$ + to IEO + delay (interrupt immediately preceding $\overline{MI}$) 3/	t_{PHL2}		9,10,11	15			130	ns
$\overline{IORQ}$ + to data out (INTA cycle)	t_{PLH3}		9,10,11	16			110	ns
	t_{PHL3}		9,10,11	16			160	ns
IEI + to IEO + delay	t_{PHL4}		9,10,11	17			100	ns
IEI + to IEO + delay (after ED decode)	t_{PLH5}		9,10,11	18			110	ns
Clock + to $\overline{INT}$ + delay (timer mode)	t_{PHL6}		9,10,11	19			(t_{cyc1} +120)	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 10\%$ Unless otherwise specified 1/	Group A sub-groups	Reference no. 2/	Device types	Limits Min	Limits Max	Unit
CLK/TRG ↑ to $\overline{INT}$ ↓ t_{SLH8} satisfied 3/ (counter mode)	t_{PHL7}	C_L = 100 pF ±10%	9,10,11	20	All		(19) +(26) 9/	ns
t_{SLH8} not satisfied 3/	t_{PHL8}		9,10,11	30			(1)+(19) +(26) 9/	ns
Clock ↑to ZC/TO ↑ delay	t_{PLH9}		9,10,11	28			140	ns
Clock ↓to ZC/TO ↓ delay	t_{PHL10}		9,10,11	29			140	ns

1/ See figure 2 for ac test conditions.

2/ The reference number refers to the position where the parameter being tested appears on figure 2.

3/ Guaranteed, if not tested, to limits specified.

4/ $t_{cyc1} = t_{PWH1} + t_{PWL1} + t_{rC1} + t_{fC1}$.

5/ $t_{PWH1} = t_{cyc1} - t_{rC1} - t_{fC1} - t_{PWL1}$.

6/ $t_{PWL1} = t_{cyc1} - t_{rC1} - t_{fC1} - t_{PWH1}$.

7/ $t_{PWH2} = t_{cyc2} - t_{rC2} - t_{fC2} - t_{PWL2}$.

8/ $t_{PWL2} = t_{cyc2} - t_{rC2} - t_{fC2} - t_{PWH2}$.

9/ Parenthetical numbers reference the table number of a parameter. For example, (1) refers to t_{cyc1}.

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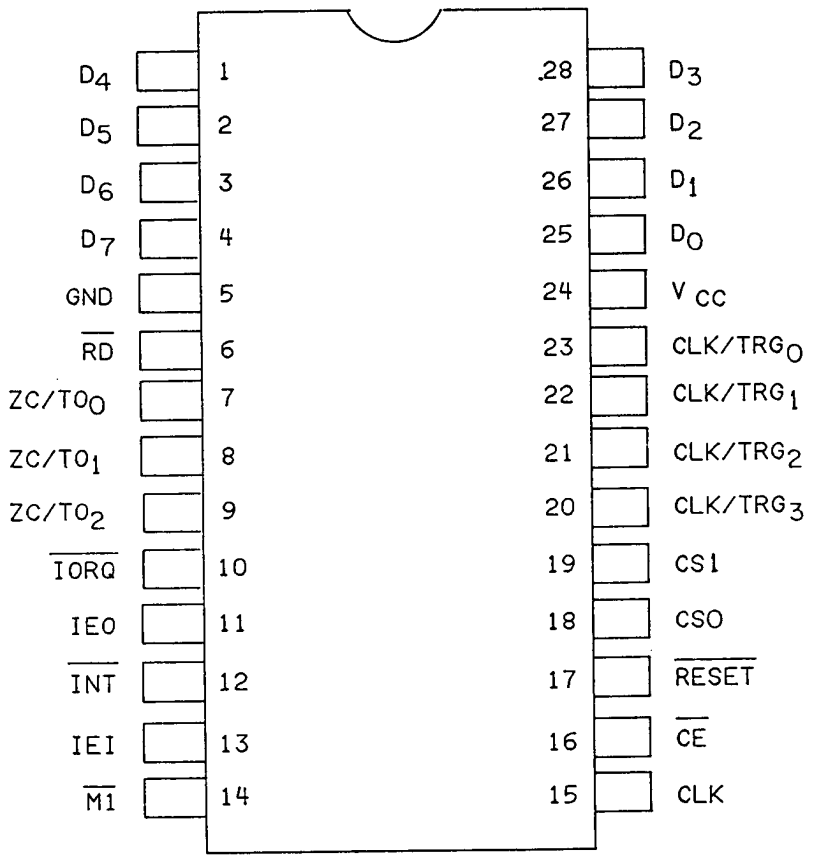

FIGURE 1. Terminal connections.

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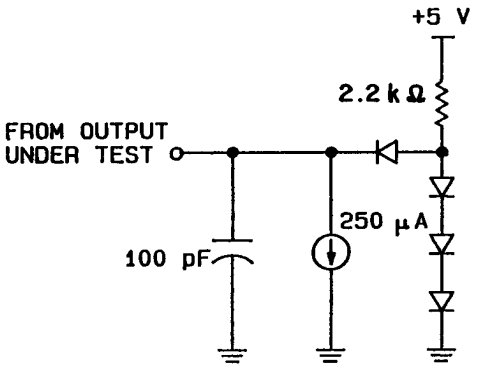
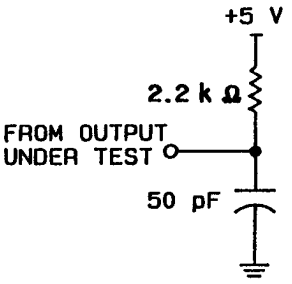
Switching test circuits

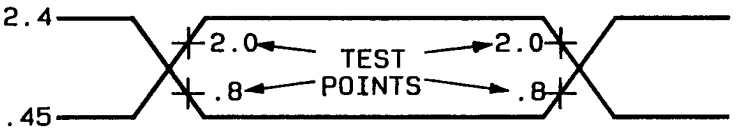
Standard test load



Open drain test load



Switching test input/output waveform



AC testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for logic "0".

FIGURE 2. Timing diagram and test circuits.

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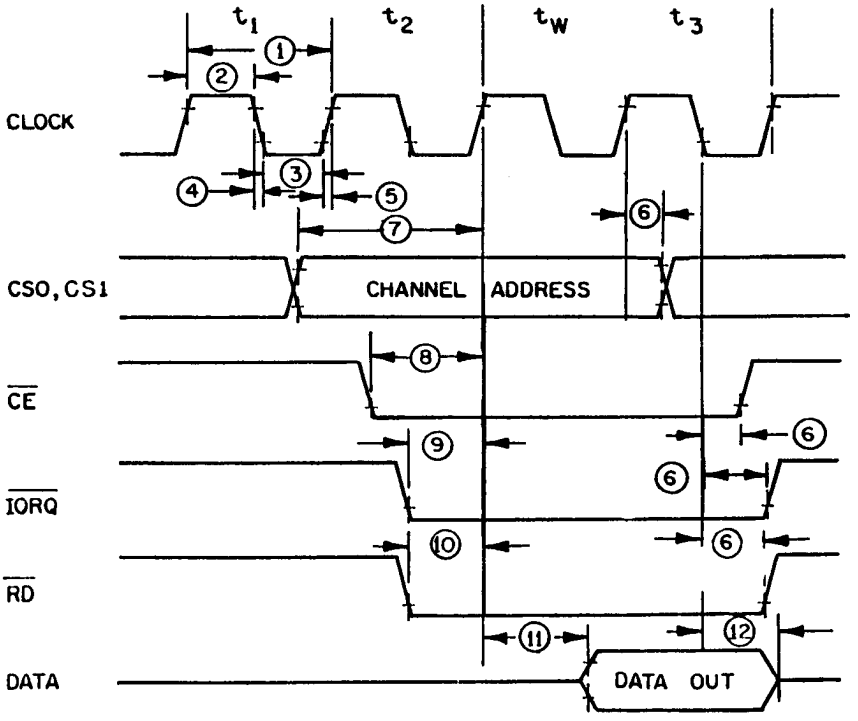
Read cycle



NOTE: No additional wait states are allowed.

FIGURE 2. Timing diagrams and test circuits - Continued.

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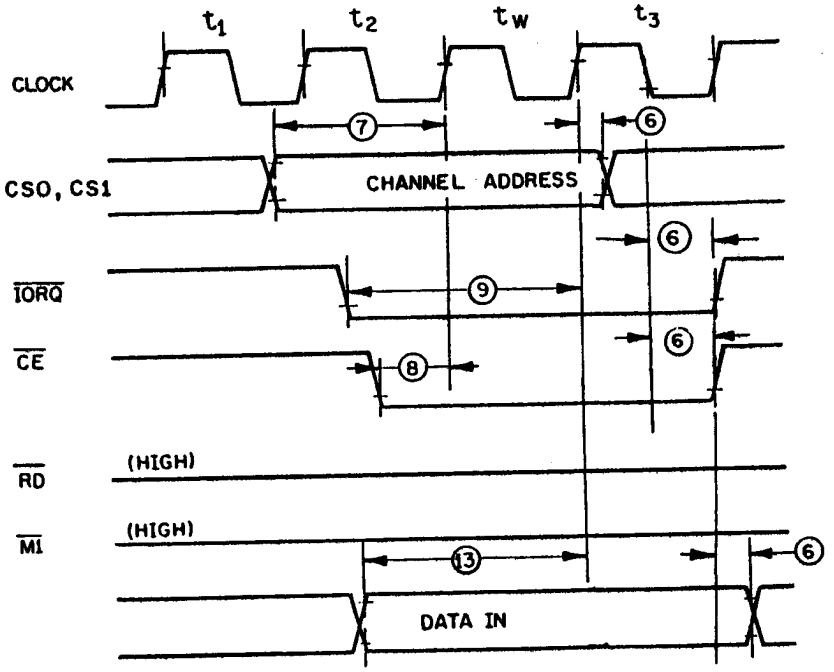
Write cycle



NOTE: No additional wait states are allowed.

FIGURE 2. Timing diagrams and test circuits - Continued.

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Counter mode timing

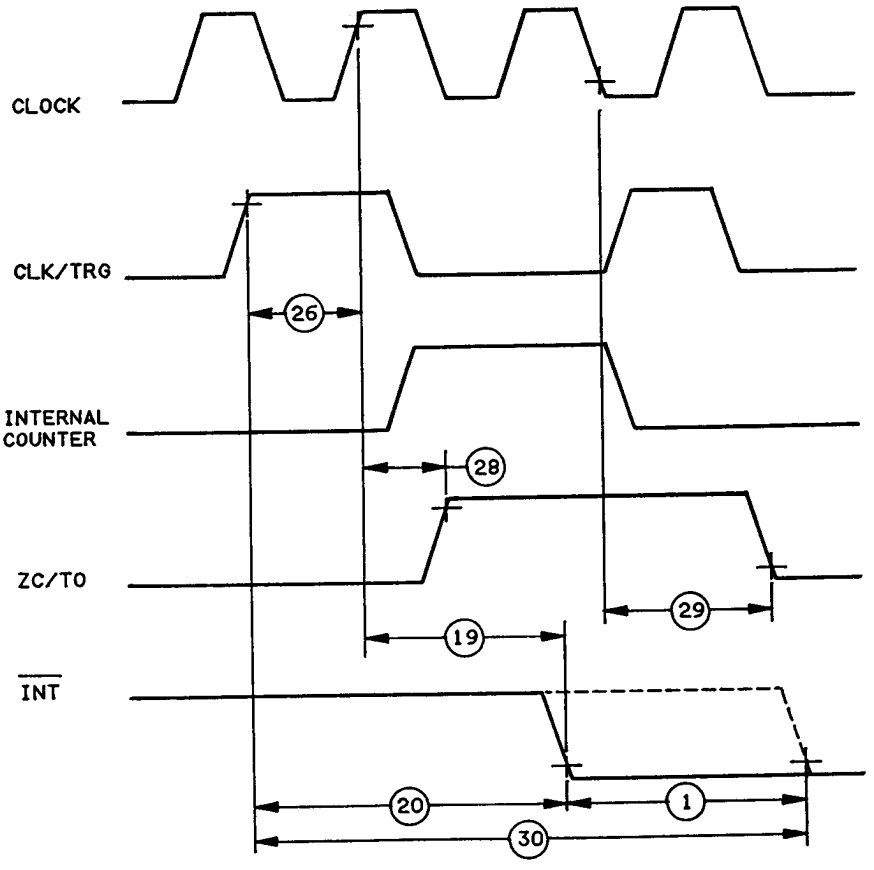

FIGURE 2. Timing diagrams and test circuits - Continued.

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IEI/IEO timing

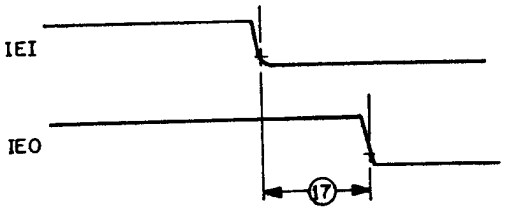

FIGURE 2. Timing diagrams and test circuits - Continued.

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Return from interrupt timing

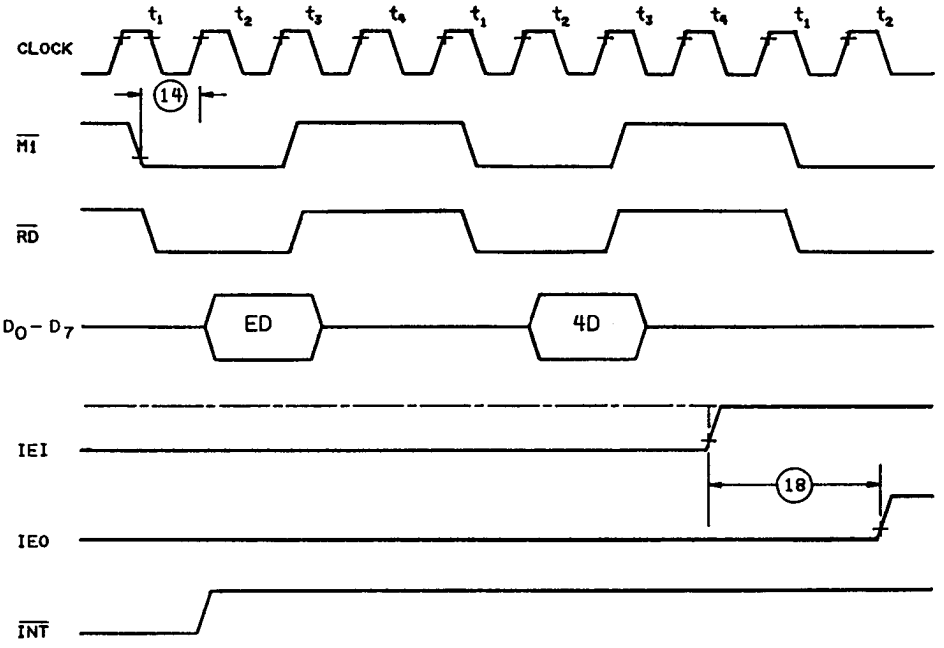

FIGURE 2. Timing diagrams and test circuits - Continued.

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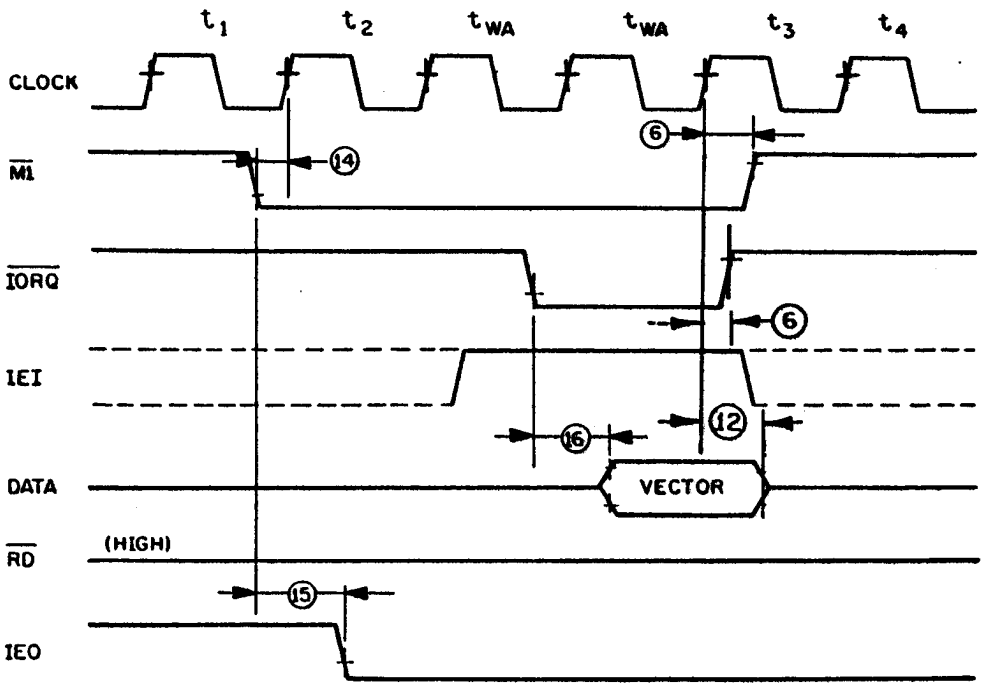
Interrupt acknowledge timing



NOTE t_{wa} = Automatic wait state.

FIGURE 2. Timing diagrams and test circuits - Continued

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Timer mode timing

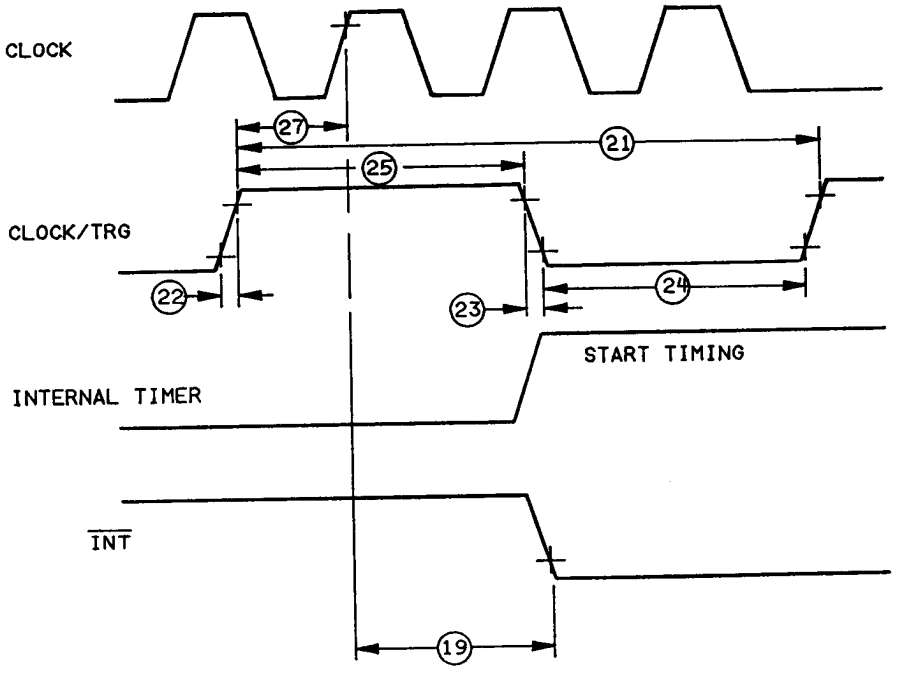

FIGURE 2. Timing diagrams and test circuits - Continued.

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3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{CLK}, C_I, and C_O measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 with zero rejects shall be required.

d. Subgroups 7 and 8 functional testing shall include verification of instruction set. The instruction set forms a part of the vendors test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

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6.4 Symbols, definitions, and functional descriptions. The symbols, definitions, and functional descriptions for this device shall be as follows:

System definitions

Symbol	Function
$D_7 - D_0$	Data bus (bidirectional, 3-state). This bus is used to transfer all data and command words between the CPU and CTC. D_0 is the least significant bit.
CS1-CS0	Channel select (inputs, active high). These pins form a two bit binary address which selects one of the four independent CTC channels for an I/O read or write.
CLK	System clock (input). CLK is the single phase time base input.
$\overline{CE}$	Chip enable (input, active low). A low level on this pin enables the CTC to accept control words, interrupt vectors, or time constant data from the data bus during an I/O write cycle, or to transmit the contents of a down counter to the CPU during an I/O read.
$\overline{M1}$	Machine cycle one (input, active low). When $\overline{M1}$ is active and the IORQ signal is active, the CTC is alerted to place an interrupt vector onto the data bus.
$\overline{RD}$	Read (input, active low). When this line is inactive, and the CTC is enabled, control words, interrupt vectors, or time constant data can be written to the CTC. When active, the contents of any down counter can be read by the CPU without disturbing the count.
IEI	Interrupt enable in (input, active high). When this line is active, the CTC is able to interrupt the CPU.
IEO	Interrupt enable out (output, active high). This output is high only if IEI is high and the CPU is not servicing an interrupt from any CTC channel. In conjunction with IEI, this line can be used to implement a system-wide interrupt priority daisy chain.
$\overline{INT}$	Interrupt request (output, open drain, active low). This signal becomes active whenever any CTC channel which has been programmed to enable interrupts has a zero count in its down counter.
$\overline{IORQ}$	Input/output request (input, active low). Used with $\overline{RD}$ and $\overline{CE}$, this input, when active, allows the transfer of data and control words between the CPU and CTC.

	CS1	CS0
Channel 0	0	0
Channel 1	0	1
Channel 2	1	0
Channel 3	1	1

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$\overline{RESET}$	Reset (input, active low). This signal stops all channels from counting and resets the channel interrupt enable bits in all control registers. The $\overline{INT}$ output is forced to assume the inactive state, IEO reflects IEI, and the CTC's data bus output drivers go to their high impedance state.
CLK/TRG_3-CLK/TRG_0	External clock/timer trigger (input, user selectable active high or low). In the counter mode, these inputs are the clocks of the four independent counters. In the timer mode, an active edge on these pins initiates the timing function. The user may select the active edge to be either the rising or falling edge.
ZC/TO_2-ZC/TO_0	Zero count/timeout (output, active high). In either counter or timer mode, the down counter decrements to zero, an active high going pulse appears on these pins.

6.5 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8951501XX	56708	Z84C3006CMB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
56708	Zilog, Incorporated 210 Hacienda Avenue Campbell, CA 95008

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