

SN54AHCT16245, SN74AHCT16245 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCLS335J – MARCH 1996 – REVISED OCTOBER 2000

查询"74AHCT16245DGGRE4"供应商

- Members of Texas Instruments' Widebus™ Family
- Inputs Are TTL-Voltage Compatible
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 250 mA Per JESD 17

description

The 'AHCT16245 devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54AHCT16245 . . . WD PACKAGE
SN74AHCT16245 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)

1DIR	1	48	$\overline{1OE}$
1B1	2	47	1A1
1B2	3	46	1A2
GND	4	45	GND
1B3	5	44	1A3
1B4	6	43	1A4
V_{CC}	7	42	V_{CC}
1B5	8	41	1A5
1B6	9	40	1A6
GND	10	39	GND
1B7	11	38	1A7
1B8	12	37	1A8
2B1	13	36	2A1
2B2	14	35	2A2
GND	15	34	GND
2B3	16	33	2A3
2B4	17	32	2A4
V_{CC}	18	31	V_{CC}
2B5	19	30	2A5
2B6	20	29	2A6
GND	21	28	GND
2B7	22	27	2A7
2B8	23	26	2A8
2DIR	24	25	$\overline{2OE}$

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74AHCT16245DL	AHCT16245
		Tape and reel	SN74AHCT16245DLR	
	TSSOP – DGG	Tape and reel	SN74AHCT16245DGGGR	AHCT16245
	TVSOP – DGV	Tape and reel	SN74AHCT16245DGVGR	HF245
–55°C to 125°C	CFP – WD	Tube	SNJ54AHCT16245WD	SNJ54AHCT16245WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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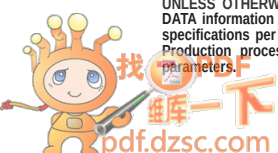
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**TEXAS
INSTRUMENTS**

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SCLSC955 "74AHCT16245D OCTOBER 2000" 供应商

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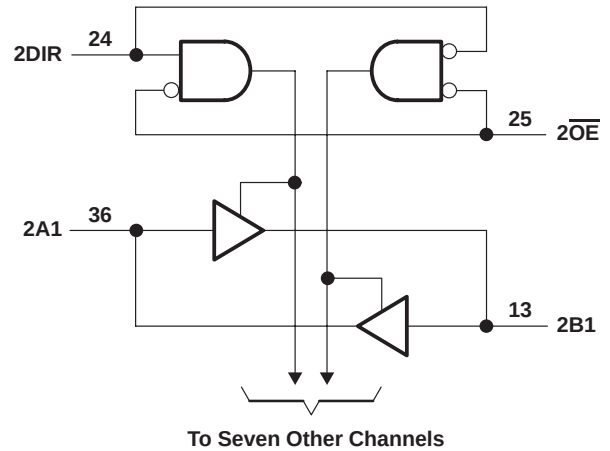
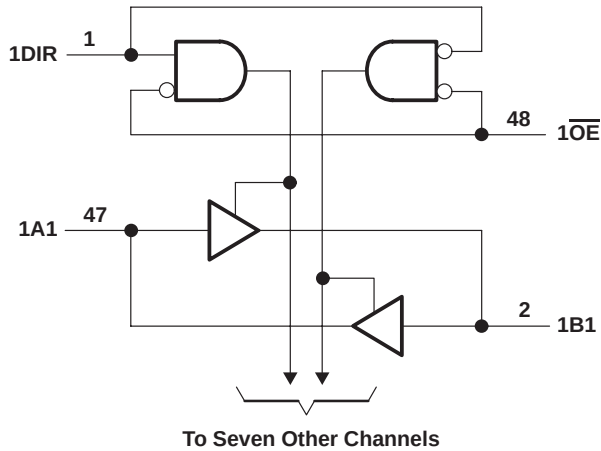
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

Pin diagram of the 74VHC04-100 10-channel inverter. The diagram shows a rectangular package with pins numbered 1 to 28. Pins 1, 25, and 26 are ground connections. Pins 48, 1, 25, and 24 are power supply connections. The internal circuitry shows 10 inverters, each with a propagation delay of 1 ns. The output of each inverter is labeled with a number and a triangle symbol.

Pin	Signal	Internal Label
48	$\overline{1OE}$	G3
1	$\overline{1DIR}$	3 EN1 [BA] 3 EN2 [AB]
25	$\overline{2OE}$	G6
24	$\overline{2DIR}$	6 EN4 [BA] 6 EN5 [AB]
47	1A1	1
46	1A2	2
44	1A3	3
43	1A4	5
41	1A5	6
40	1A6	8
38	1A7	9
37	1A8	11
36	2A1	12
35	2A2	13
33	2A3	14
32	2A4	16
30	2A5	17
29	2A6	19
27	2A7	20
26	2A8	22
2	1B1	23
3	1B2	24
5	1B3	25
6	1B4	26
8	1B5	27
9	1B6	28
11	1B7	29
12	1B8	30
13	2B1	31
14	2B2	32
16	2B3	33
17	2B4	34
19	2B5	35
20	2B6	36
22	2B7	37
23	2B8	38



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}		-0.5 V to 7 V
Input voltage range, V_I (see Note 1): Control inputs		-0.5 V to 7 V
I/O, Output voltage range, V_O (see Note 1)		-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$): Control inputs		-20 mA
I/O, Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)		± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})		± 25 mA
Continuous current through each V_{CC} or GND		± 75 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package		70°C/W
	DGV package	58°C/W
	DL package	63°C/W
Storage temperature range, T_{stg}		-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54AHCT16245		SN74AHCT16245		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	5.5	0	5.5	V
V _{IO}	Input/output voltage, A or B pins	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		−8		−8	mA
I _{OL}	Low-level output current		8		8	mA
Δt/Δv	Input transition rise or fall rate		20		20	ns/V
T _A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54AHCT16245, SN74AHCT16245

16-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCL5331 MAR 1991 REVISION 001 (PR1200) 供应商

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHCT16245		SN74AHCT16245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	4.5 V	4.4	4.5		4.4		4.4		V
	I _{OH} = -8 mA		3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
	I _{OL} = 8 mA				0.36		0.44		0.44	
I _I	$\overline{\text{OE}}$ or DIR	V _I = V _{CC} or GND	0 V to 5.5 V			±0.1		±1*		µA
I _{OZ} [†]	A or B inputs	V _O = V _{CC} or GND	5.5 V			±0.25		±2.5		µA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40		µA
ΔI _{CC} [‡]		One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			1.35		1.5		mA
C _i	$\overline{\text{OE}}$ or DIR	V _I = V _{CC} or GND	5 V			2.5		10		pF
C _{iO}	A or B inputs	V _I = V _{CC} or GND	5 V			4				pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

† For I/O ports, the parameter I_{OZ} includes the input leakage current.

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHCT16245		SN74AHCT16245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	C _L = 15 pF	4.5**	8.5**		1**	10**	1	9.5	ns
t _{PHL}				4.5**	8.5**		1**	10**	1	9.5	
t _{PZH}	$\overline{\text{OE}}$	A or B	C _L = 15 pF	8.9**	13**		1**	14**	1	14	ns
t _{PZL}				8.9**	13**		1**	14**	1	14	
t _{PHZ}	$\overline{\text{OE}}$	A or B	C _L = 15 pF	9.2**	14**		1**	15**	1	15	ns
t _{PLZ}				9.2**	14**		1**	15**	1	15	
t _{PLH}	A or B	B or A	C _L = 50 pF	7	9.5		1	11	1	10.5	ns
t _{PHL}				5.3	9.5		1	11	1	10.5	
t _{PZH}	$\overline{\text{OE}}$	A or B	C _L = 50 pF	8.3	14		1	15	1	15	ns
t _{PZL}				8.3	14		1	15	1	15	
t _{PHZ}	$\overline{\text{OE}}$	A or B	C _L = 50 pF	8	14		1	15	1	15	ns
t _{PLZ}				8	14		1	15	1	15	
t _{sk(o)}			C _L = 50 pF			1***				1	ns

** On products compliant to MIL-PRF-38535, this parameter is not production tested.

*** On products compliant to MIL-PRF-38535, this parameter does not apply.

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SN54AHCT16245, SN74AHCT16245
16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

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noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER	SN74AHCT16245			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}		0.6		V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}		–0.6		V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}		4.8		V
$V_{IH(D)}$ High-level dynamic input voltage		2		V
$V_{IL(D)}$ Low-level dynamic input voltage			0.8	V

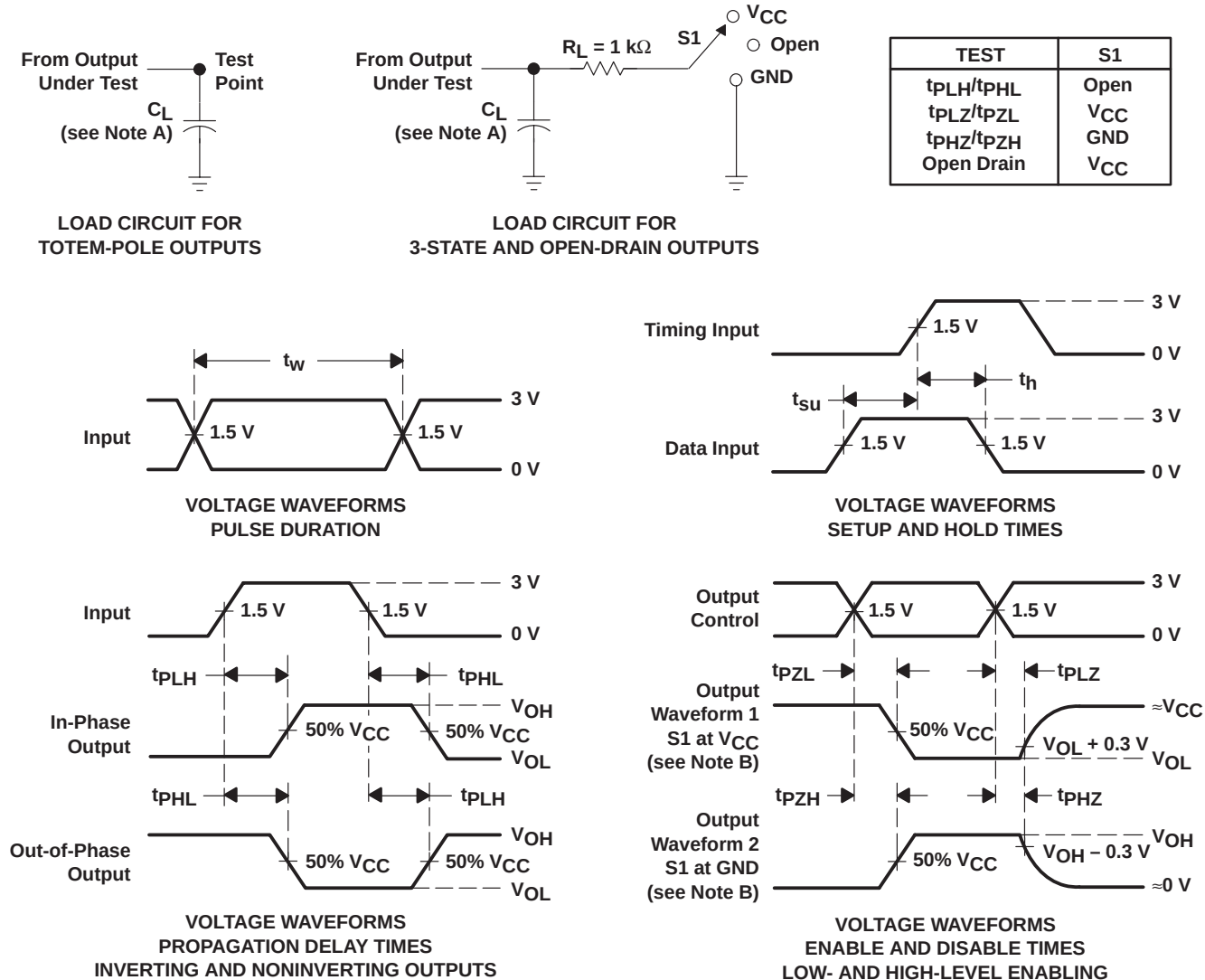
NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	17	pF



PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74AHCT16245DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHCT16245DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHCT16245DGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHCT16245DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT16245DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT16245DGV	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT16245DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT16245DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT16245DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

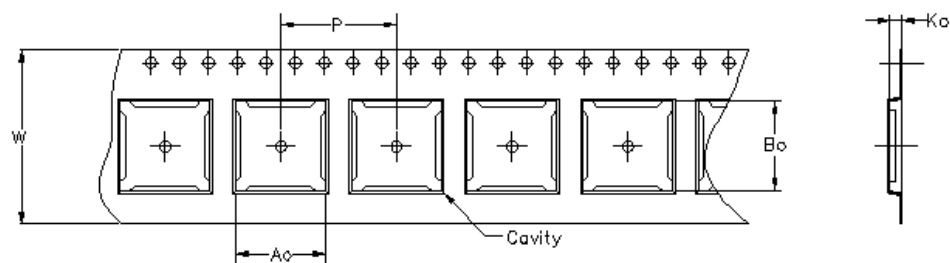
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

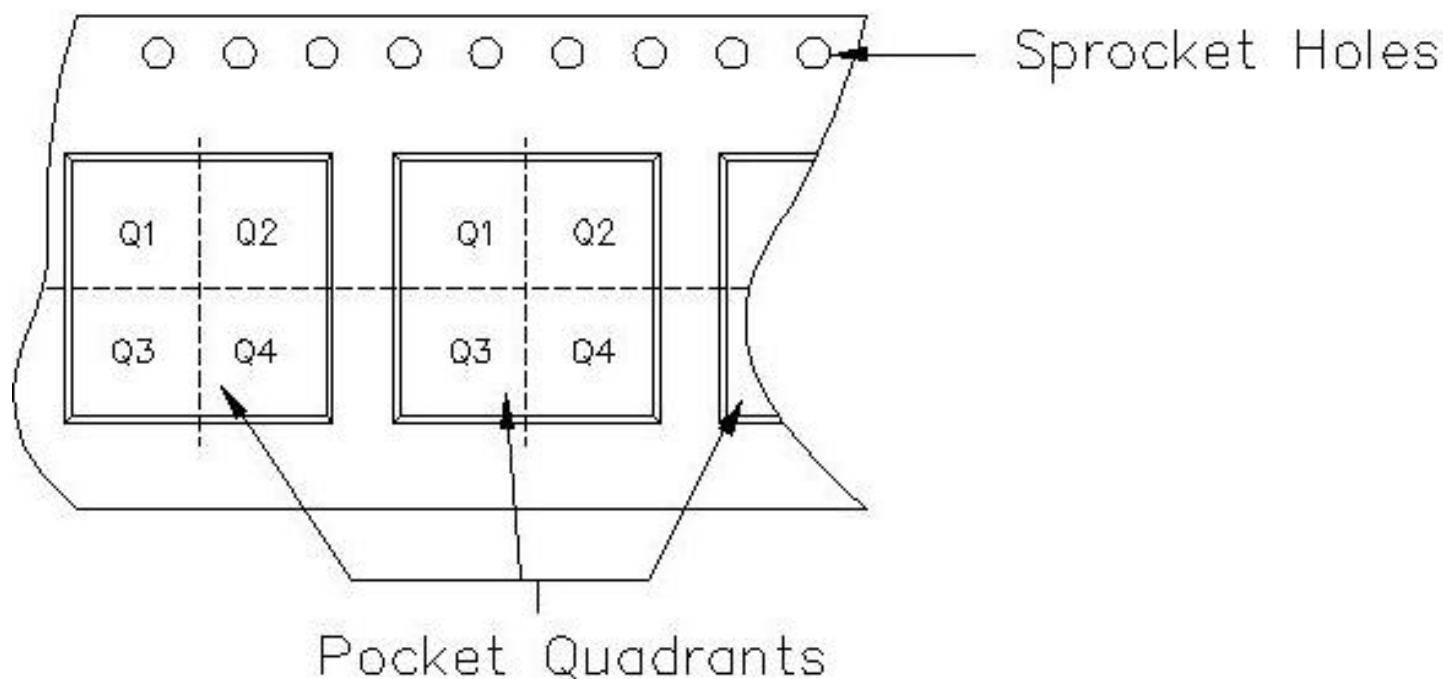
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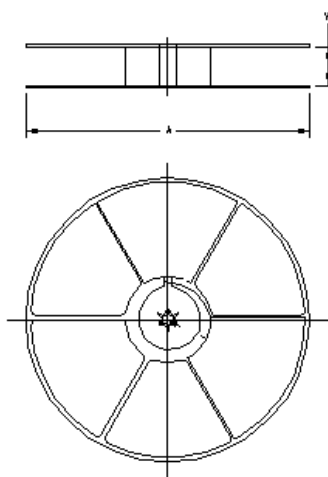
Carrier tape design is defined largely by the component length, width, and thickness.

A_o = Dimension designed to accommodate the component width.
B_o = Dimension designed to accommodate the component length.
K_o = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.

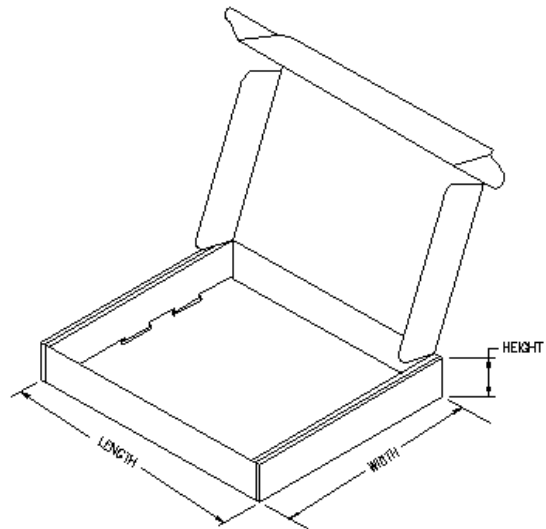


TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT16245DGGR	DGG	48	MLA	330	24	8.6	15.8	1.8	12	24	Q1
SN74AHCT16245DGVR	DGV	48	MLA	330	24	6.8	10.1	1.6	12	24	Q1
SN74AHCT16245DLR	DL	48	MLA	330	32	11.35	16.2	3.1	16	32	Q1


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74AHCT16245DGGR	DGG	48	MLA	333.2	333.2	31.75
SN74AHCT16245DGVR	DGV	48	MLA	333.2	333.2	31.75
SN74AHCT16245DLR	DL	48	MLA	336.6	342.9	41.3



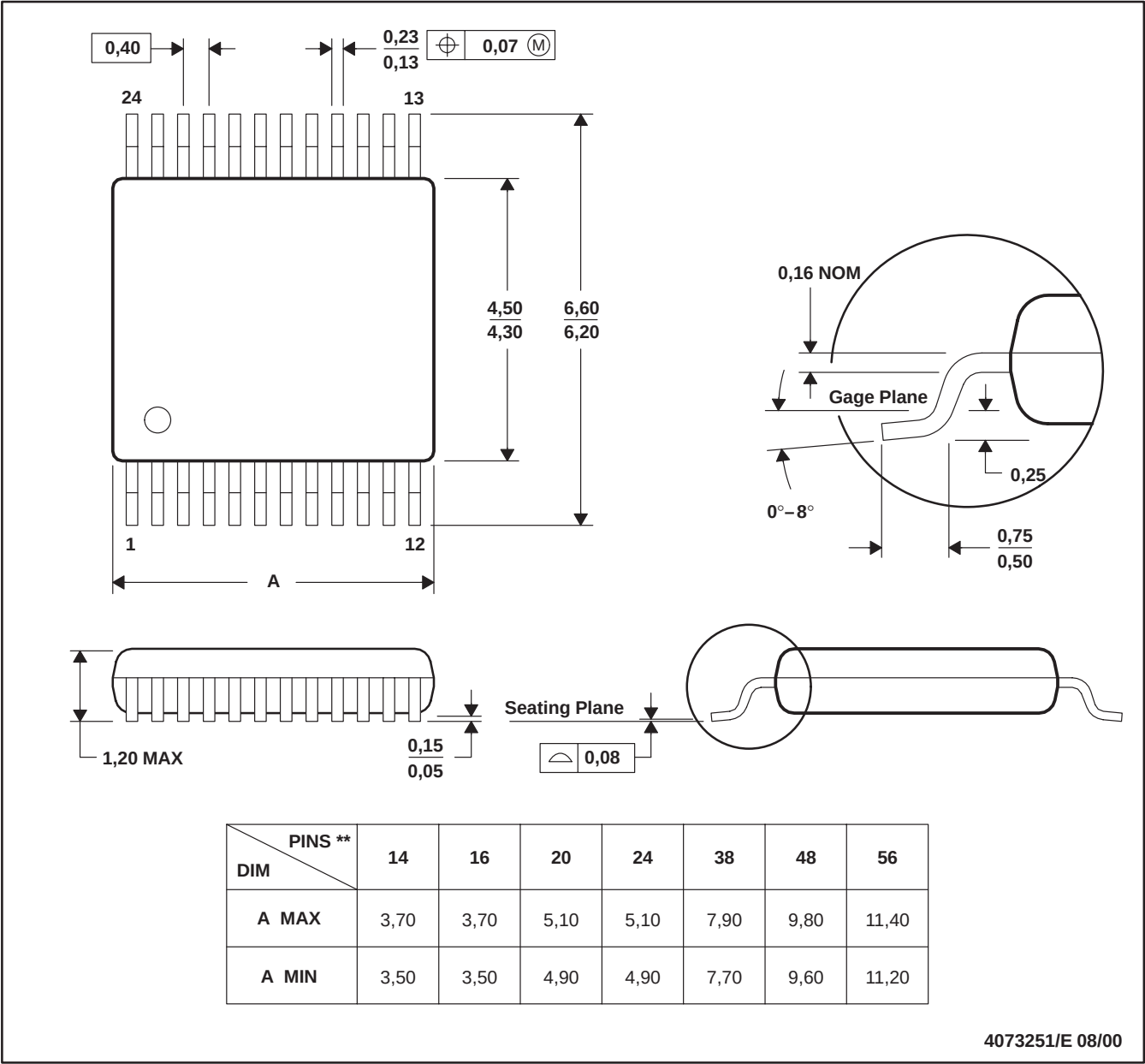
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DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

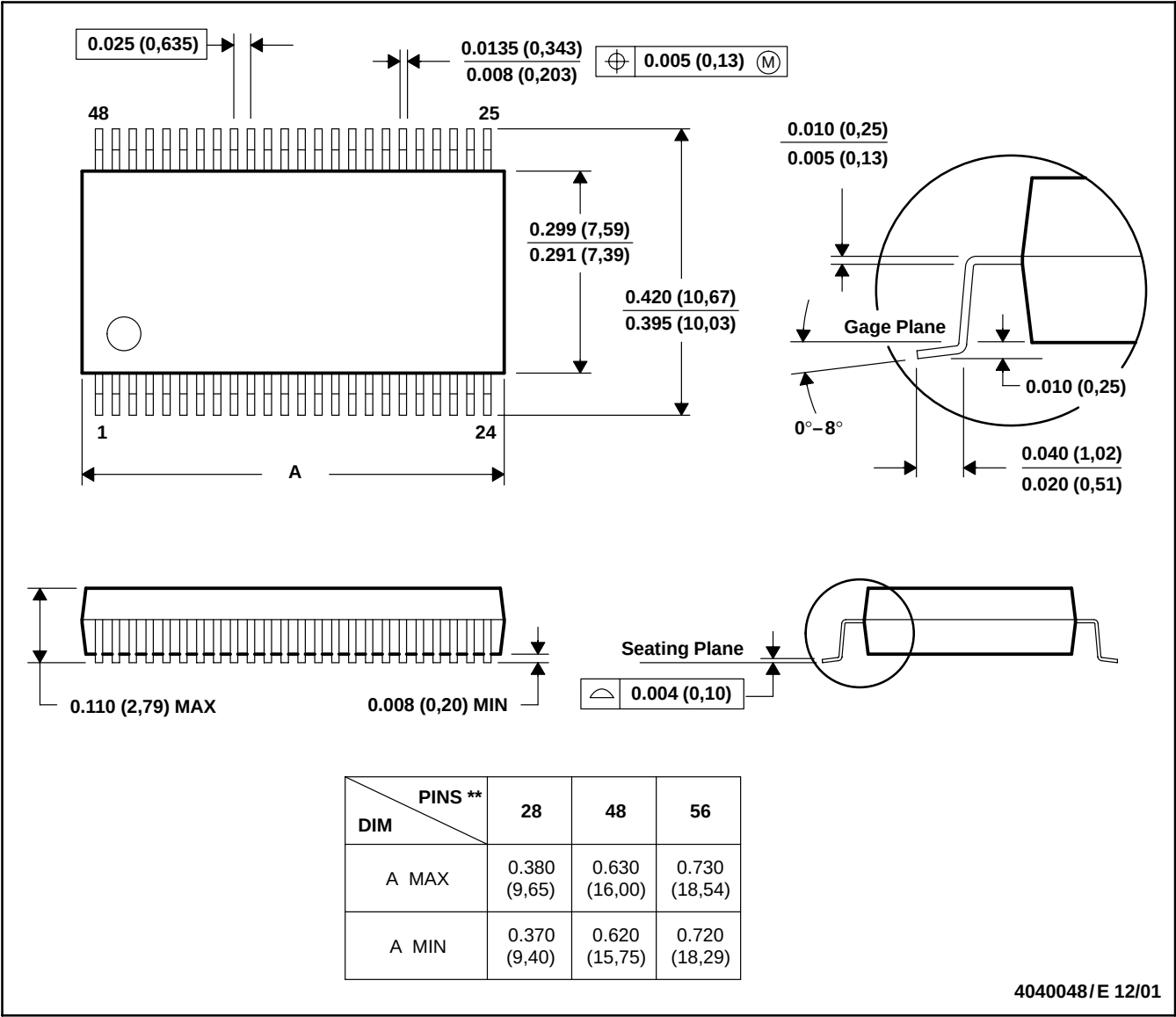


- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

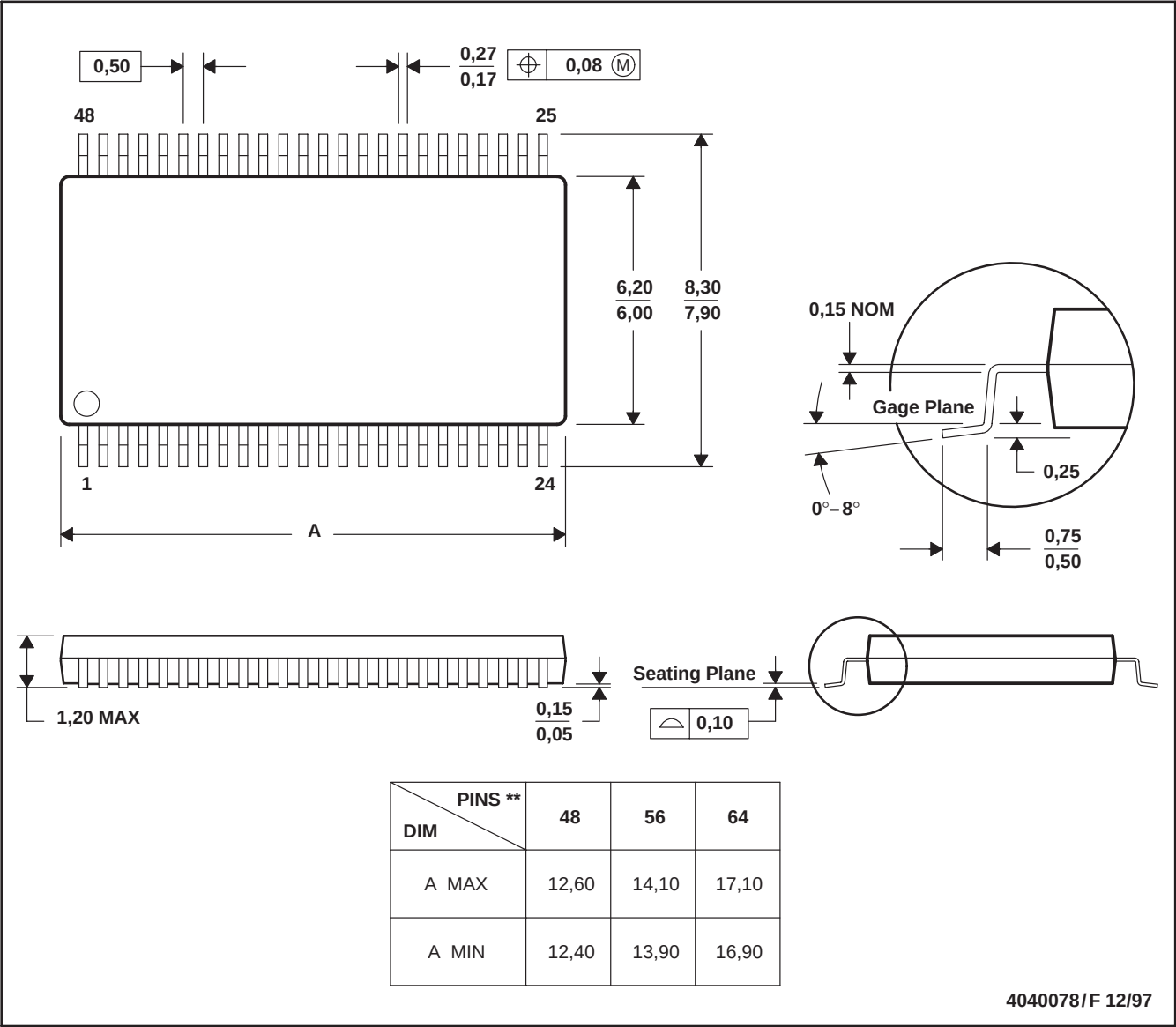
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MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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