88PG8237, 88PG8227, 88PG8226, 88PG8216, 88PG8204

Field Programmable DSP Switcher™ Family

1MHz, Dual Step-down Regulator with AnyVoltage™ Technology

Datasheet

Doc. No. MV-S103563-00, Rev. C
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Document Conventions

	**Note:** Provides related information or information of special importance.
	**Caution:** Indicates potential damage to hardware or software, or loss of data.
	**Warning:** Indicates a risk of personal injury.

Document Status

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PRODUCT OVERVIEW

The 88PG82XX family integrates the dual synchronous Step-Down (Buck) switching regulators housed in a 3 X 4mm QFN-20 package. Internally self-compensated, the step-down regulator requires no external compensation and works with low-ESR output capacitors to simplify the design, minimize the board space, and reduce the amount of external components. The switching frequency for the step-down regulator is 1MHz, allowing the use of low profile surface mount inductors and low value capacitors. Each step-down regulator includes programmable output voltage to allow the user to easily set the output voltage with external resistors, logic control, or serial data interface. The output voltage range is 0.72V to 3.63V.

The 88PG82XX family operates from an input voltage range of 2.75V to 5.5V, making the device well suited for portable applications.

Other key features of the 88PG82XX family include soft start, an internal current limit, an under-voltage lockout, thermal shutdown, over voltage protection, and power-on-reset signals.

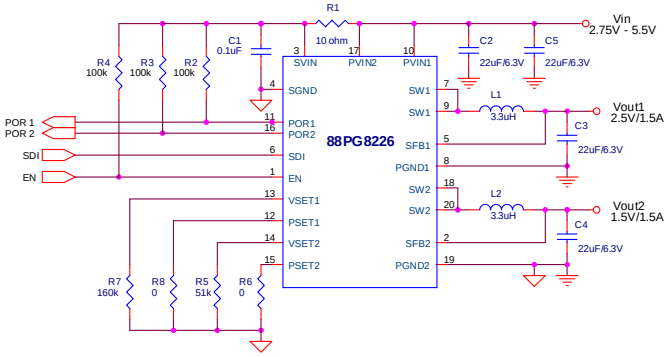
Features

- Tiny 3 X 4 mm QFN-20 package
- Dual switching regulators
- 1MHz switching frequency
- Low quiescent current of 2.1 mA (typ.)
- Stable with low-ESR ceramic output capacitors
- No external compensation required
- Up to 95% efficiency
- Input voltage range: 2.75V to 5.5V
- Programmable output voltage range: 0.72V to 3.63V
- Serial / Logic Programmability
- Any Voltage™ Technology provides 64 output voltage selections to provide up most flexibility
- Built-in undervoltage lockout
- Over voltage protection
- Thermal shutdown protection
- Output short circuit protection
- Output voltage margining capability
- Lead-free packages

Applications

- Portable and handheld computing
- Point-of-load power supplies
- DSP power supplies
- Disk drive power supplies

Figure 1: Typical Application Circuit: Output 1.8V/1.5A and 1.2V/1.5A



!	**Caution:** This is a very high frequency device, proper PCB layout is required. Refer to page 47 for further details.

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Table 1: DC Loading Current Ratings

	Buck 2			
Buck 1	**0.75A**	**1.0A**	**1.5A**	**2.0A**
0.75A	**88PG8204**[1]	88PG8205	88PG8206	88PG8207
1.0A	88PG8214	88PG8215	**88PG8216**[1]	88PG8217
1.5A	88PG8224	88PG8225	**88PG8226**[1]	**88PG8227**[1]
2.0A	88PG8234	88PG8235	88PG8236	**88PG8237**[1]

1. The part numbers in Bold are released to production. The other parts are available upon request. Contact Marvell® marketing for availability.

The devices shown in Table 1 have the same input and output voltage range for step-down registers.

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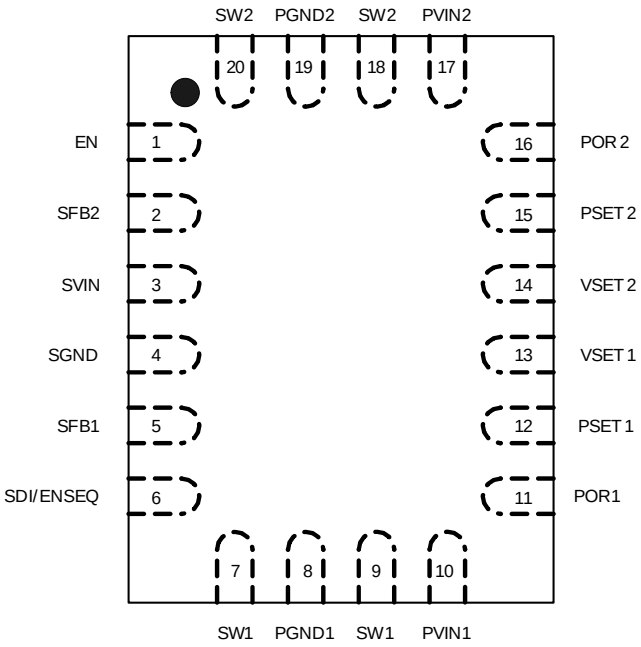
1.1 Pin Configuration

Figure 2: 88PG82XX Family 3X4mm QFN-20 Package—Top View



1.2 Pin Description

1.2.1 Pin Types

Table 2: Pin Type Definitions

Pin Type	Definition
I	Input Only
O	Output Only
S	Supply
NC	Not Connected
GND	Ground

Table 3 provides pin descriptions for the 88PG82XX.

Table 3: Pin Descriptions

Pin #	Pin Name	Pin Type	Pin Description
1	EN	I	Enable. Logic high (≥ 2.0V) enables both switching regulators. Logic low (≤0.8V) disables the regulators. When disabled, the switch nodes SW1 and SW2 are Hi-Z. The feedback nodes SFB1 and SFB2 are pulled down by 20K resistors, and the power on reset nodes POR1 and POR2 are pulled down by internal open drain NFETs. The low signal has to be at least 20 µs to disable both regulators. If this pin is left floating, an internal 10 µA current source pulls this pin high to SVIN, enabling the regulator.
2	SFB2	I	Switching Regulator Feedback. Senses the output voltage of the switching regulator 2.
3	SVIN	S	Signal Input Voltage. The input voltage is 2.75V to 5.5V for internal circuitry. Connect a 0.1 µF decoupling capacitor between SVIN and SGND and position it as close as possible to the IC.
4	SGND	GND	Ground. Connect to a ground plane.
5	SFB1	I	Switching Regulator Feedback. Senses the output voltage of the switching regulator 1.

Table 3: Pin Descriptions

Pin #	Pin Name	Pin Type	Pin Description
6	SDI/ENSEQ	I	Multi-purpose logic input. Logic high (≥ 2.0V) enables soft start and sequence. Buck 1 starts followed by Buck 2, once V_{OUT1} is within a specified tolerance. The soft start rise time is typically 5 ms and is dependent on output, but independent of capacitance and load current. If a short circuit is detected on Buck1, then Buck 2 will be disabled. Logic low (≤ 0.8V) disables the start up sequence. Buck 1 and Buck 2 will start up together without any soft start. Serial Data Input. The input data into this pin is used to program the output voltage (See "Output Voltage Settings" on page 22). The power-good signal has to be high before the serial data interface can be used. To implement soft start a 10K pull-up resistor must be connected to SVIN. This pin is internally pulled down by a 10 µA current source.
7, 9	SW1	O	Switch Node for regulator 1. Internal power MOSFET drain. Connects to an external inductor.
8	PGND1	GND	Power Ground. The power ground must be connected to the negative terminal of the input and output capacitors.
10	PVIN1	S	Power Input Voltage. Internal power MOSFET source. Connect the 10µF decoupling capacitor between PVIN and PGND and position it as close as possible to the IC. **NOTE:** PVIN and PVIN2 must be connected together and should not be separated.
11	POR1	O	Power-On Reset 1. This pin is an open drain output to indicate the status of the output voltage. The output pin goes high 40 ms after the output voltage is within the specified tolerance. POR2 and POR1 can be connected to the same external pull-up resistor to indicate "both outputs good".
12	PSET1	I	Percent Set for Regulator 1. 1. Resistor Programming: Connect an external resistor to ground to set the output voltage of the switching regulator. See the "Electrical Characteristics" for resistor values and Output Voltage Settings. Use resistor values with a tolerance of 5% or better. The total capacitance across this pin and GND should be equal to 25 pF or less. If the pin is not used, it must be connected to GND. 2. Logic Programming: Four output voltage levels (1.8V, 2.5V, 3.0V, 3.3V) can be set by connecting the VSET and PSET pins to either GND or SVIN.
13	VSET1	I	Voltage Set for Regulator 1. 1. Resistor Programming: Connect an external resistor to ground to set the output voltage of the switching regulator. See the "Electrical Characteristics" for resistor values and Output Voltage Settings. Use resistor values with a tolerance of 5% or better. The total capacitance across this pin and GND should be equal to 25 pF or less. 2. Logic Programming: Four output voltage levels (1.8V, 2.5V, 3.0V, 3.3V) can be set by connecting the VSET and PSET pins to either GND or SVIN.

Table 3: Pin Descriptions

Pin #	Pin Name	Pin Type	Pin Description
14	VSET2	I	Voltage Set for Regulator 2. 1. Resistor Programming: Connect an external resistor to ground to set the output voltage of the switching regulator. See the “Electrical Characteristics” for resistor values and Output Voltage Settings. Use resistor values with a tolerance of 5% or better. The total capacitance across this pin and GND should be equal to 25 pF or less. 2. Logic Programming: Four output voltage levels (0.8V, 1.0V, 1.2V, and 1.5V) can be set by connecting the VSET and PSET pins to either GND or SVIN.
15	PSET2	I	Percent Set for Regulator 2. 1. Resistor Programming: Connect an external resistor to ground to set the output voltage of the switching regulator. See the “Electrical Characteristics” for resistor values and Output Voltage Settings. Use resistor values with a tolerance of 5% or better. The total capacitance across this pin and GND should be equal to 25 pF or less. If the pin is not used, it must be connected to GND. 2. Logic Programming: Four output voltage levels (0.8V, 1.0V, 1.2V, and 1.5V) can be set by connecting the VSET and PSET pins to either GND or SVIN.
16	POR2	O	Power-On Reset 2. This pin is an open drain output to indicate the status of the output voltage. The output pin goes high 40 ms after the output voltage is within the specified tolerance. POR2 and POR1 can be connected to the same external pull up resistor to indicate “both output good”.
17	PVIN2	S	Power Input Voltage for regulator 2: Internal power MOSFET source. Connect the 10 µF decoupling capacitor between PVIN2 and PGND2 and position it as close as possible to the IC. **NOTE:** PVIN and PVIN2 must be connected together and should not be separated.
19	PGND2	GND	Power Ground for regulator 2: The power ground must be connected to the negative terminal of the input and output capacitors.
18, 20	SW2	O	Switch Node for regulator 2: Internal power MOSFET drain. Connects to an external inductor.

2 Electrical Specifications

2.1 Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings[1]

Parameter	Symbol	Range	Units
Signal Input Voltage	S_{VIN}	-0.3 to 6.0	V
Power Input Voltage	P_{VIN1}, P_{VIN2}	-0.3 to 6.0	V
Switch Voltage[2]	V_{SW1}, V_{SW2}	-0.6 to (S_{VIN} +0.3)	V
Switching Regulator Feedback Voltage	V_{SFB1}, V_{SFB2}	-0.6 to (S_{VIN} +0.3)	V
Voltage Set	V_{VSET1}, V_{VSET2}	-0.6 to (S_{VIN} +0.3)	V
Percentage Set Voltage	V_{PSET1}, V_{PSET2}	-0.6 to (S_{VIN} +0.3)	V
Enable	V_{EN}	-0.6 to (S_{VIN} +0.3)	V
POR Voltage	V_{POR}	-0.6 to (S_{VIN} +0.3)	V
SDI Voltage	V_{SDI}	-0.6 to (S_{VIN} +0.3)	V
Operating Temperature Range[3]	T_{OP}	-40 to 85	°C
Maximum Junction Temperature	T_{JMAX}	125	°C
Storage Temperature Range	T_{STOR}	-65 to 150	°C
ESD Rating[4]		2	kV

1. Exceeding the absolute maximum rating may damage the device
2. -10V to (VIN +0.3)V for less than 50µs
3. Specifications over the -40°C to 85°C operating temperature ranges are assured by design, characterization and correction with statistical process controls
4. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF

2.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions[1]

Parameter	Symbol	range	Units
Single Input Voltage	S_{VIN}	2.75 to 5.5	V
Power Input Voltage	P_{VIN1}, P_{VIN2}	2.75 to 5.5	V
Package Thermal Resistance[2]	θ_{JA}	70	°C/W
	θ_{JC}	19	°C/W

1. This device is not gauranteed to function outside the specified operating range
2. Test on 4-layer (JESD51-7) and vias (JESD51-5) board

2.3 Electrical Characteristics

The following applies unless otherwise noted: S_{VIN} = P_{VIN1}= P_{VIN2}, V_{VSET1} = V_{PSET} = 0, V_{OUT1} = 1.8V, V_{VSET2} = SV_{IN}, V_{PSET2} = 0, V_{OUT2} = 1.2V, V_{EN} = SV_{IN}, $L_{(BUCK1)}$ = 2.2 µH, $C_{OUT\ (BUCK1)}$ = 22µF (Ceramic), $L_{(BUCK2)}$ = 2.2 µH, $C_{OUT\ (BUCK2)}$ = 22 µF (Ceramic), T_A = 25 °C. **Bold values indicate -40 °C ≤ T_A ≤ 85 °C.**

Table 6: Electrical Characteristics Table

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Signal Input Voltage Range	S_{VIN}	S_{VIN} = P_{VIN}	**2.75**		**5.5**	V
Power Input Voltage Range	P_{VIN}		**2.75**		**5.5**	V
Total Quiescent Current		No load		2.1		mA
Shutdown Supply Current	I_{SVIN}	V_{EN} = 0V		1	50	µA
Undervoltage Lockout	V_{UVLO}	High threshold, SV_{IN} increasing		2.65	2.70	V
		Low threshold, SV_{IN} decreasing	2.44	2.55		V
Over-voltage Protection	V_{OVP}	High threshold, SV_{IN} increasing		5.7		V
		Low threshold, SV_{IN} decreasing		5.6		
EN Threshold Voltage	V_{EN}	Enable regulators	1.70			V
		Disable regulators			0.7	
EN Pin Input Current	I_{EN}	V_{EN} = 5.0V			1	µA
		V_{EN} = 0V		10	20	
Over-temperature Thermal Shutdown	T_{OTS}	T_J increasing (Disable regulators)		150		°C
		T_J decreasing (Enable regulators)		105		

2.4 Switching Step-down Regulator

The following applies unless otherwise noted: $S_{VIN} = P_{VIN1} = P_{VIN2}$, $V_{VSET1} = V_{PSET} = 0$, $V_{OUT1} = 1.8V$, $V_{VSET2} = SV_{IN}$, $V_{PSET2} = 0$, $V_{OUT2} = 1.2V$, $V_{EN} = SV_{IN}$, $L_{(BUCK1)} = 2.2\ \mu H$, $C_{OUT\ (BUCK1)} = 22\ \mu F$ (Ceramic), $L_{(BUCK2)} = 2.2\ \mu H$, $C_{OUT\ (BUCK2)} = 22\ \mu F$ (Ceramic), $T_A = 25\ °C$. **Bold values indicate -40 °C ≤ T_A ≤ 85 °C.**

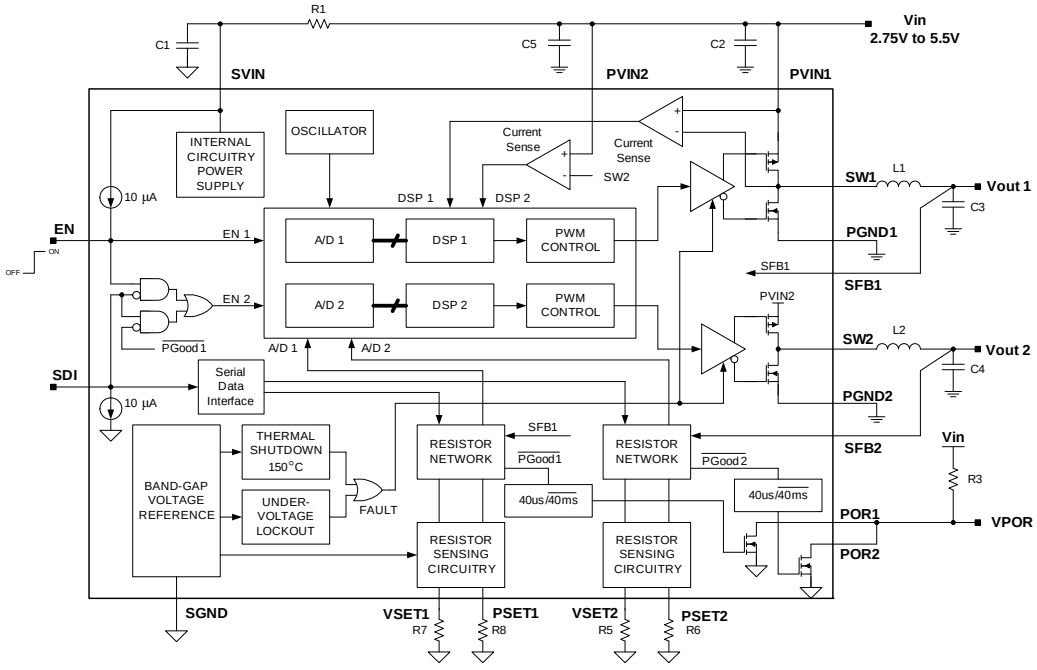
Table 7: Switching Step-down Regulator Table

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Minimum Peak Switch Current Limit	I_{LIM}	88PG8204 = V_{OUT1}		1.12		A
		88PG8204 = V_{OUT2}		1.12		
		88PG8216 = V_{OUT1}		1.5		
		88PG8216 = V_{OUT2}		2.25		
		88PG8226 = V_{OUT1}		2.25		
		88PG8226 = V_{OUT2}		2.25		
		88PG8227 = V_{OUT1}		2.25		
		88PG8227 = V_{OUT2}		3.0		
		88PG8237 = V_{OUT1}		3.0		
		88PG8237 = V_{OUT2}		3.0		
Maximum Output Current	I_{OUT}	88PG8204 = V_{OUT1}, L1 = 4.7 µH		0.75		A
		88PG8204 = V_{OUT2}, L2 = 4.7 µH		0.75		
		88PG8216 = V_{OUT1}, L1 = 4.7 µH		1.0		
		88PG8216 = V_{OUT2}, L2 = 3.3 µH		1.5		
		88PG8226 = V_{OUT1}, L1 = 3.3 µH		1.5		
		88PG8226 = V_{OUT2}, L2 = 3.3 µH		1.5		
		88PG8227 = V_{OUT1}, L3 = 3.3 µH		1.5		
		88PG8227 = V_{OUT2}, L4 = 2.0 µH		2.0		
		88PG8237 = V_{OUT1}, L1 = 2.0 µH		2.0		
		88PG8237 = V_{OUT2}, L2 = 2.0 µH		2.0		
Output Voltage	V_{OUT}	R_{VSET} = 11K		0.8		V
		R_{VSET} = 18K		1.0		
		R_{VSET} = 30K		1.2		
		R_{VSET} = 51K		1.5		
		R_{VSET} = 100K		1.8		
		R_{VSET} = 160K		2.5		
		R_{VSET} = 270K		3.0		
		R_{VSET} = 470K		3.3		
Output Voltage 1, Logic Programmability	V_{OUT1}	V_{VSET1} = 0V, V_{PSET1} = 0V		1.8		V
		V_{VSET1} = 0V, V_{PSET1} = SVIN		2.5		
		V_{VSET1} = SVIN, V_{PSET1} = 0V		3.0		
		V_{VSET1} = SVIN, V_{PSET1} = SVIN		3.3		

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Voltage 2, Logic Programmability	V_{OUT2}	V_{VSET2} = 0V, V_{PSET2} = 0V		0.8		V
		V_{VSET2} = 0V, V_{PSET2} = SVIN		1.0		
		V_{VSET2} = SVIN, V_{PSET2} = 0V		1.2		
		V_{VSET2} = SVIN, V_{PSET2} = SVIN		1.5		
Percentage Set		R_{VSET} = 11K		-10		%
		R_{VSET} = 18K		-7.5		
		R_{VSET} = 30K		-5		
		R_{VSET} = 51K		-2.5		
		R_{VSET} = 0K		0		
		R_{VSET} = 100K		2.5		
		R_{VSET} = 160K		5		
		R_{VSET} = 270K		7.5		
		R_{VSET} = 470K		10		
Output Voltage Line Regulation	V_{LNREG}	S_{VIN} = P_{VIN} = 3.0V to 5.0V V_{OUT} = 1.5V I_{LOAD} = $I_{OUT(MAX)}$/4		0.05		%
Output Voltage Load Regulation	V_{LDREG}	S_{VIN} = P_{VIN} = 5.0V V_{OUT} = 1.5V I_{LOAD} = $I_{OUT(MAX)}$/4 to $I_{OUT(MAX)}$		0.05		%
Switching Frequency	f_{SW}	I_{LOAD} = $I_{OUT(MAX)}$/2		1		MHz
Switch Leakage Current	I_{LSW}	S_{VIN} = P_{VIN} = 5V, V_{EN} = 0V V_{SW} = P_{VIN}		1	50	µA
		S_{VIN} = P_{VIN}, V_{EN} = 0V V_{SW} = SGND = PGND		1	50	
Power-On Reset Threshold Voltage for Buck1	V_{PORTH}	V_{OUT} ≥ 1.35V		V_{OUT}* 90%		V
		V_{OUT} ≤ 1.32V		V_{OUT}-130 mV		
Power-On Reset Threshold Voltage for Buck2	V_{PORTH}	V_{OUT} ≥ 1.35V		V_{OUT}* 90%		V
		V_{OUT} ≤ 1.32V		V_{OUT}-130 mV		
Power-On Reset Output Low Voltage	V_{PORL}	I_{SINK} = 2 mA, V_{EN} = SV_{IN}			0.4	V
Power-On Reset Leakage Current	I_{POR}	V_{EN} = 5V		1		µA
Power-On Reset Delay	t_{RESET}			40		ms

3 Functional Description

Figure 3: 88PG82XX Block Diagram

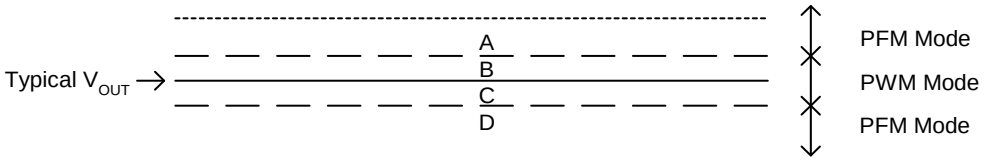


3.1 Regulation and Start-up

The step-down switching regulator uses Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM) modes to regulate the output voltage using digital control. The mode of operation depends on the level of output current and the output voltage.

In steady states, the step-down switching regulator monitors the current flowing through the inductor to determine if the regulator is handling heavy or light load applications. For heavy load applications, the step-down regulator operates in the PWM mode (B and C) to minimize the ripple current for optimum efficiency and to minimize the ripple output voltage. The step-down regulator operates in the PFM and Discontinuous Conduction Mode (DCM) (A and D) to limit the switching actions for optimum efficiency in light load applications. In this mode, the average output voltage is slightly higher than the average output voltage for heavy transient load applications.

Figure 4: Output Voltage Window



3.1.1 Soft Start and Sequencing

The 88PG82XX device's outputs can either be sequenced to start up together or have V_{OUT1} start followed by $V_{OUT2.}$ When the SDI pin is low, the V_{OUT1} and V_{OUT2} will start up together with a start up time in the order of 100 µs, as shown in Figure 5. If the SDI pin is high, then V_{OUT1} will start first and V_{OUT2} will start as soon as V_{OUT1} is within its specified tolerance (see Figure 6). Both outputs will have a soft start ramp. The POR2 output will go high 40 ms after V_{OUT2} is within its regulation limits.

Soft start is a highly desirable property in "Hot-Plug" applications. The 88PG82XX starts up in less then 100 µs when soft-start is disabled (Figure 7). However in soft-start mode, the 88PG82XX controls the rise time of the output voltage, thereby dramatically reducing the inrush current. The 88PG82XX rise time is roughly 0.25V/ms and it is independent of output capacitance and load current (see Figure 8). Figure 9 shows the output voltage rise time with a 100 µF output capacitor. Although there is a difference in output capacitance between Figure 6 and Figure 9, the output voltage rise time difference is less than 0.1 ms.

Figure 5: Startup without Sequencing

Figure 6: Startup with Sequencing and Soft Start (C_{OUT}= 22 µF)

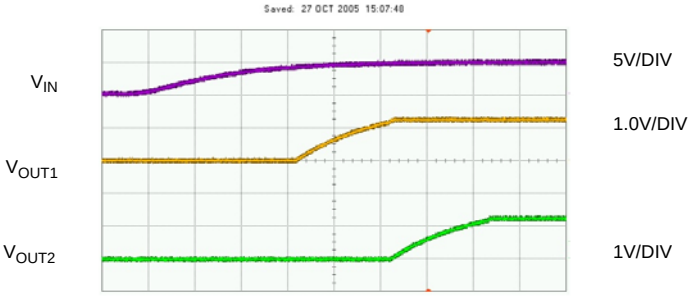


Figure 7: Fast Startup (0.8V, 1.2V, 1.8V, 2.5V, 3.3V)

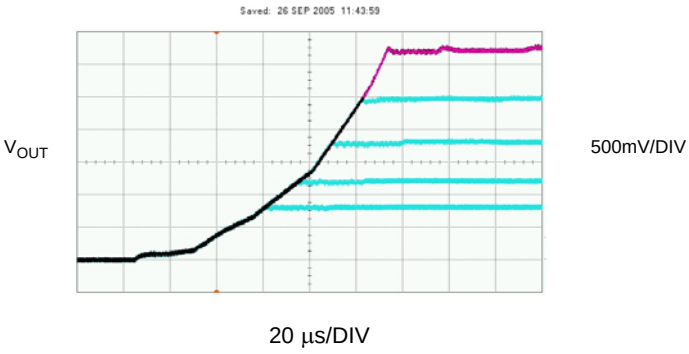


Figure 8: Soft Start up (0.8V, 1.2V, 1.8V, 2.5V, 3.3V)

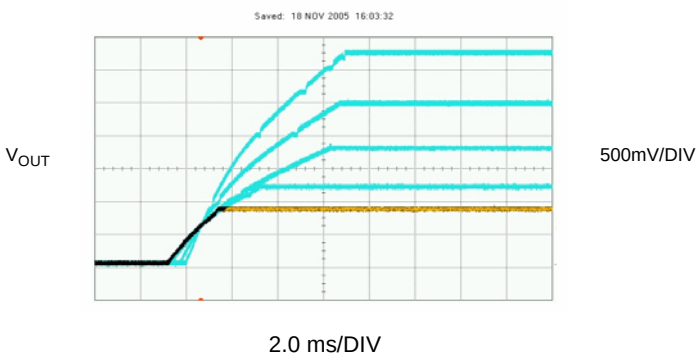
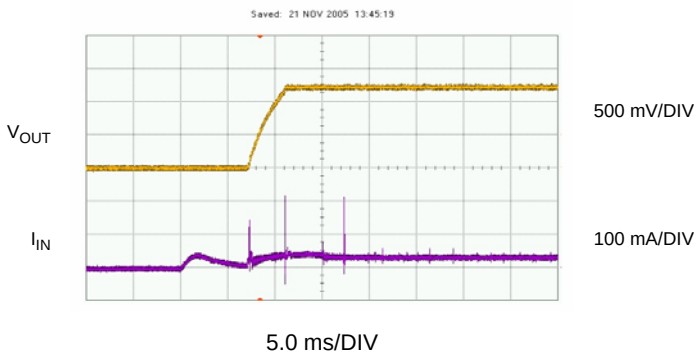


Figure 9: Inrush Current with C_{OUT} = 100 µF



3.2 Output Voltage Settings

3.2.1 Logic Programmability

The output voltage of the step-down switching regulator can be programmed by connecting VSET and PSET pins to SGND and/or SVIN. This can be very useful for standard output voltages.

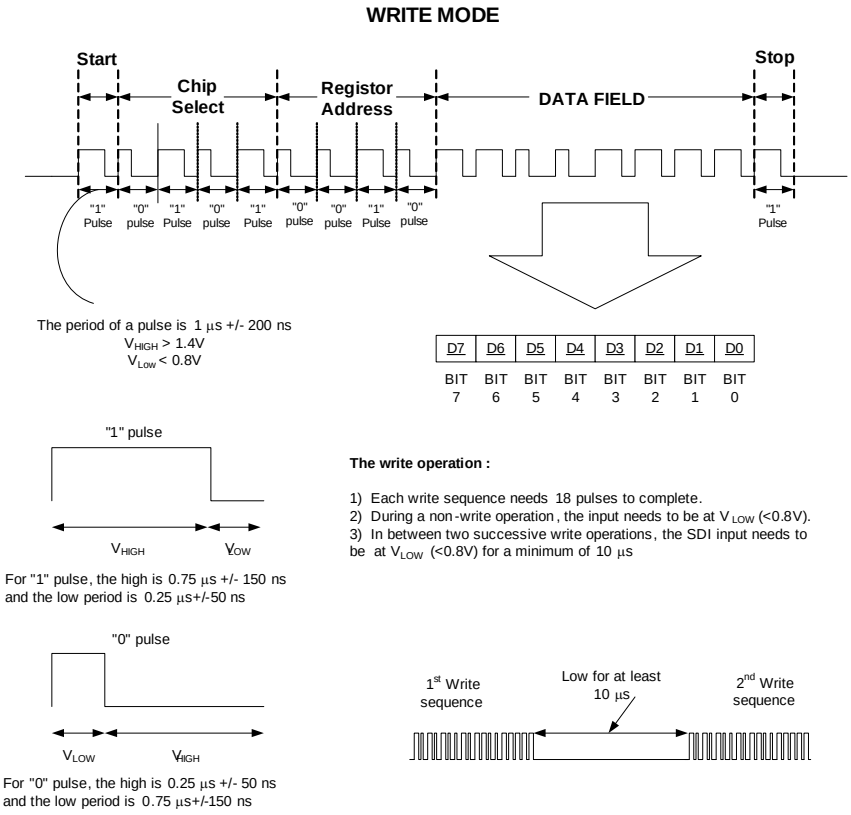
Table 8: Logic Programmability Table

V_{VSET1}	V_{PSET1}	V_{OUT1}	V_{VSET2}	V_{PSET2}	V_{OUT2}
SGND	SGND	1.8V	SGND	SGND	0.8V
SGND	SVIN	2.5V	SGND	SVIN	1.0V
SVIN	SGND	3.0V	SVIN	SGND	1.2V
SVIN	SVIN	3.3V	SVIN	SVIN	1.5V
SGND	$11K \leq R_{PSET2} \leq 475K$	Hi-Z	SGND	$11K \leq R_{PSET2} \leq 475K$	Hi-Z

3.2.2 Serial Programmability

The output voltage of the step-down switching regulator can also program by using 18-bit serial data into the SDI pin.

Figure 10: Serial Programmability



The first 4 bits (MSB-bits) of the data field are used to select the output voltage where the second 4 bits (LSB-bits) of the data field are used to trim the output voltage (percent of output voltage). The default value for the data field is as follows.

Table 9: Default Value of Data Field

	Data Field							
Description	Voltage Set				Percent Set			
Bits	7	6	5	4	3	2	1	0
Default Value	0	0	1	0	0	1	0	0

On power up, the output voltage is set according to R_{PSET} and R_{VSET}. The output voltage can then be field programmed by setting bit 3 and bit 7 to “1”. The output voltage and percent set are selected according to Table 6.

Table 10: Voltage and Percentage Set

	Data Field				V_{OUT} (V)	Data Field				Percent Set
Bits	7	6	5	4		3	2	1	0	
Value	1	0	0	0	0.8	1	0	0	0	-7.5%
	1	0	0	1	1.0	1	0	0	1	-10%
	1	0	1	0	1.2	1	0	1	0	-5.0%
	1	0	1	1	1.5	1	0	1	1	-2.5%
	1	1	0	0	1.8	1	1	0	0	+2.5%
	1	1	0	1	2.5	1	1	0	1	+5.0%
	1	1	1	0	3.0	1	1	1	0	+7.5%
	1	1	1	1	3.3	1	1	1	1	+10%

All combinations of the VSET (Table 8) can be used with all combinations of the PSET (Table 8) to provide maximum flexibility in output voltage selection (Table 6).

To select the output voltage, use the value from Table 7 to program the address bits.

Table 11: Output Voltage Selection

Description	Register Address				Output Voltage Selection
Bits	3	2	1	0	
Value	0	0	0	0	V_{OUT1}
	0	0	1	0	V_{OUT2}

3.2.3 Output Voltage – AnyVoltage™ Technology

The output voltage of the step-down switching regulator is programmed by using Table 8 or Table 9 to select resistor values for VSET and PSET pin. The VSET pin sets the output voltage and the PSET pin trims the set voltage to a percentage value. For example, to program 2.25V output, a 165 kΩ resistor is selected for the VSET pin, and an 11 kΩ resistor is selected for the PSET pin. The 165 kΩ resistor sets the output voltage to 2.5V and the 11 kΩ resistor trims the set voltage by -10%.

Using the VSET resistor's value greater than 619 kΩ or less than 7.68 kΩ disables the step-down switching regulator and sets the SW pin to high impedance. If the VSET resistor's value is outside the 5% tolerance, the output can be either higher or lower than the set voltage.

Using resistor values greater than 619 kΩ or less than 7.68 kΩ for the PSET pin does not affect the set voltage. When the PSET pin is not used, it must be connected to ground. Like the VSET resistor, the percent value can be either higher or lower if the PSET resistor's value is outside the 5% tolerance.

Table 12: AnyVoltage™ Programming Table for 1% Resistors

		PSET								
		-10.0%	-7.5%	-5.0%	-2.5%	0%	2.5%	5.0%	7.5%	10.0%
		11k	18.7k	31.6k	53.6k	GND	97.6k	165k	280k	475k
VSET	11k	0.720	0.740	0.760	0.780	0.800	0.820	0.840	0.860	0.880
	18.7k	0.900	0.925	0.950	0.975	1.000	1.025	1.050	1.075	1.100
	31.6k	1.080	1.110	1.140	1.170	1.200	1.230	1.260	1.290	1.320
	53.6k	1.350	1.388	1.425	1.463	1.500	1.538	1.575	1.613	1.650
	97.6k	1.620	1.665	1.710	1.755	1.800	1.845	1.890	1.935	1.980
	165k	2.250	2.313	2.375	2.438	2.500	2.563	2.625	2.688	2.750
	280k	2.700	2.775	2.850	2.925	3.000	3.075	3.150	3.225	3.300
	475k	2.970	3.053	3.135	3.218	3.300	3.383	3.465	3.548	3.630

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Table 13: AnyVoltage™ Programming Table for 5% Resistors

		PSET								
		-10.0%	-7.5%	-5.0%	-2.5%	0%	2.5%	5.0%	7.5%	10.0%
		11k	18k	30k	51k	GND	100k	160k	270k	470k
VSET	11k	0.720	0.740	0.760	0.780	0.800	0.820	0.840	0.860	0.880
	18k	0.900	0.925	0.950	0.975	1.000	1.025	1.050	1.075	1.100
	30k	1.080	1.110	1.140	1.170	1.200	1.230	1.260	1.290	1.320
	51k	1.350	1.388	1.425	1.463	1.500	1.538	1.575	1.613	1.650
	100k	1.620	1.665	1.710	1.755	1.800	1.845	1.890	1.935	1.980
	160k	2.250	2.313	2.375	2.438	2.500	2.563	2.625	2.688	2.750
	270k	2.700	2.775	2.850	2.925	3.000	3.075	3.150	3.225	3.300
	470k	2.970	3.053	3.135	3.218	3.300	3.383	3.465	3.548	3.630

The VSET and PSET resistors are read once during start-up before the output voltage is turned on. After the output voltage is turned on, the output voltage can change to different values using serial programming interface. Otherwise to configure the output to a different voltage, power has to recycle or the 88PG82XX has to turn OFF and back ON using the shutdown pin.

Figure 11 shows the startup waveforms of the 88PG82XX. Once the input voltage (V_{IN}) is above the under voltage lockout (UVLO) upper threshold (UTH), the VSET and PSET pin become active. Current is first sourced out of PSET pin and then the VSET pin, in exponentially increasing steps. After each step there is a blanking time before the VSET voltage is compared to an internal 1.2V reference. If the VSET voltage is below internal reference voltage, the current source proceeds to the next step. Once the VSET voltage is above the internal reference voltage the sequence stops and the output voltage (VOUT) is allowed to turn on. The Figure 12 shows the VSET waveform for VSET = 2.5V and PSET = –5% output. The 88PG82XX keeps track of how many steps are required to determine the appropriate output voltage. Table 10 provides the number of steps necessary for each output voltage option. Using a VSET resistor of 165 kΩ requires the current source to step 4 times, and a PSET resistor of 31.6 kΩ requires 7 steps.

Figure 11: Startup Sequence

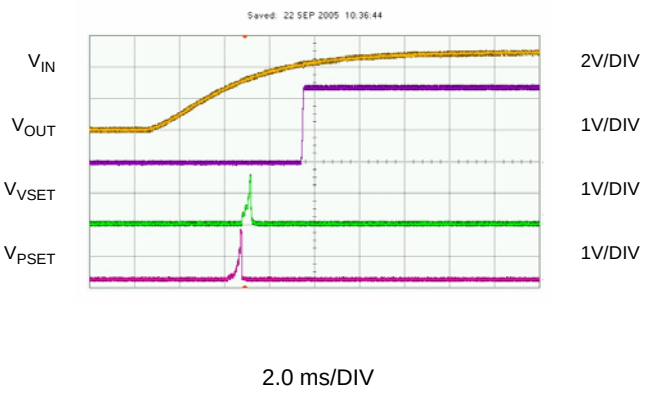


Figure 12: VSET = 2.5V and PSET = -5%

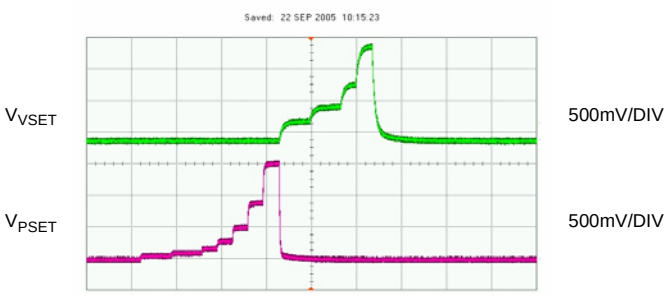


Table 14: Output Voltage Option Steps

Step	VOUT (V)	RVSET (K)
1	0	0
2	3.3	475
3	3.0	280
4	2.5	165
5	1.8	97.6
6	1.5	53.6
7	1.2	31.6
8	1.0	18.7
9	0.8	11

Step	PSET (%)	RSPSET (k)
1	0	0
2	+10	475
3	+7.5	280
4	+5.0	165
5	+2.5	97.6
6	-2.5	53.6
7	-5.0	31.6
8	-7.5	18.7
9	-10	11

The 88PG82XX provides an innovative technique to set the output voltage. During start-up it reads the value of external resistors, which are located outside the regulator's feedback loop to program the output voltage. By placing the output voltage programming resistor outside the regulator's feedback loop, its tolerance does not affect the accuracy of the output voltage. Normally, adjustable regulators use 1% resistors to set the output voltage. However, these resistors are located inside the feedback loop, introducing as much as 2% of initial accuracy error to the output voltage, resulting in an overall initial accuracy of 3%. Whereas, the 88PG82XX initial accuracy is 2% for any of the eight output voltages.

The VSET and PSET pins are sensitive to excessive leakage currents and stray capacitance. The output voltage can potentially be programmed to the lower output voltage if there is contamination, which introduces excessive leakage current on the VSET and PSET pin, especially for a RVSET and RPSET of 470kΩ. The parasitic resistance on these nodes must be greater than 3 MΩ and the stray capacitance must be less than 25 pF; otherwise, a 3.3V output can potentially end up at 3V.

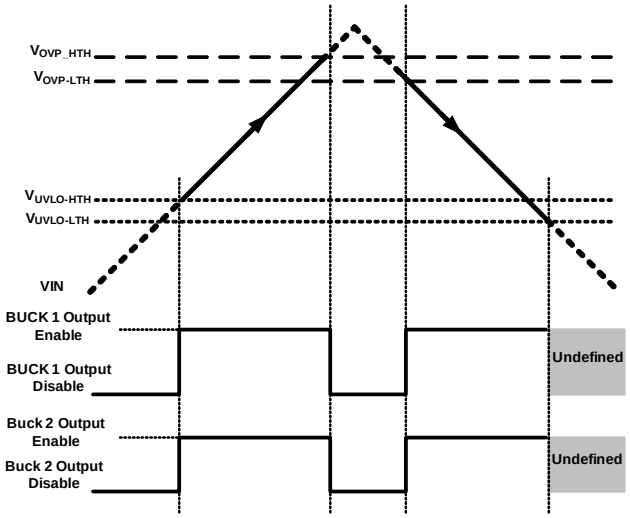
3.3 Undervoltage Lockout (UVLO)

This feature ensures that the internal MOSFETs have adequate voltage levels to operate properly. When the input voltage drops below 2.55V (typical), both MOSFETs are off until the input rises above the upper threshold of 2.65V (typical).

3.4 Over Voltage Protection (OVP)

An over voltage comparator guards against transient overshoots, as well as other serious conditions, that may damage the IC. When the input voltage is rises above 5.7V (typical), both internal MOSFETs are turned off until the input voltage drops below the lower threshold of 5.6V (typical)

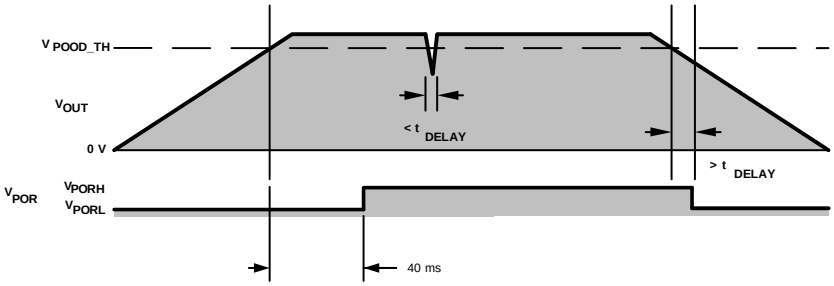
Figure 13: UVLO and OVP Waveforms



3.5 Power-On Reset (POR)

The Power-On Reset (POR) pin is an active-high, open-drain output pin. This output is held low when the output voltage of the step-down regulator is below the threshold. When the output voltage is above the threshold, the Power-On Reset pin goes high 40 ms later. Setting the output voltage greater than 1.35V, the threshold voltage is 0.9% * $V_{OUT\ (typical)}$. Setting the output voltage less than 1.32V, the threshold voltage is V_{OUT} – 130 mV (typical). A built-in 25 µs (t_{DELAY}) delay is incorporated to prevent nuisance tripping.

Figure 14: Power-On Reset Waveforms



3.6 Thermal Shutdown

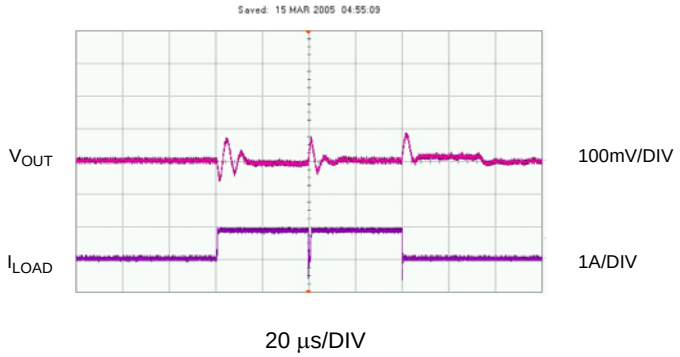
When the junction temperature of the 88PG82XX exceeds 150 °C (typical), the thermal shutdown circuitry disables the step-down regulator. The step-down switching regulator is enabled when the junction temperature is decreased to 105 °C (typical).

3.7 Adaptive Transient Response

The 88PG82XX device's Smart Technology allows the step-down switching regulator to quickly respond to the multiple step loads and maintain stability over a wide range of applications. Figure 15 shows an example of a second step-load applied while the output voltage of the step-down switching regulator increased due to the inductive kick from the first step-load.

Condition: V_{IN} = 5.0V, R_{SVIN} = 10Ω, C_{SVIN} = 0.1 µF, C_{PVIN} = 22 µF, L = 3.3 µH, C_{OUT} = 22 µF, V_{OUT} = 1.2V, I_{LOAD} = 500 mA to 1.5A.

Figure 15: Adaptive Transient Response



The worst case overshoot (V_{SOAR}) during a full-load to light-load transient due to stored inductor energy (Figure 15) can be calculated as:

$$V_{SOAR} = \frac{\Delta I_{LOAD(MAX)}{}^{2} \bullet L}{2 \bullet C_{OUT} \bullet V_{OUT}}$$

Although the V_{SOAR} cannot be eliminated, its amplitude can be controlled based on the C_{OUT} capacitor value. The appropriate C_{OUT} value can easily be calculated for the acceptable V_{SOAR} level for each specific application.

$$C_{OUT} = \frac{\Delta I_{LOAD(MAX)}{}^{2} \bullet L}{2 \bullet V_{SOAR} \bullet V_{OUT}}$$

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4 Functional Characteristics

The following applies unless otherwise noted: T_A = 25°C, R_{SVIN} = 10Ω, C_{SVIN} = 0.1 µF, C_{PVIN} = 2 x 22 µF, L1 = L2 = 3.3 µH, $C_{OUT\ (BUCK1)}$ = 22 µF (ceramic), $C_{OUT\ (BUCK2)}$ = 22 µF (ceramic).

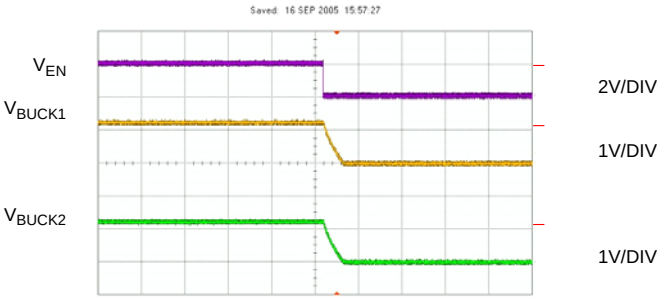
4.1 Start-Up Waveforms

NOTE: When the input voltage rises above the UVLO's upper threshold, there is a delay (4 ms typ) before the step-down regulator's output voltage turns on.

Figure 16: Startup Using the Enable Pin

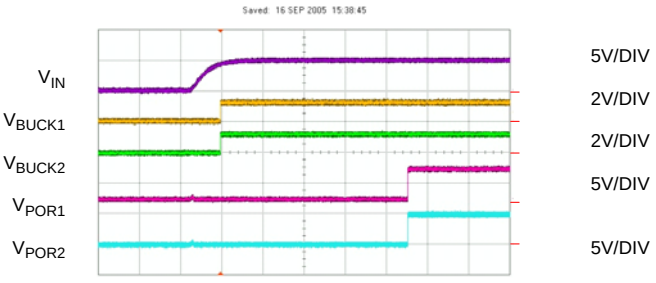
V_{IN} = 5.0V
V_{BUCK1}= 1.2V
V_{BUCK2}= 1.2V
I_{LOAD} = No Load
t_{DLY}= 4.0 ms
SDI = 0V

Figure 17: Turn Off Using the Enable Pin



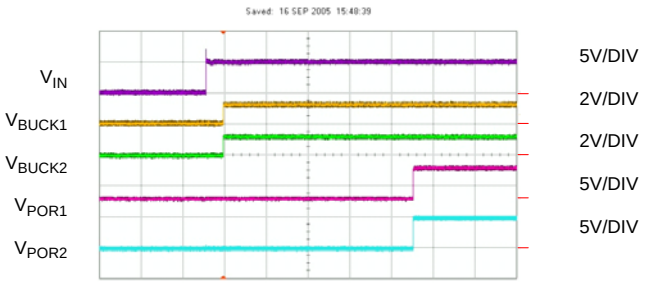
V_{IN} = 5.0V
V_{BUCK1}= 1.2V
V_{BUCK2}= 1.2V
I_{LOAD} = 50 mA

Figure 18: Startup Sequence



V_{IN} = 5.0V
V_{BUCK1}= 1.2V
V_{BUCK2}= 1.2V
I_{LOAD} = No Load
SDI = 0V

Figure 19: Hot Plug



V_{IN} = 5.0V
V_{BUCK1}= 1.2V
V_{BUCK2}= 1.2V
I_{LOAD} = No Load
SDI = 0V

Figure 20: UVLO and OVP Thresholds

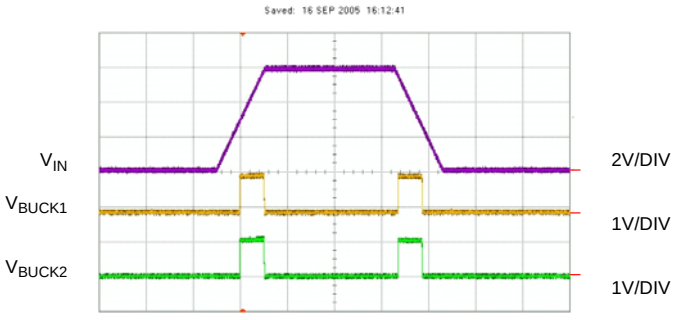
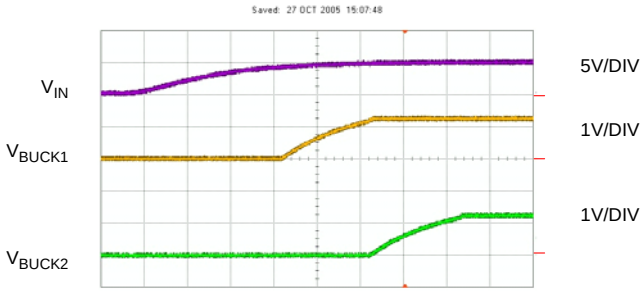


Figure 21: Input Soft Start and Start up Sequence



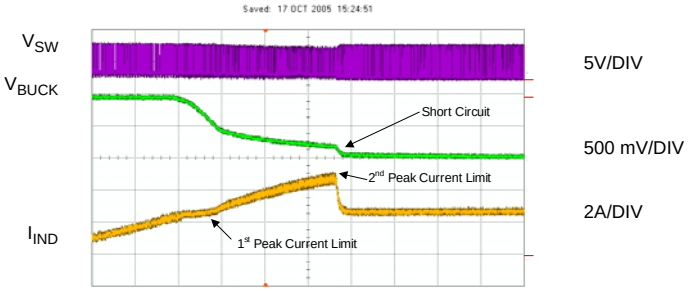
V_{IN} = 0 to 6.0V
V_{BUCK1}= 1.0V
V_{BUCK2}= 1.0V
I_{LOAD1} = 10 mA
I_{LOAD2} = 10 mA

$V_{UVLO(HTH)}$ = 2.608V
$V_{UVLO(LTH)}$= 2.531V
$V_{OVP(HTH)}$ = 5.64V
$V_{OVP(LTH)}$ = 5.32V

V_{IN} = 5V
V_{BUCK1}= 1.2V
V_{BUCK2}= 1.2V
I_{LOAD} = No Load
SDI = SV_{IN}

4.2 Short-Circuit Waveforms

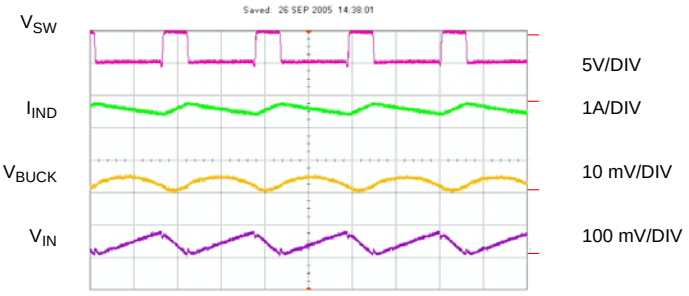
Figure 22: Step-Down Short-Circuit Response



4.3 Switching Waveforms

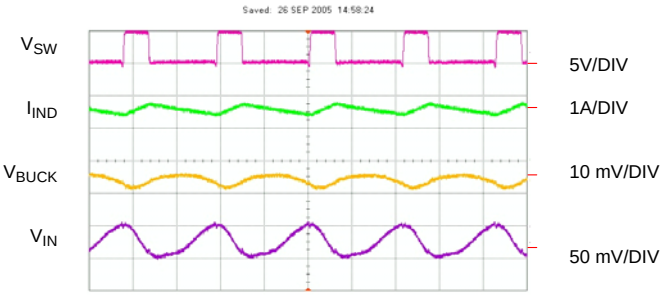
NOTE: For repeatability of measuring output ripple ($V_{BUCK\ (P-P)}$) for the BUCK regulator, the standard test procedure limits the scope bandwidth to 20 MHz and uses a coax cable with very short leads terminated into 50Ω. The coax leads must be routed away from the switching node as much as possible.

Figure 23: Switching Waveforms - PWM mode



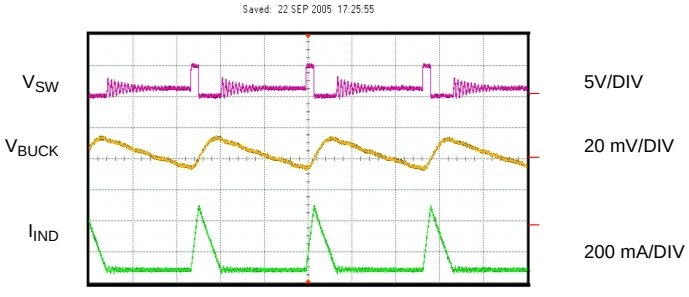
C_{IN} = 22 µF
V_{IN} = 5.0V
V_{BUCK}= 1.2V
I_{OUT} = 1.5A
$V_{OUT(P-P)}$ = 5.4 mV (Note)
$V_{IN(P-P)}$ = 77.3 mV
$I_{IND(P-P)}$ = 412.3 mA
$I_{IND(PK)}$ = 1.73A
Freq = 940 kHz

Figure 24: Switching Waveforms - PWM mode



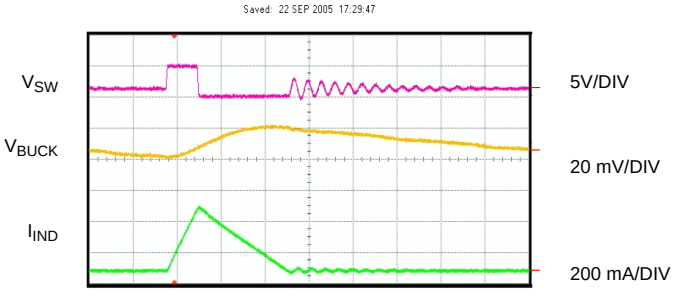
C_{IN} = 2 x 22 µF
V_{IN} = 5.0V
V_{BUCK}= 1.2V
I_{OUT} = 1.5A
$V_{OUT(P-P)}$ = 5 mV (Note)
$V_{IN(P-P)}$ = 58.9 mV
$I_{IND(P-P)}$ = 446.8 mA
$I_{IND(PK)}$ = 1.76A
Freq = 940 kHz

Figure 25: Switching Waveforms - DCM Mode



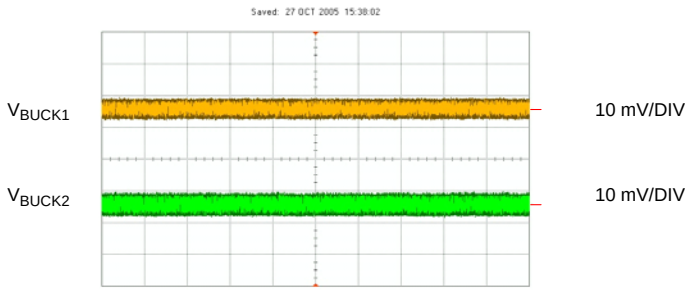
V_{IN} = 5.0V
V_{BUCK}= 1.2V
I_{OUT} = 29 mA
$V_{OUT(P-P)}$ =22 mV (Note)
$I_{IND(PK)}$ = 440 mA
Freq = 187 kHz

Figure 26: Switching Waveforms - DCM Mode-Zoom



V_{IN} = 5.0V
V_{BUCK}= 1.2V
I_{OUT} = 29 mA
Ringing Freq = 6.5 MHz

Figure 27: PWM Output Ripple Voltage

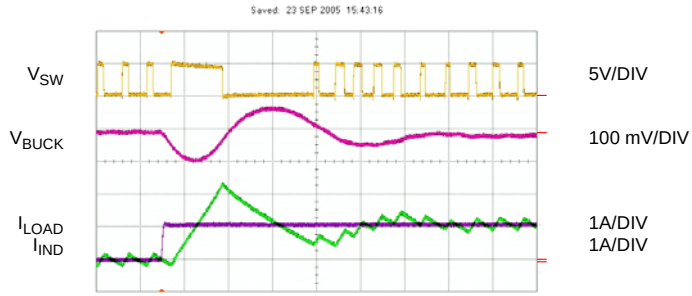


V_{IN} = 5.0V
V_{BUCK1}= 1.2V
V_{BUCK2}= 1.2V
I_{OUT1} = 1.5A
I_{OUT2} = 1.5A
$V_{BUCK1(P-P)}$ = 7.3 mV (Note)
$V_{BUCK2(P-P)}$ = 8.2 mV (Note)

4.4 Load Transient Waveforms

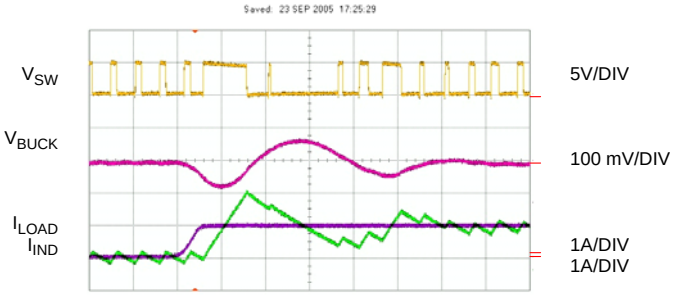
4.4.1 Step-Down Regulator

Figure 28: Fast Load Rise Time



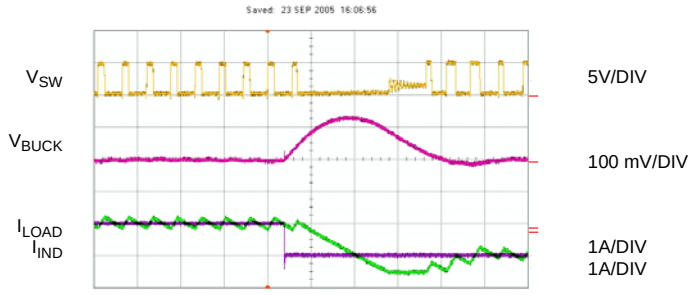
V_{IN} = 5.0V
V_{BUCK}= 1.2V
I_{OUT} = 500 mA to 1.5A
C_{OUT} = 22 µF
t_{RISE} = 13.1 A/µs

Figure 29: Slow Load Rise Time



V_{IN} = 5.0V
V_{BUCK}= 1.2V
I_{OUT} = 500 mA to 1.5A
C_{OUT} = 2 µF
t_{RISE} = 1.2 A/µs

Figure 30: Fast Load Fall Time



2 µs/DIV

V_{IN} = 5.0V

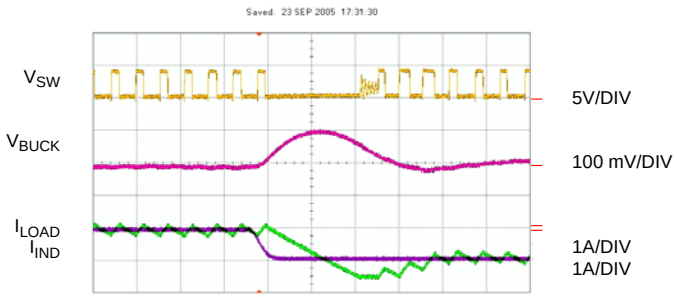
V_{BUCK}= 1.2V

I_{OUT} = 500 mA to 1.5A

C_{OUT} = 22 µF

t_{FALL} = 88 A/µs

Figure 31: Slow Load Fall Time



2 µs/DIV

V_{IN} = 5.0V

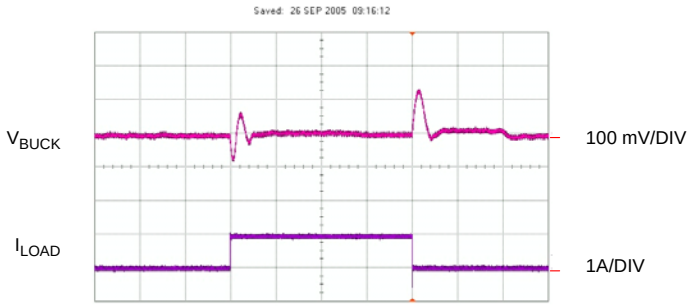
V_{BUCK}= 1.2V

I_{OUT} = 500 mA to 1.5A

C_{OUT} = 22 µF

t_{FALL} = 1.2 A/µs

Figure 32: Load Transient Response



20 µs/DIV

V_{IN} = 5.0V

V_{BUCK}= 1.2V

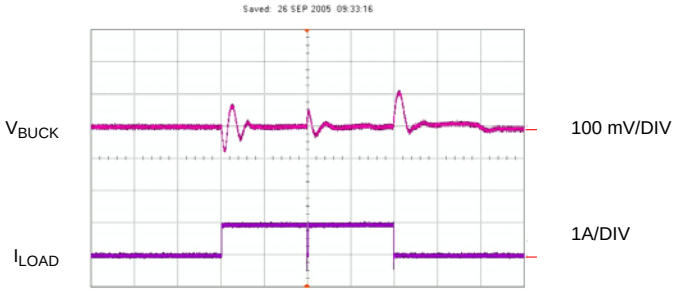
C_{OUT} = 22 µF

I_{LOAD} = 500 mA to 1.5A

t_{RISE} = 13.8 A/µs

t_{FALL} = 121 A/µs

Figure 33: Double-Pulsed Load Response



20 µs/DIV

V_{IN} = 5.0V

V_{BUCK}= 1.2V

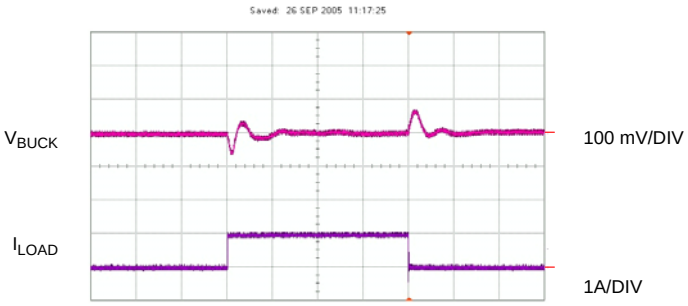
C_{OUT} = 22 µF

I_{LOAD} = 500 mA to 1.5A

t_{RISE} = 11.2 A/µs

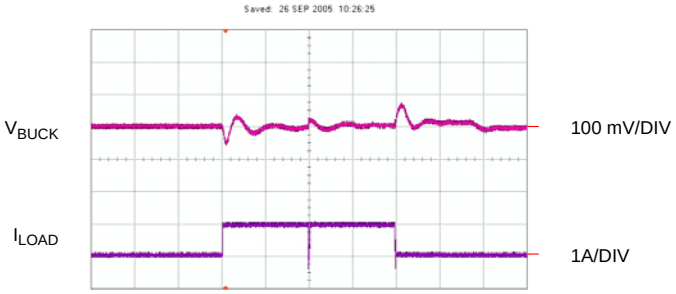
t_{FALL} = 95.3 A/µs

Figure 34: Load Transient Response



V_{IN} = 5.0V
V_{BUCK}= 1.2V
C_{OUT} = 2 x 22 µF
I_{LOAD} = 500 mA to 1.5A
t_{RISE} = 15 A/µs
t_{FALL} = 95.2 A/µs

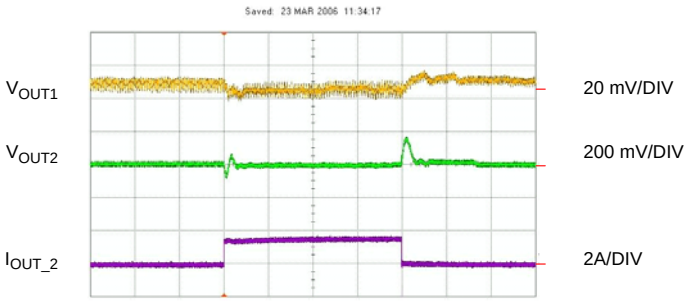
Figure 35: Double-Pulsed Load Response



V_{IN} = 5.0V
V_{BUCK}= 1.2V
C_{OUT} = 2 x 22 µF
I_{LOAD} = 500 mA to 1.5A
t_{RISE} = 13.2 A/µs
t_{FALL} = 91 A/µs

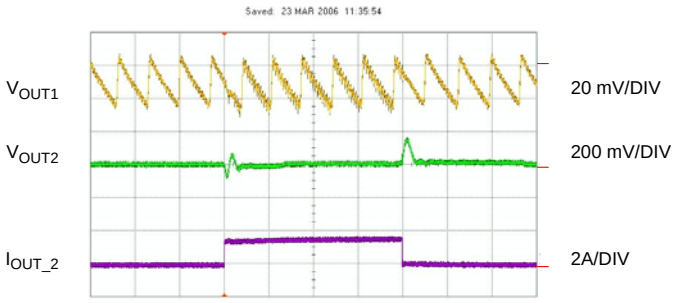
4.4.2 Cross-Talk Waveforms

Figure 36: Cross-talk Continuous Mode



I_{OUT1} = 30 mA
I_{OUT2} = 0.5A to 2.0A
V_{OUT1} = 1.5V
V_{OUT2} = 1.5V

Figure 37: Cross-talk Discontinuous Mode



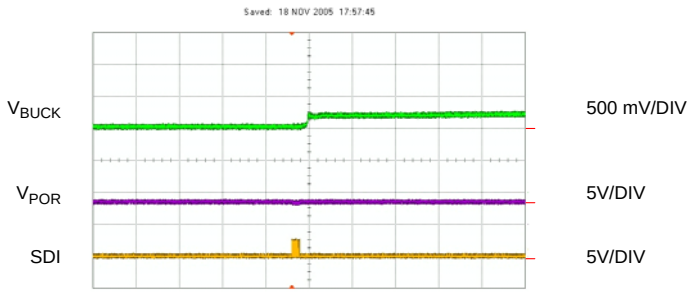
I_{OUT1} = 500 mA
I_{OUT2} = 0.5A to 2.0A
V_{OUT1} = 1.5V
V_{OUT2} = 1.5V

4.5 Output Voltage Transient Waveforms

The following graphs show the effect of changing the step-down regulator's output voltage using the serial interface. Depending on the change in the step-size of the output voltage, the output load, and the output capacitance, the power-on reset pin de-asserts when the changes of the output voltage occur beyond the 25 µs (typical) delay.

4.5.1 Step-Down Regulator

Figure 38: V_{OUT} = 1.0V to 1.2V with No Load



100 µs/DIV

V_{IN} = 5.0V

C_{OUT}= (2 x 22) + 1000 µF

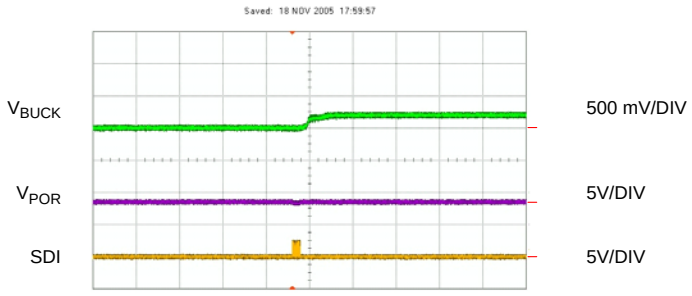
Figure 39: V_{OUT} = 1.0V to 1.5V with No Load

100 µs/DIV

V_{IN} = 5.0V

C_{OUT}= (2 x 22) +1000 µF

Figure 40: V_{OUT} = 1.0V to 1.2V with I_{LOAD} = 1.5A

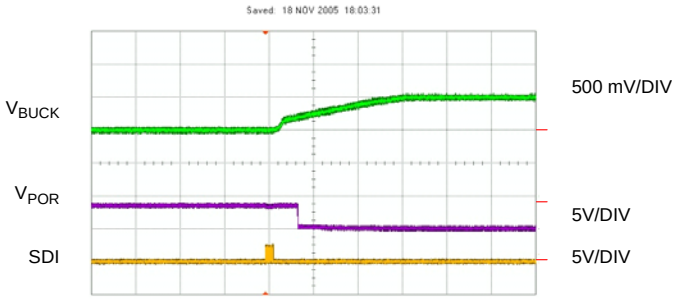


100 µs/DIV

V_{IN} = 5.0V

C_{OUT}= (2 x 22) + 1000 µF

Figure 41: V_{OUT} = 1.0V to 1.5V with I_{LOAD} = 1.5A

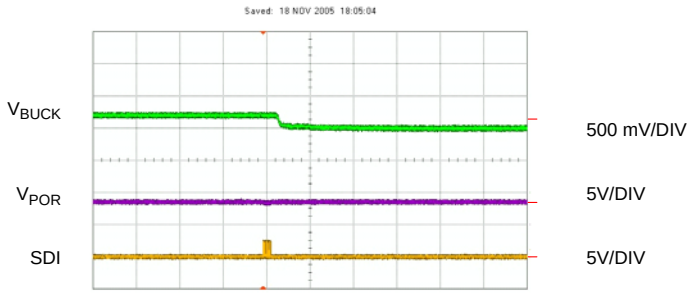


100 µs/DIV

V_{IN} = 5.0V

C_{OUT}= (2 x 22) +1000 µF

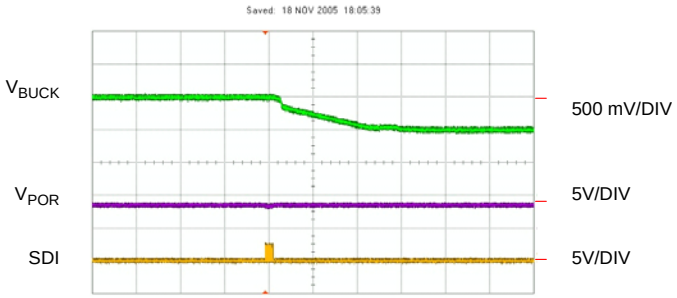
Figure 42: V_{OUT} = 1.2V to 1.0V with I_{LOAD} = 1.5A



V_{IN} = 5.0V

C_{OUT}= (2 x 22)+1000 µF

Figure 43: V_{OUT} = 1.5V to 1.0V with I_{LOAD} = 1.5A



V_{IN} = 5.0V

C_{OUT}= (2 x 22)+1000 µF

4.6 Line Transient Waveforms

Figure 44: Line Transient @ V_{IN} = 3.6V

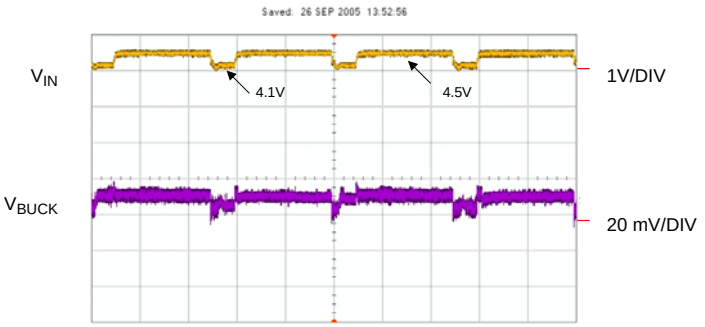
V_{IN} = 3.6V

C_{IN}= 22 µF

V_{BUCK} = 1.2V

I_{LOAD} = 1.5A

Figure 45: Line Transient @ V_{IN} = 4.5V



V_{IN} = 4.5V

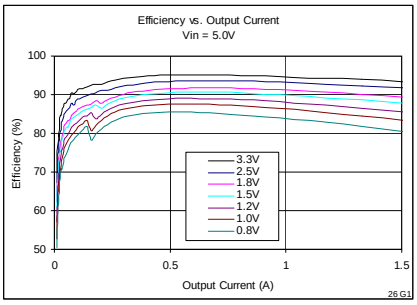
C_{IN}= 22 µF

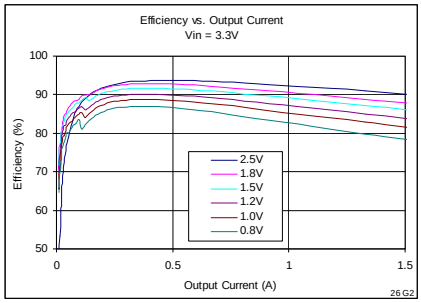
V_{BUCK} = 1.2V

I_{LOAD} = 1.5A

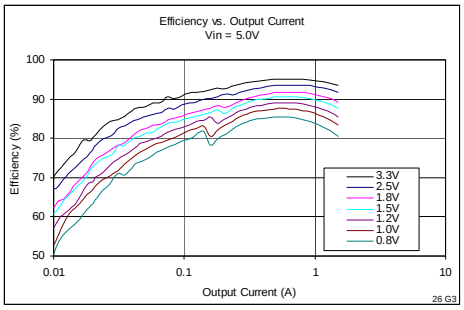
5 Typical Characteristics

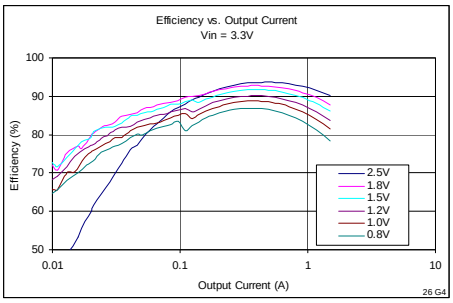
5.1 Efficiency Graphs



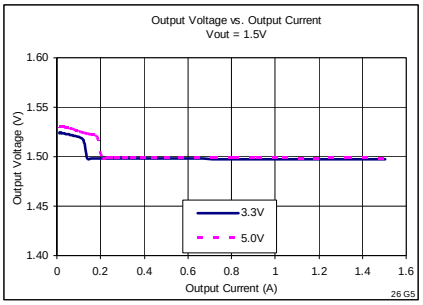


5.1.1 Efficiency Graphs in Log Scale

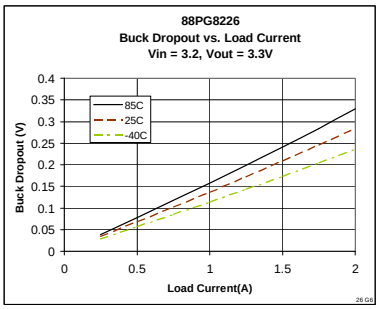




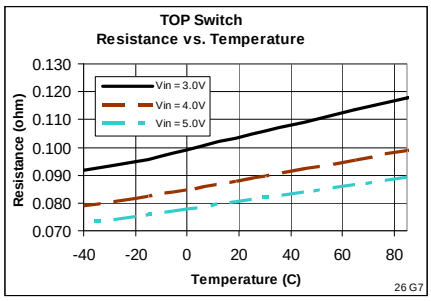
5.2 Load Regulation

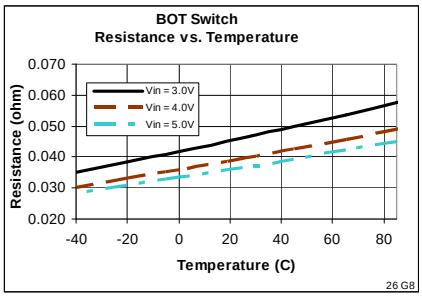


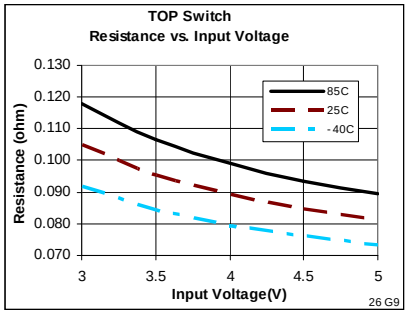
5.3 Dropout Voltage

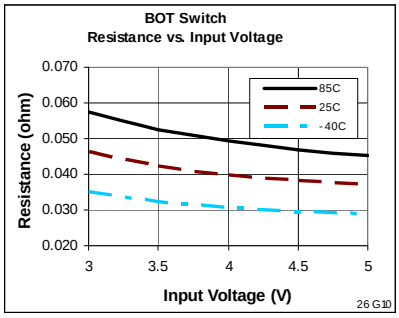


5.4 RDS (ON) Resistance



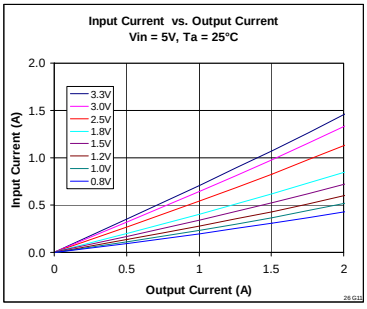


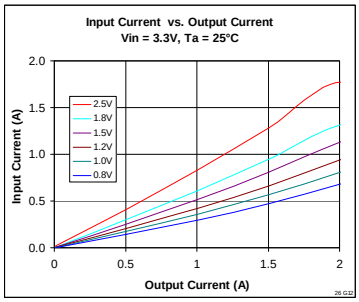


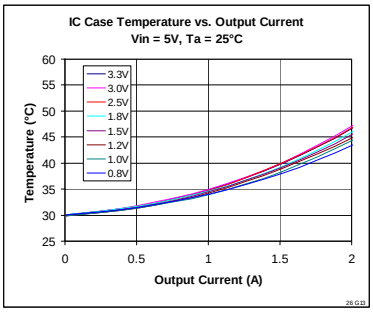


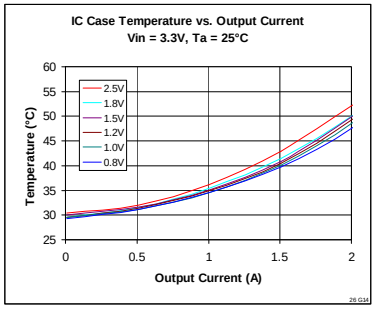
5.5 IC Case and Inductor Temperature

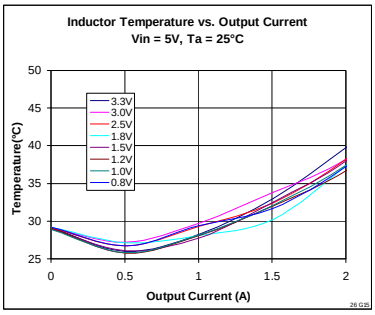
The following data was taken using a 1.4 square inch PCB 1 oz. copper and L = 1.2 µH. Actual results depend upon the size of the PCB proximity to other heat emitting components.

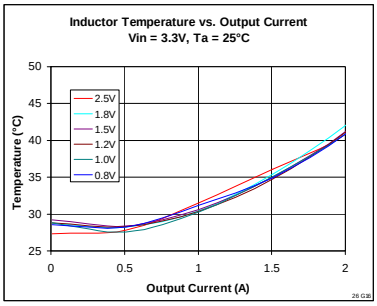


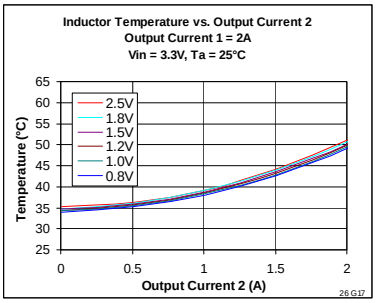


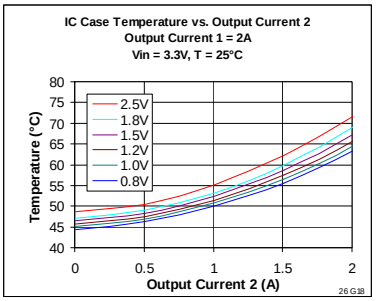






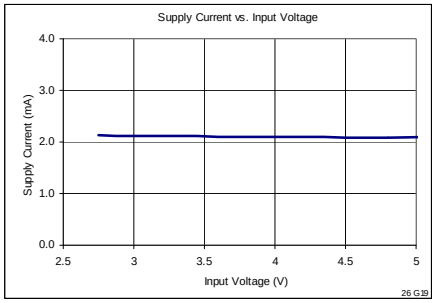




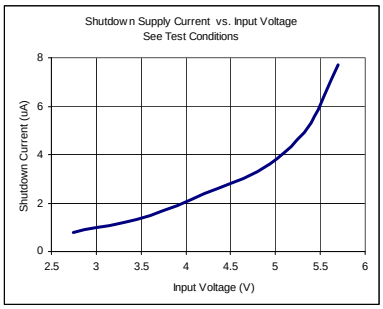


5.6 Input Voltage Graphs

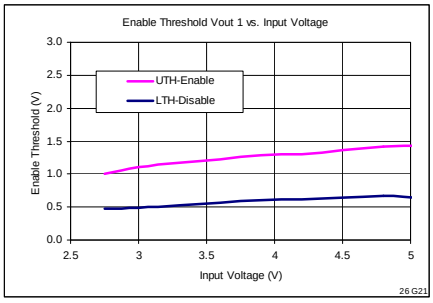
The 88PG8237 part was used to determine the following graph data.



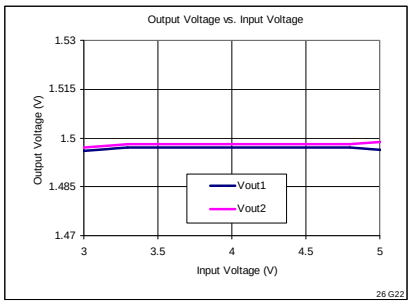
Load = No Load



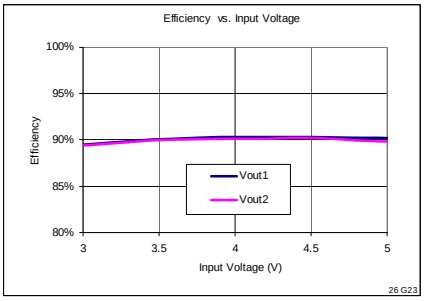
V_{EN} = GND



5.6.1 Step-Down Regulator

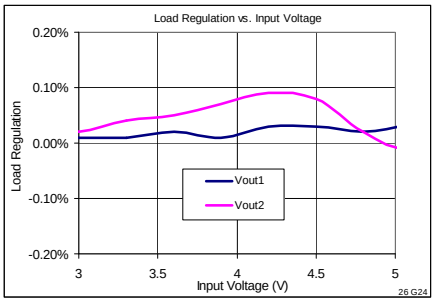


$I_{OUT(BUCK)}$ = 375 mA



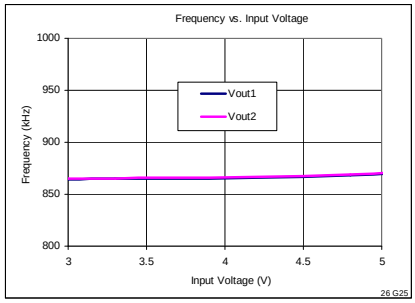
$V_{OUT(BUCK)}$ = 1.5V

$I_{OUT(BUCK)}$ = 0.75A



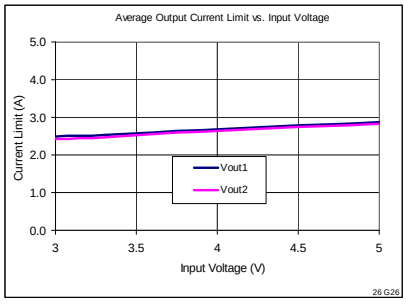
$V_{OUT(BUCK)}$ = 1.5V

$I_{OUT(BUCK)}$ = 0.375A - 1.5A



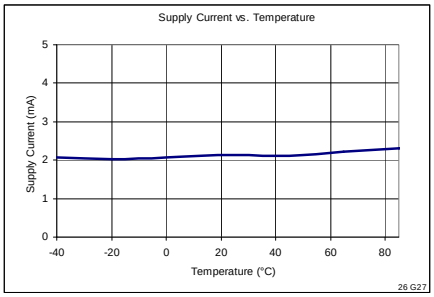
$V_{OUT(BUCK)}$ = 1.5V

$I_{OUT(BUCK)}$ = 0.75A



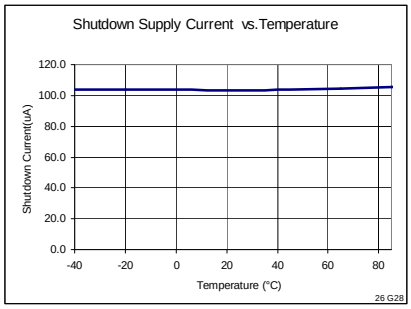
5.7 Temperature Graphs

The 88PG8237 part was used to determine the following graph data.



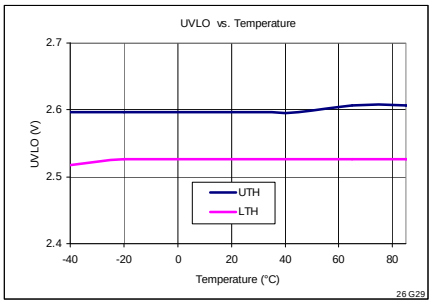
$I_{OUT(BUCK1)}$ = No Load

$I_{OUT(BUCK2)}$ = No Load



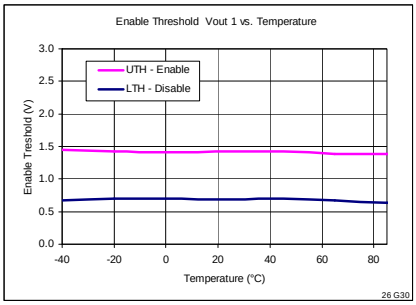
V_{IN} = 5V

V_{EN} = GND



V_{IN}= 5V

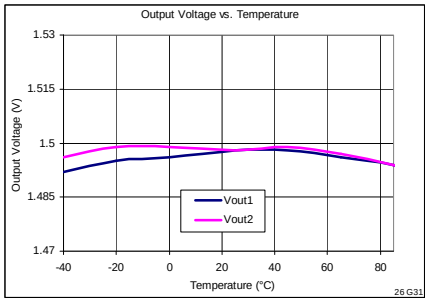
$I_{OUT(BUCK)}$ = 10mA



V_{IN} = 5V

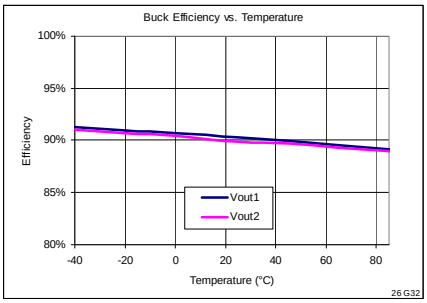
$I_{OUT(BUCK)}$ = 10mA

5.7.1 Step-Down regulator



V_{IN} = 5.0V

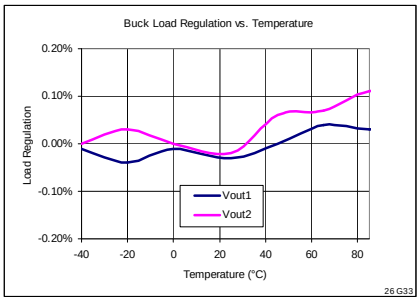
$I_{OUT(BUCK)}$ = 750 mA



V_{IN} = 5.0V

$V_{OUT(BUCK)}$ = 1.5V

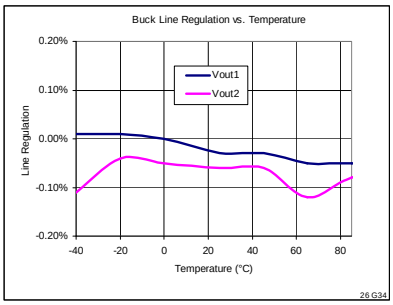
$I_{OUT(BUCK)}$ = 1.5A



V_{IN} = 5.0V

$V_{OUT(BUCK)}$ = 1.5V

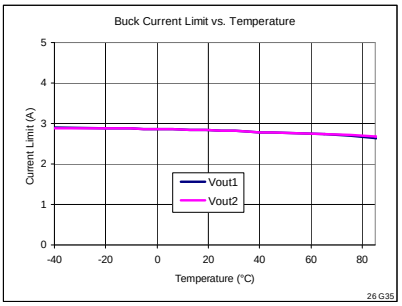
$I_{OUT(BUCK)}$ = 750 mA - 3A

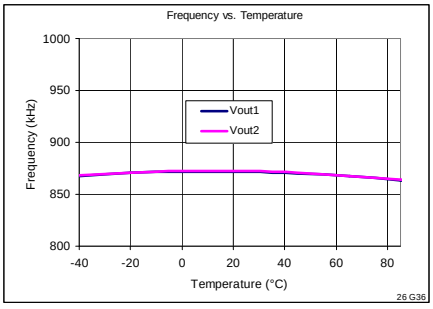


V_{IN} = 3.0V - 5.0V

$V_{OUT(BUCK)}$ = 1.5V

$I_{OUT(BUCK)}$ = 1.5A





V_{IN} = 5.0V

$I_{OUT(BUCK)}$ = 1.5A

6 Applications Information

6.1 PC Board Layout Considerations and Guidelines

The PC board layout is very critical in any switching converter. An improper layout can contribute to system instability, excessive EMI (Electro-magnetic interference), and high switching loss. Follow these basic guidelines for good PC layout:

1. This is a 2-layer board with 1 ground plane and 1 routing layer.
2. Copy the layout input Figure 48 and Figure 49 as much as possible and use the recommended BOM in Table 15. Contact the factory where substitutions are made.
3. Review the recommended solder pad layout and notes on page 50.
4. Do not replace the Ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor as long as the Ceramic input capacitor is placed next to the IC. If Tantalum input capacitor is used, it must be rated for switching regulator applications and the operating voltage must be derated by 50%.
5. Any type of capacitor can be placed in parallel with the output capacitor.
6. Low-ESR capacitors like the POSCAP from Sanyo can replace the Ceramic output capacitors as long as the capacitor value is the same or greater. Note that the Ceramic capacitors provide the lowest noise and smallest foot print solution.
7. Use planes for the ground, input and output power to maintain good voltage filtering, and to keep power losses low.
8. If there is not enough space for a power plane for the input supply, then the input supply trace must be at least 3/8 inch wide.
9. If there is not enough space for a power plane for the output supplies, then place the output as close to the load as possible with a trace at least 3/8 inch wide.
10. Do not lay out the inductor first. The input capacitor placement is the most critical for proper operation. The AC current circulating through the input capacitor and loop 1 (LP1) are square wave with rise and fall times of 8 ns and slew rates as high as 300 A/µs (see Figure 46). At these fast slew rates, stray PCB inductance can generate a voltage spike as high as 3V per inch of PCB trace, VIND = L * di/dt. Therefore, the ceramic input capacitor (C2 and C5) must be placed as close as possible to the PVIN and PGND pins with a short and wide trace as possible. Also, the PVIN and PGND traces must be placed on the top layer. This will isolate the fast AC currents from interfering with the analog ground plane.
11. The 88PG82XX has two internal grounds, analog (SGND) and power (PGND). The analog ground ties to all the noise sensitive signals (PSET, VSET, and SVIN) while the power ground ties to the higher current power paths. Noise on an analog ground can cause problems with the IC's internal control and bias signals. For this reason, separate analog and power ground traces are recommended. The signal ground is connected to the power ground at one point, which is the (-) terminal of the output capacitor.
12. Keep loop 2 (LP2) as small as possible and connect the (-) terminal of the output capacitor as close to the (-) terminal of the input capacitor. A back-to-back placing of bypass capacitors, as shown in Figure 48, is recommended for best results.
13. Keep the switching node (SW) away from the SFB pin and all sensitive signal nodes, minimizing capacitive coupling effects. If the SFB trace must cross the SW node, cross it at a right angle.
14. Try not to route analog or digital lines in close proximity to the power supply especially the VSW node. If this can't be avoided, shield these lines with a power plane placed between the VSW node and the signal lines.

15. PVIN1 and PVIN2 must be connected together and should not be separated.
16. The type of solder paste recommended for QFN packages is “No clean”, due to the difficulty of cleaning flux residues from beneath the QFN package.

Figure 46: Simpified Schematic

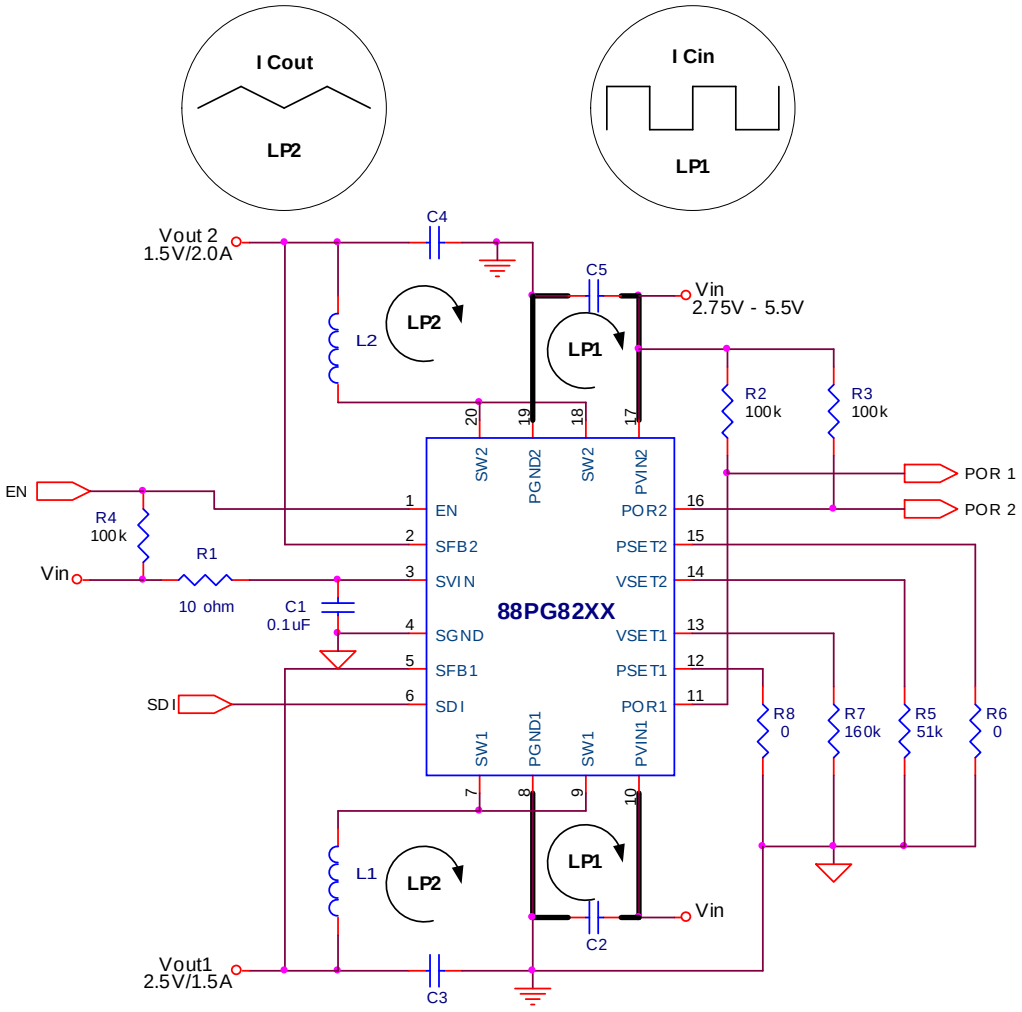
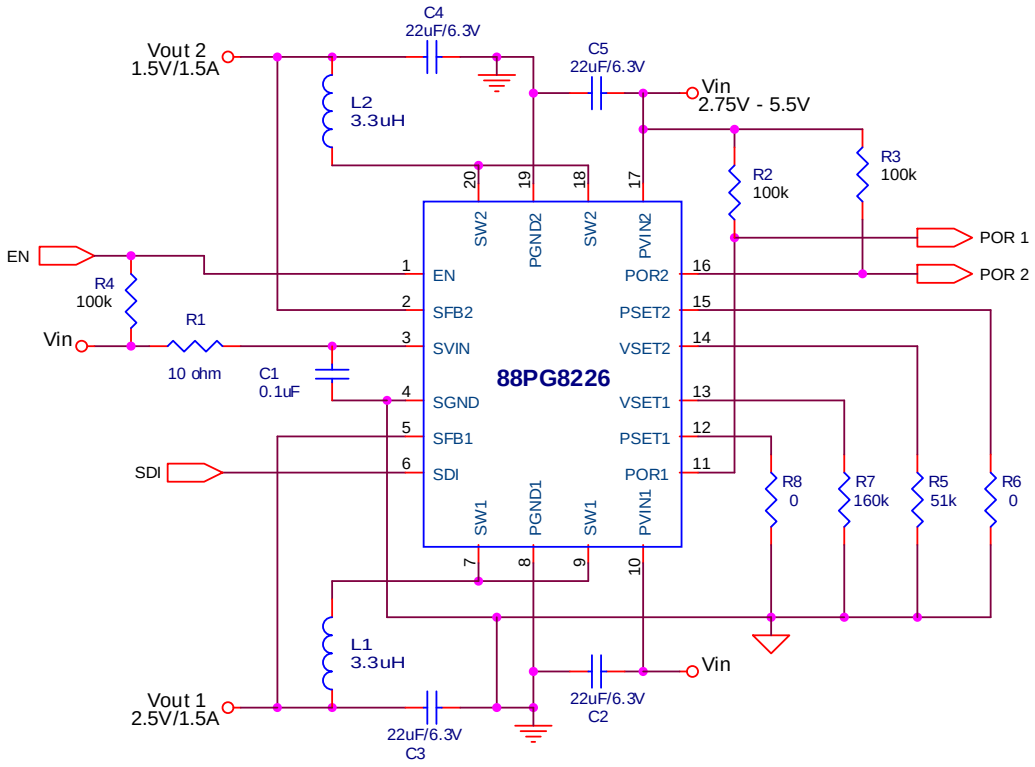


Figure 47: PC Board Schematic



6.1.1 PC Board Layout Examples for 88PG82XX

- Actual board size = 570 mil x 630 mil; Area = 0.359 Sq. Inches.
- Total copper layers = 2 (Top and Bottom)
- All the components are on the top layer

Figure 48: Top Silk-Screen, Top Traces, Vias, and Top Copper (Not to Scales)

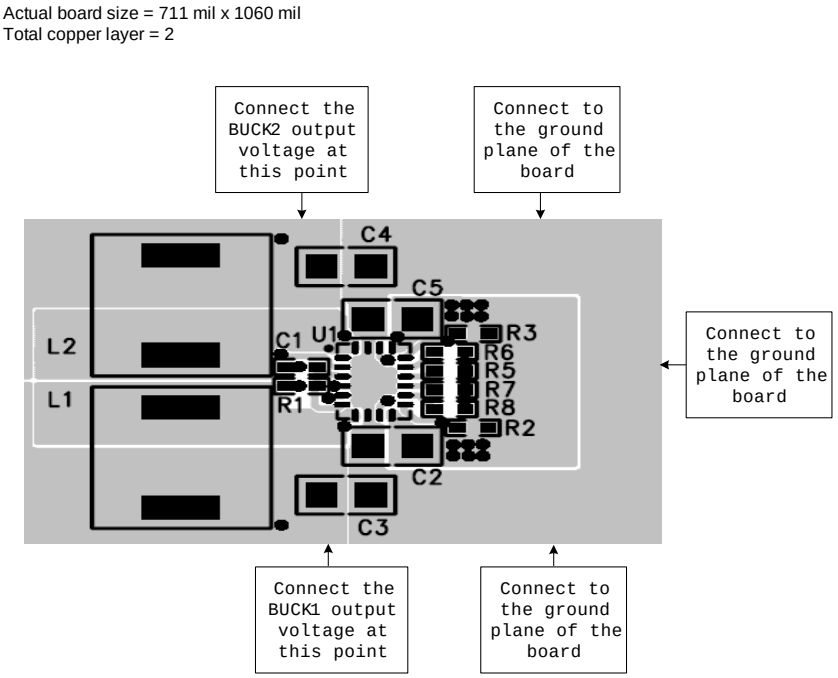
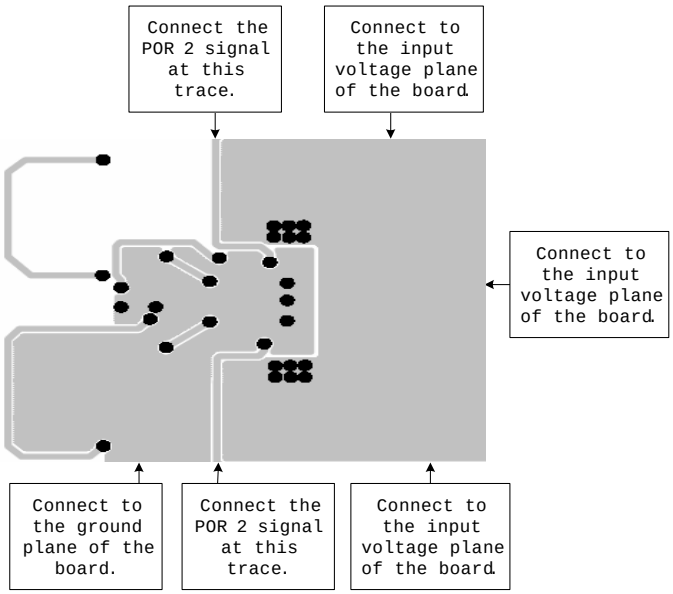


Figure 49: Bottom Silk Screen, Bottom Trace, Vias, and Bottom Copper (Not to Scale)



6.1.2 Bill of Materials (BOM)

The following tables list the components used with the 88PG82XX.

Table 15: BOM for 88PG82XX

Item	Qty.	Ref.	Manufacturer Part #	Manufacturer	Description
1	1	U1	**88PG8204**	**Marvell Semiconductor**	1MHz, Dual (0.75A/0.75A) Step-Down Regulator
2	1	C1	ECJ-1VB1C104K	Pansonic - ECG	0.1µF, ±10%,X7R,16V,0603 Case Size, Ceramic
3	4	C2,C3, C4,C5	C2012X5R0J106MT	TDK	10µF, ±20%,X5R,6.3V,0805 Case Size, Ceramic
4	2	L1,L2	1117AS-4R7M	Toko	4.7µH, 0.91A, 170mΩ, H=1mm, L=2.8mm, W=3.0mm
5	1	R1	ERJ-2RKF10R0X	Pansonic - ECG	10.0Ω, 1/16W, 1%, 0402 Case Size
6	1	R2,R3, R4	ERJ-3GEYJ104V	Pansonic - ECG	100Ω, 1/10W, 5%, 0603 Case Size
7	4	R5,R6, R7,R8		Pansonic - ECG	See AnyVoltage Programming Table 1/16W, 1%, 0402 Case Size
Item	**Qty.**	**Ref.**	**Manufacturer Part #**	**Manufacturer**	**Description**
1	1	U1	**88PG8216**	**Marvell Semiconductor**	1MHz, Dual (1.0A/1.5A) Step-Down Regulator
2	1	C1	ECJ-1VB1C104K	Pansonic - ECG	0.1µF, ±10%,X7R,16V,0603 Case Size, Ceramic
3	1	C3	C2012X5R0J106MT	TDK	10µF, ±20%,X5R,6.3V,0805 Case Size, Ceramic
4	3	C2,C4, C5	C2012X5R0J226MT	TDK	22µF, ±20%,X5R,6.3V,0805 Case Size, Ceramic
5	1	L1	A918CY-4R7M=P3	Toko	4.7µH, 0.91A, 170mΩ, H=1mm, L=2.8mm, W=3.0mm
6	1	L2	A918CY-2R0M=P3	Toko	3.3µH, 1.99A, 39mΩ, H=2mm, L=6.2mm, W=6.3mm
7	1	R1	ERJ-2RKF10R0X	Pansonic - ECG	10.0Ω, 1/16W, 1%, 0402 Case Size
8	3	R2,R3, R4	ERJ-3GEYJ104V	Pansonic - ECG	100Ω, 1/10W, 5%, 0603 Case Size
9	4	R5,R6, R7,R8		Pansonic - ECG	See AnyVoltage Programming Table 1/16W, 1%, 0402 Case Size
Item	**Qty.**	**Ref.**	**Manufacturer Part #**	**Manufacturer**	**Description**
1	1	U1	**88PG8227**	**Marvell Semiconductor**	1MHz, Dual (1.5A/2.0A) Step-Down Regulator
2	1	C1	ECJ-1VB1C104K	Pansonic - ECG	0.1µF, ±10%,X7R,16V,0603 Case Size, Ceramic
3	2	C2,C5	C2012X5R0J226MT	TDK	22µF, ±20%,X5R,6.3V,0805 Case Size, Ceramic
4	2	C3,C4	C2012X5R0J226MT	TDK	22µF, ±20%,X5R,6.3V,0805 Case Size, Ceramic
5	1	L1	A918CY-3R3M=P3	Toko	3.3µH, 1.99A, 39mΩ, H=2mm, L=6.2mm, W=6.3mm
6	1	L2	A918CY-2R0M=P3	Toko	2.0µH, 2.47A, 24mΩ, H=2mm, L=6.2mm, W=6.3mm
7	1	R1	ERJ-2RKF10R0X	Pansonic - ECG	10.0Ω, 1/16W, 1%, 0402 Case Size
8	3	R2,R3, R4	ERJ-3GEYJ104V	Pansonic - ECG	100Ω, 1/10W, 5%, 0603 Case Size

Table 15: BOM for 88PG82XX

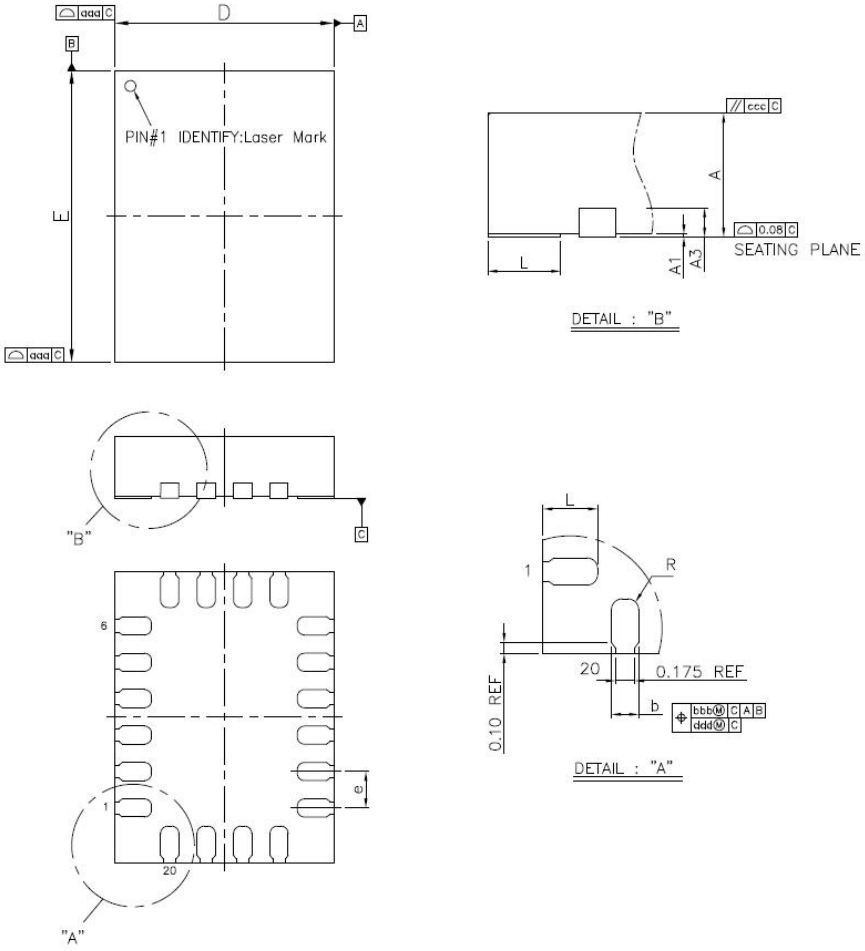
Item	Qty.	Ref.	Manufacturer Part #	Manufacturer	Description
9	4	R5,R6, R7,R8		Pansonic - ECG	See AnyVoltage Programming Table 1/16W, 1%, 0402 Case Size
Item	**Qty.**	**Ref.**	**Manufacturer Part #**	**Manufacturer**	**Description**
1	1	U1	**88PG8226**	**Marvell Semiconductor**	1MHz, Dual (1.5A/1.5A) Step-Down Regulator
2	1	C1	ECJ-1VB1C104K	Pansonic - ECG	0.1µF, ±10%, X7R, 16V, 0603 Case Size, Ceramic
3	2	C2,C5	C2012X5R0J226MT	TDK	22µF, ±20%, X5R, 6.3V, 0805 Case Size, Ceramic
4	2	C3,C4	C2012X5R0J226MT	TDK	22µF, ±20%, X5R, 6.3V, 0805 Case Size, Ceramic
5	2	L1,L2	A918CY-3R3M=P3	Toko	3.3µH, 1.99A, 39mΩ, H=2mm, L=6.2mm, W=6.3mm
6	1	R1	ERJ-2RKF10R0X	Pansonic - ECG	10.0Ω, 1/16W, 1%, 0402 Case Size
7	3	R2,R3, R4	ERJ-3GEYJ104V	Pansonic - ECG	100Ω, 1/10W, 5%, 0603 Case Size
8	4	R5,R6, R7,R8		Pansonic - ECG	See AnyVoltage Programming Table 1/16W, 1%, 0402 Case Size
Item	**Qty.**	**Ref.**	**Manufacturer Part #**	**Manufacturer**	**Description**
1	1	U1	**88PG8237**	**Marvell Semiconductor**	1MHz, Dual (2.0A/2.0A) Step-Down Regulator
2	1	C1	ECJ-1VB1C104K	Pansonic - ECG	0.1µF, ±10%, X7R, 16V, 0603 Case Size, Ceramic
3	2	C2,C5	C2012X5R0J226MT	TDK	22µF, ±20%, X5R, 6.3V, 0805 Case Size, Ceramic
4	2	C3,C4	C2012X5R0J226MT	TDK	22µF, ±20%, X5R, 6.3V, 0805 Case Size, Ceramic
5	2	L1,L2	A918CY-2R0M=P3	Toko	2.0µH, 2.47A, 24mΩ, H=2mm, L=6.2mm, W=6.3mm
6	1	R1	ERJ-2RKF10R0X	Pansonic - ECG	10.0Ω, 1/16W, 1%, 0402 Case Size
7	3	R2,R3, R4	ERJ-3GEYJ104V	Pansonic - ECG	100Ω, 1/10W, 5%, 0603 Case Size
8	4	R5,R6, R7,R8		Pansonic - ECG	See AnyVoltage Programming Table 1/16W, 1%, 0402 Case Size

Table 16: Ceramic Capacitor Cross Reference

Manufacturer	Manufacturer Part #	Description
Taiyo-Yuden	CE JMK212BJ226MG-T	22µF
TDK	C2012X5R0J226MT	
Murata	GRM21BR60J226ME39L	
Taiyo-Yuden	CE JMK212BJ106MG-T	10µF
TDK	C2012X5R0J106MT	
Murata	GRM219R60J106KE190	
Taiyo-Yuden	RM LMK105BJ104KV-F	0.1µF
TDK	C1005X5R1A104K	

7 Mechanical Drawing

7.1 88PG82XX Mechanical Drawing



7.2 Dimensions

Table 17: Package Dimensions

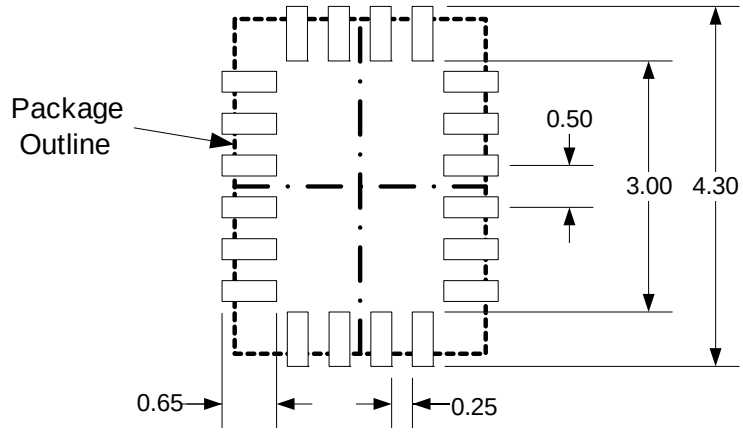
Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.80	0.85	1.00
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.20	0.25	0.30
D		3.00 BSC	
E		4.00 BSC	
e		0.50 BSC	
L	0.45	0.50	0.55
R	0.10		
aaa			0.15
bbb			0.10
ccc			0.10
ddd			0.05

Notes:

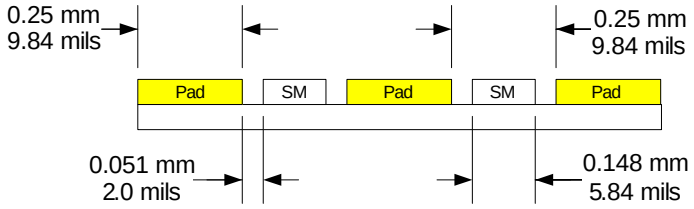
1. CONTROLLING DIMENSION: MILLIMETER
2. SPECIAL CHARACTERISTICS C CLASS: ccc

7.3 Typical Pad Layout Dimensions

7.3.1 Recommeded Solder Pad Layout



4x3 QFN-20
Land Pattern (mm)



QFN Lead with
Non-Solder Mask Defined Terminal
(Not to Scale)

Notes:

1. TOP VIEW
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE IN MILLIMETERS
4. OVERSIZE SOLDER MASK BY 4 MILS OVER PAD SIZE (2 MIL ANNULAR RING)
5. 0.148mm SOLDER MASK (SM) BETWEEN PADS
6. TOLERANCE ±0.05mm

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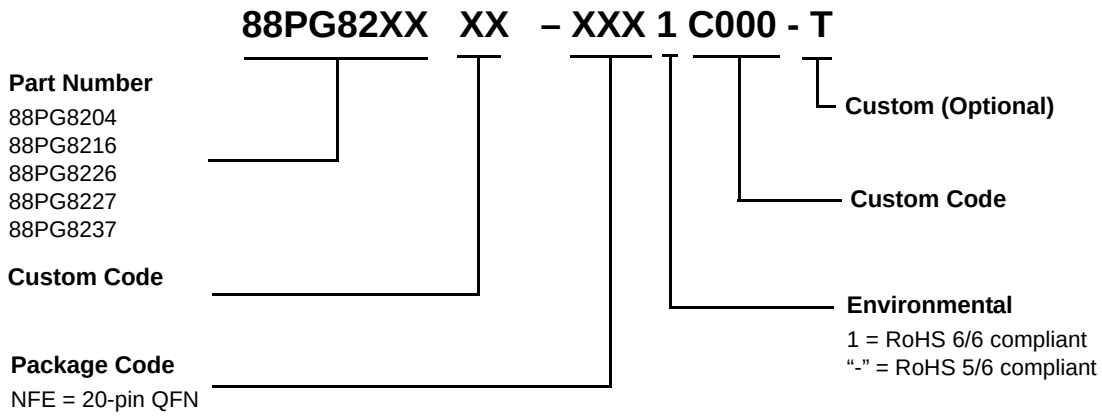
8 Ordering Information

8.1 Ordering Part Numbers and Package Markings

Figure 50 shows the ordering part numbering scheme for the 88PG82XX devices. Contact Marvell® FAEs or sales representatives for complete ordering information.

Figure 50: Sample Part Number



8.2 Sample Ordering Part Number

The standard ordering part numbers for the respective solutions are as follows:

Table 18: 88PG82XX Ordering Part Numbers[1]

Booking Part Number	Marking	Current		Ambient Temperature Range[2]	Package[3]
		V_{OUT1}	V_{OUT2}		
88PG8204A0-NFE1C000	G204	0.75A	0.75A	-40°C to 85°C	3 X 4 QFN-20
88PG8216A1-NFE1C000	G216	1.0A	1.5A	-40°C to 85°C	3 X 4 QFN-20
88PG8226A1-NFE1C000	G226	1.5A	1.5A	-40°C to 85°C	3 X 4 QFN-20
88PG8227A1-NFE1C000	G227	1.5A	2.0A	-40°C to 85°C	3 X 4 QFN-20
88PG8237A1-NFE1C000	G237	2.0A	2.0A	-40°C to 85°C	3 X 4 QFN-20

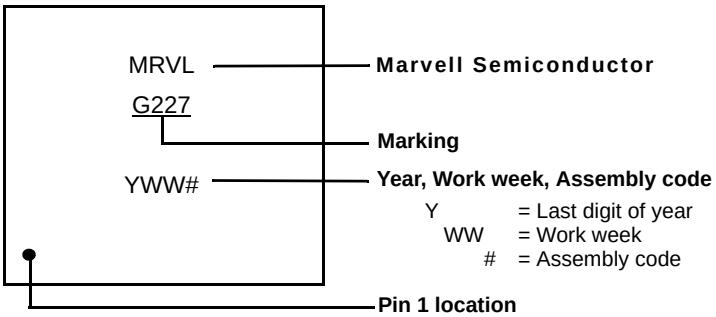
1. Contact Marvell for details.
2. Specifications over the -40C to 85C operating temperature range are assured by design, characterization and correlation with statistical process controls.
3. Package dimensions are in mm.

8.3 Package Marking

8.3.1 88PG82XX Package Marking and Pin 1 Locations

Figure 51 is an example of the package marking and pin 1 location for the 88PG847 part. Markings for the other variants are similar.

Figure 51: 88PG8227 Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Locations of markings are approximate.

A Revision History

Table 19: Revision History

Document Type	Document Revision
Release	Rev. C
• Document brought into new template. • “Confidential” removed. • Functional Characteristic Graphs edited. • Replaced Mechanical Drawing	

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