Fractional-N Frequency Synthesizer

Features

- Delta-Sigma Fractional-N Frequency Synthesis
  - Generates a Low Jitter 6 - 75 MHz Clock from an 8 - 75 MHz Reference Clock
- Highly Accurate PLL Multiplication Factor
  - Maximum Error Less Than 1 PPM
- I²C® / SPI™ Control Port
- Configurable Auxiliary Output
  - Buffered Reference Clock
  - PLL Lock Indication
  - Duplicate PLL Output
- Flexible Sourcing of Reference Clock
  - External Oscillator or Clock Source
  - Supports Inexpensive Local Crystal
- Minimal Board Space Required
  - No External Analog Loop-filter Components

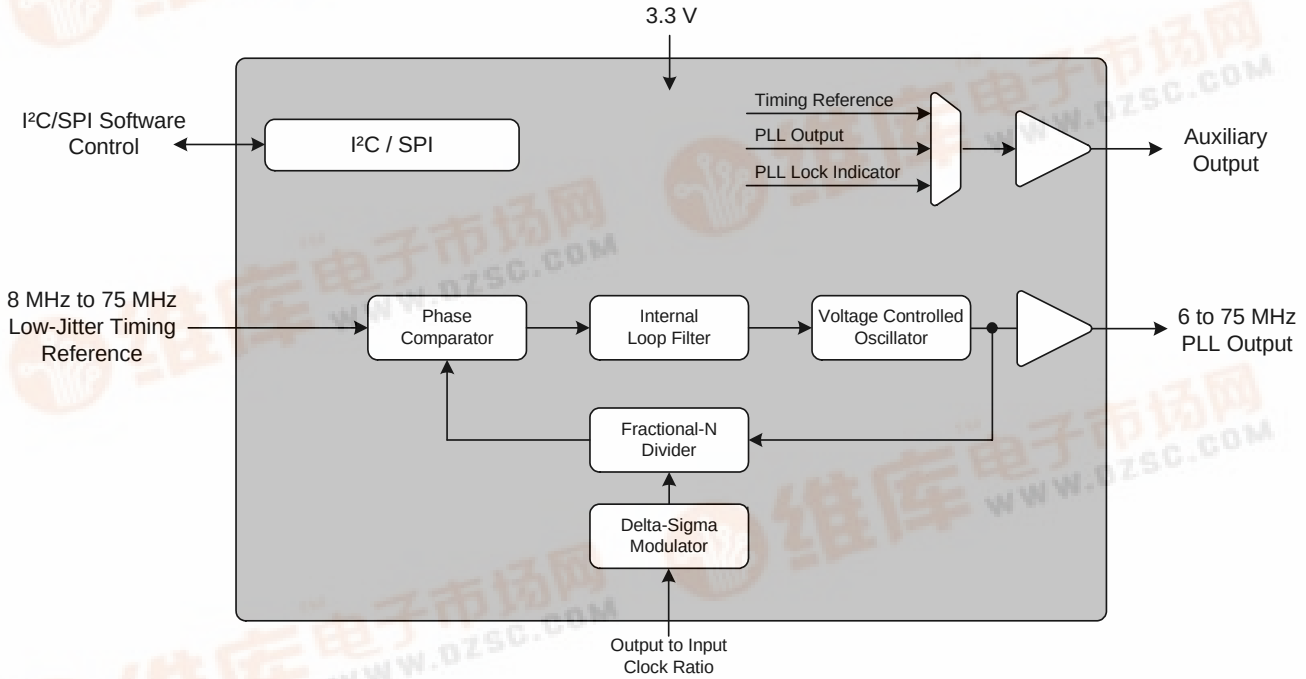
General Description

The CS2200-CP is an extremely versatile system clocking device that utilizes a programmable phase lock loop. The CS2200-CP is based on an analog PLL architecture comprised of a Delta-Sigma Fractional-N Frequency Synthesizer. This architecture allows for frequency synthesis and clock generation from a stable reference clock.

The CS2200-CP supports both I²C and SPI for full software control.

The CS2200-CP is available in a 10-pin MSOP package in Commercial (-10 °C to +70 °C) grade.

Customer development kits are also available for device evaluation. Please see "Ordering Information" on page 25 for complete details.



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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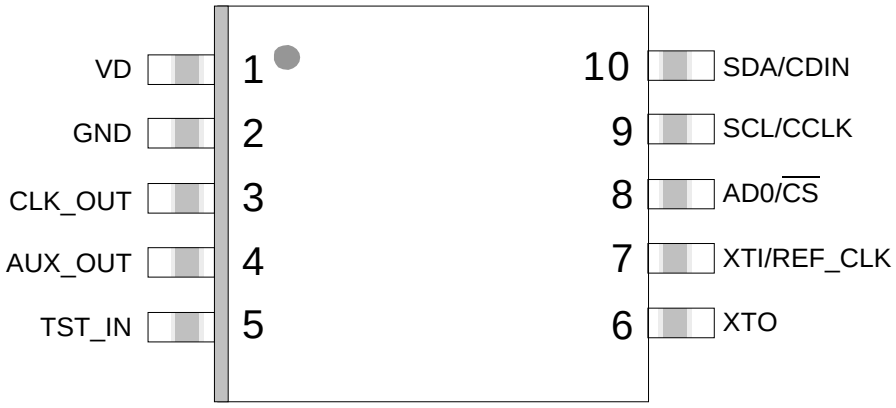
1. PIN DESCRIPTION



Pin Name	#	Pin Description
VD	1	**Digital Power** (*Input*) - Positive power supply for the digital and analog sections.
GND	2	**Ground** (*Input*) - Ground reference.
CLK_OUT	3	**PLL Clock Output** (*Output*) - PLL clock output.
AUX_OUT	4	**Auxiliary Output** (*Output*) - This pin outputs a buffered version of one of the input or output clocks, or a status signal, depending on register configuration.
TST_IN	5	**Test Input** (*Input*) - This pin is for factory test purposes and must be connected to GND for proper operation.
XTO XTI/REF_CLK	6 7	**Crystal Connections (XTI/XTO) / Timing Reference Clock Input (REF_CLK)** (*Input/Output*) - XTI/XTO are I/O pins for an external crystal which may be used to generate the low-jitter PLL input clock. REF_CLK is an input for an externally generated low-jitter reference clock.
AD0/$\overline{CS}$	8	**Address Bit 0 (I²C) / Control Port Chip Select (SPI)** (*Input*) - AD0 is a chip address pin in I²C Mode. $\overline{CS}$ is the chip select signal in SPI Mode.
SCL/CCLK	9	**Control Port Clock** *(Input)* - SCL/CCLK is the serial clock for the serial control port in I²C and SPI mode.
SDA/CDIN	10	**Serial Control Data** (*Input/Output*) - SDA is the data I/O line in I²C Mode. CDIN is the input data line for the control port interface in SPI Mode.

2. TYPICAL CONNECTION DIAGRAM

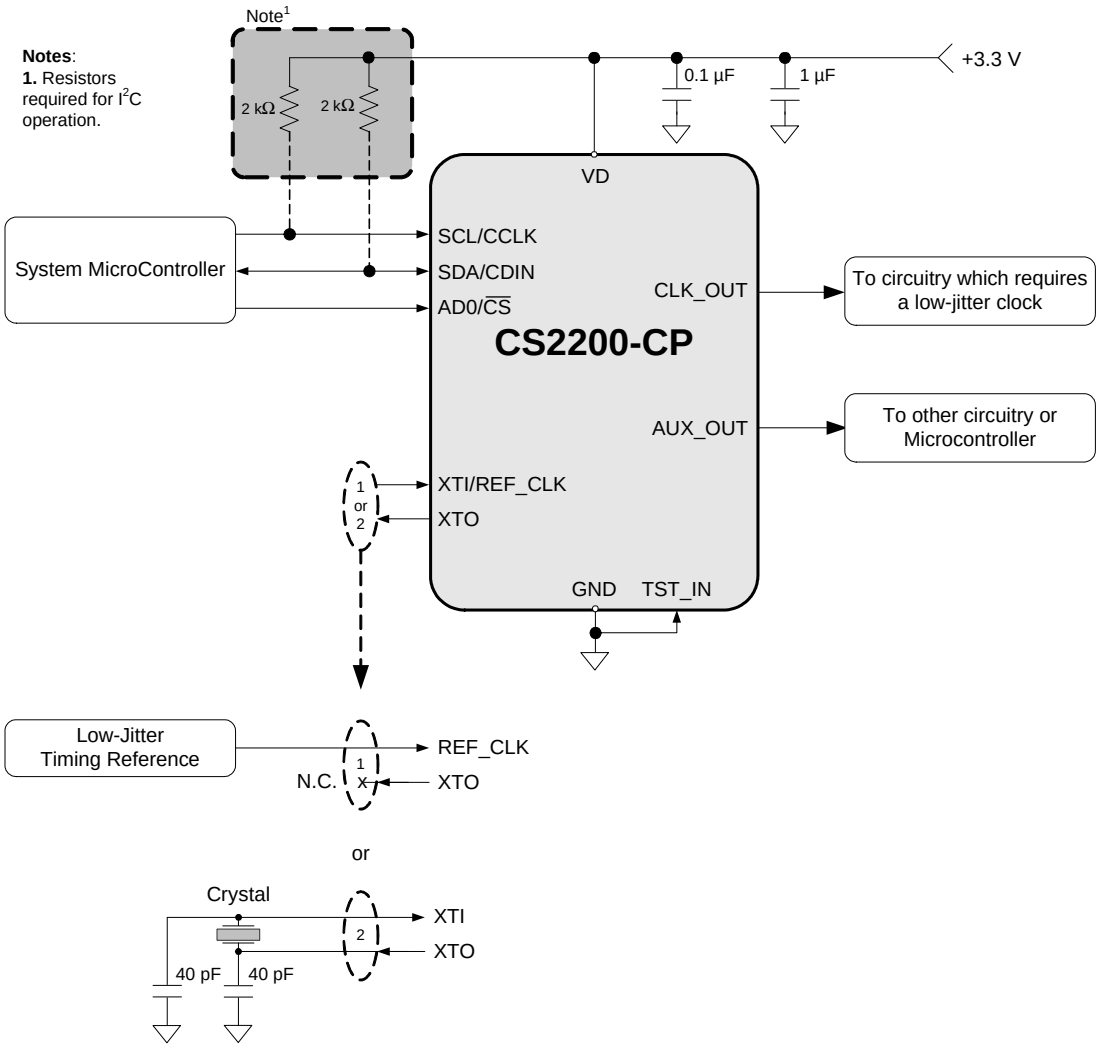


Figure 1. Typical Connection Diagram

3. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

GND = 0 V; all voltages with respect to ground. (Note 1)

Parameters	Symbol	Min	Typ	Max	Units
DC Power Supply	VD	3.1	3.3	3.5	V
Ambient Operating Temperature (Power Applied) Commercial Grade	T_{AC}	-10	-	+70	°C

Notes: 1. Device functional operation is guaranteed within these limits. Functionality is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

ABSOLUTE MAXIMUM RATINGS

GND = 0 V; all voltages with respect to ground.

Parameters	Symbol	Min	Max	Units
DC Power Supply	VD	-0.3	6.0	V
Input Current	I_{IN}	-	±10	mA
Digital Input Voltage (Note 1)	V_{IN}	-0.3	VD + 0.4	V
Ambient Operating Temperature (Power Applied)	T_A	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Notes: 1. The maximum over/under voltage is limited by the input current except on the power supply pin.

DC ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise specified): VD = 3.1 V to 3.5 V; T_A = -10°C to +70°C (Commercial Grade).

Parameters	Symbol	Min	Typ	Max	Units
Power Supply Current - Unloaded (Note 2)	I_D	-	12	18	mA
Power Dissipation - Unloaded (Note 2)	P_D	-	40	60	mW
Input Leakage Current	I_{IN}	-	-	±10	µA
Input Capacitance	I_C	-	8	-	pF
High-Level Input Voltage	V_{IH}	70%	-	-	VD
Low-Level Input Voltage	V_{IL}	-	-	30%	VD
High-Level Output Voltage (I_{OH} = -1.2 mA)	V_{OH}	80%	-	-	VD
Low-Level Output Voltage (I_{OH} = 1.2 mA)	V_{OL}	-	-	20%	VD

Notes: 2. To calculate the additional current consumption due to loading (per output pin), multiply clock output frequency by load capacitance and power supply voltage.
For example, f_{CLK_OUT} (49.152 MHz) * C_L (15 pF) * VD (3.3 V) = 2.4 mA of additional current due to these loading conditions on CLK_OUT.

AC ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise specified): VD = 3.1 V to 3.5 V; T_A = -10°C to +70°C (Commercial Grade); C_L = 15 pF.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
Crystal Frequency	f_{XTAL}	Fundamental Mode	8	-	50	MHz
Reference Clock Input Frequency	f_{REF_CLK}		8	-	75	MHz
Reference Clock Input Duty Cycle	D_{REF_CLK}		45	-	55	%
Internal System Clock Frequency	f_{SYS_CLK}		8		18.75	MHz
PLL Clock Output Frequency	f_{CLK_OUT}		6	-	75	MHz
PLL Clock Output Duty Cycle	t_{OD}	Measured at VD/2	48	50	52	%
Clock Output Rise Time	t_{OR}	20% to 80% of VD	-	1.7	3.0	ns
Clock Output Fall Time	t_{OF}	80% to 20% of VD	-	1.7	3.0	ns
Period Jitter	t_{JIT}	(Note 3)	-	70	150	ps rms
Base Band Jitter (100 Hz to 40 kHz)		(Notes 3, 4)	-	50	-	ps rms
Wide Band JItter (100 Hz Corner)		(Notes 3, 5)	-	175	-	ps rms
PLL Lock Time - REF_CLK	t_{LR}	f_{REF_CLK} = 8 to 75 MHz	-	1	2	ms
Output Frequency Synthesis Resolution (Note 6)	f_{err}		0	-	±0.5	ppm

Notes: 3. f_{CLK_OUT} = 24.576 MHz; Sample size = 10,000 points; AuxOutSrc[1:0] = 11.

4. In accordance with AES-12id-2006 section 3.4.2. Measurements are Time Interval Error taken with 3rd order 100 Hz to 40 kHz bandpass filter.

5. In accordance with AES-12id-2006 section 3.4.1. Measurements are Time Interval Error taken with 3rd order 100 Hz Highpass filter.

6. The frequency accuracy of the PLL clock output is directly proportional to the frequency accuracy of the reference clock.

CONTROL PORT SWITCHING CHARACTERISTICS- I²C FORMAT

Inputs: Logic 0 = GND; Logic 1 = VD; C_L = 20 pF.

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
Bus Free-Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low Time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 7)	t_{hdd}	0	-	µs
SDA Setup Time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_r	-	1	µs
Fall Time SCL and SDA	t_f	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns
Delay from Supply Voltage Stable to Control Port Ready	t_{dpor}	100	-	µs

Notes: 7. Data must be held for sufficient time to bridge the transition time, t_f, of SCL.

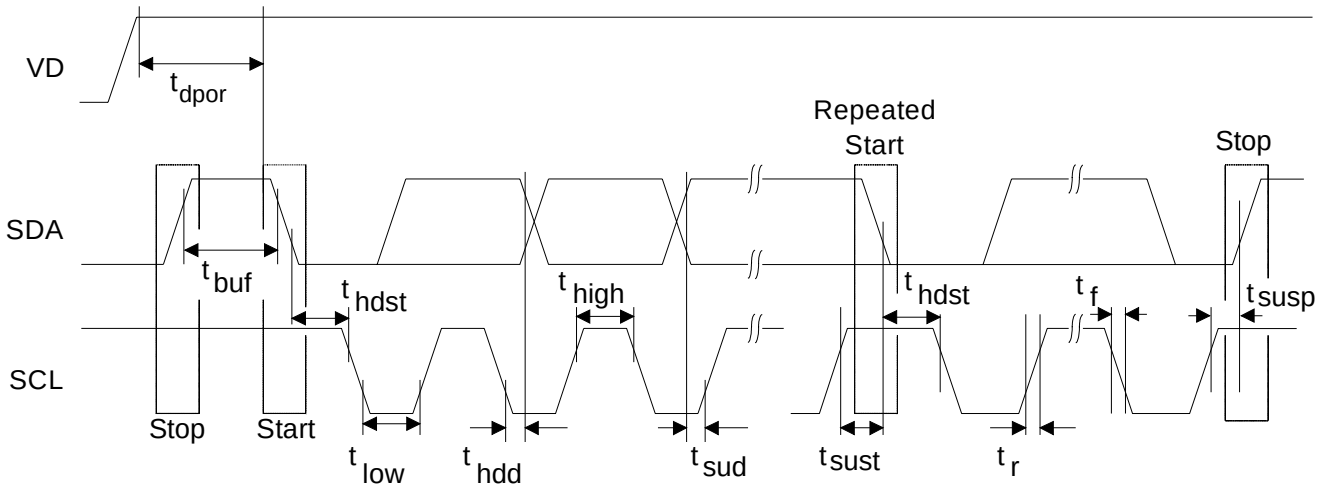


Figure 2. Control Port Timing - I²C Format

CONTROL PORT SWITCHING CHARACTERISTICS - SPI FORMAT

Inputs: Logic 0 = GND; Logic 1 = VD; C_L = 20 pF.

Parameter		Symbol	Min	Max	Unit
CCLK Clock Frequency		f_{cclk}	-	6	MHz
CCLK Edge to $\overline{CS}$ Falling	(Note 8)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 9)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 10)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 10)	t_{f2}	-	100	ns
Delay from Supply Voltage Stable to Control Port Ready		t_{dpor}	100	-	µs

Notes: 8. t_{spi} is only needed before first falling edge of $\overline{CS}$ after power is applied. t_{spi} = 0 at all other times.

9. Data must be held for sufficient time to bridge the transition time of CCLK.

10. For f_{cclk} < 1 MHz.

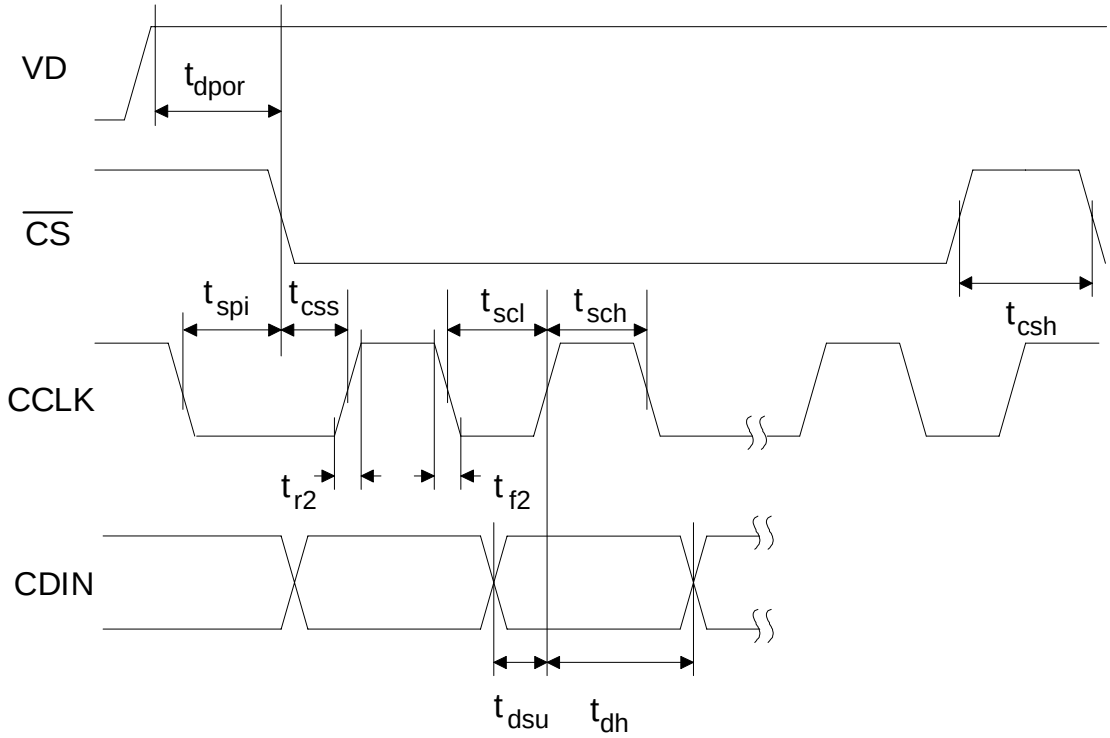


Figure 3. Control Port Timing - SPI Format (Write Only)

4. ARCHITECTURE OVERVIEW

4.1 Delta-Sigma Fractional-N Frequency Synthesizer

The core of the CS2200 is a Delta-Sigma Fractional-N Frequency Synthesizer which has very high-resolution for Input/Output clock ratios, low phase noise, very wide range of output frequencies and the ability to quickly tune to a new frequency. In very simplistic terms, the Fractional-N Frequency Synthesizer multiplies the Timing Reference Clock by the value of N to generate the PLL output clock. The desired output to input clock ratio is the value of N that is applied to the delta-sigma modulator (see Figure 4).

The analog PLL based frequency synthesizer uses a low-jitter timing reference clock as a time and phase reference for the internal voltage controlled oscillator (VCO). The phase comparator compares the fractional-N divided clock with the original timing reference and generates a control signal. The control signal is filtered by the internal loop filter to generate the VCO's control voltage which sets its output frequency. The delta-sigma modulator modulates the loop integer divide ratio to get the desired fractional ratio between the reference clock and the VCO output (thus the one's density of the modulator sets the fractional value). This allows the design to be optimized for very fast lock times for a wide range of output frequencies without the need for external filter components. As with any Fractional-N Frequency Synthesizer the timing reference clock should be stable and jitter-free.

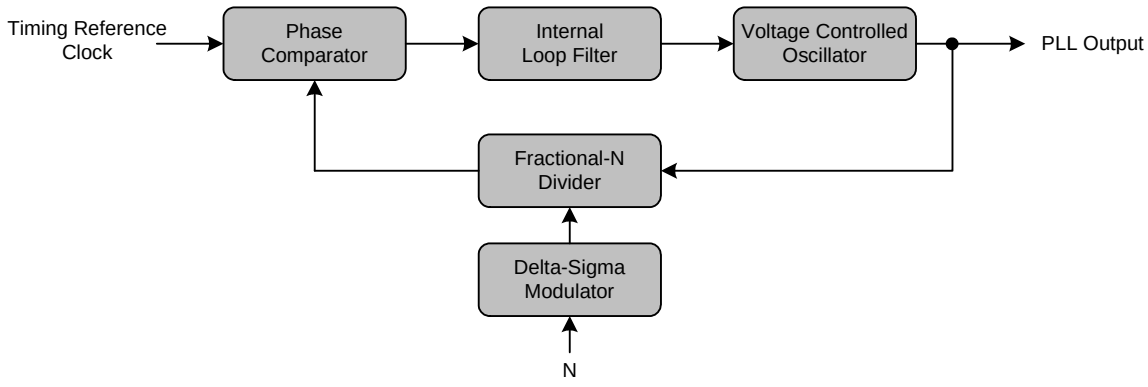


Figure 4. Delta-Sigma Fractional-N Frequency Synthesizer

5. APPLICATIONS

5.1 Timing Reference Clock Input

The low jitter timing reference clock (RefClk) can be provided by either an external reference clock or an external crystal in conjunction with the internal oscillator. In order to maintain a stable and low-jitter PLL output the timing reference clock must also be stable and low-jitter; the quality of the timing reference clock directly affects the performance of the PLL and hence the quality of the PLL output.

5.1.1 Internal Timing Reference Clock Divider

The Internal Timing Reference Clock (SysClk) has a smaller maximum frequency than what is allowed on the XTI/REF_CLK pin. The CS2200 supports the wider external frequency range by offering an internal divider for RefClk. The *RefClkDiv[1:0]* bits should be set such that SysClk, the divided RefClk, then falls within the valid range as indicated in Figure 5.

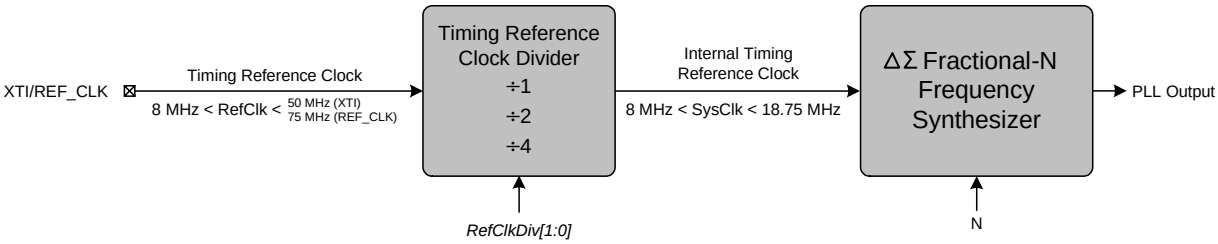


Figure 5. Internal Timing Reference Clock Divider

It should be noted that the maximum allowable input frequency of the XTI/REF_CLK pin is dependent upon its configuration as either a crystal connection or external clock input. See the "AC Electrical Characteristics" on page 7 for more details.

Referenced Control	Register Location
RefClkDiv[1:0]	"Reference Clock Input Divider (RefClkDiv[1:0])" on page 22

5.1.2 Crystal Connections (XTI and XTO)

An external crystal may be used to generate RefClk. To accomplish this, a 20 pF fundamental mode parallel resonant crystal must be connected between the XTI and XTO pins as shown in Figure 6. As shown, nothing other than the crystal and its load capacitors should be connected to XTI and XTO. Please refer to the "AC Electrical Characteristics" on page 7 for the allowed crystal frequency range.

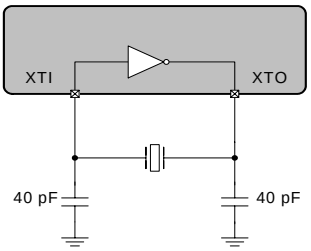


Figure 6. External Component Requirements for Crystal Circuit

5.1.3 External Reference Clock (REF_CLK)

For operation with an externally generated REF_CLK signal, XTI/REF_CLK should be connected to the reference clock source and XTO should be left unconnected or pulled low through a 47 kΩ resistor to GND.

5.2 Output to Input Frequency Ratio Configuration

5.2.1 User Defined Ratio (R_{UD})

The User Defined Ratio, R_{UD}, is a 32-bit un-signed fixed-point number, stored in the *Ratio* register set, which determines the basis for the desired input to output clock ratio. The 32-bit R_{UD} is represented in a 12.20 format where the 12 MSBs represent the integer binary portion while the remaining 20 LSBs represent the fractional binary portion. The maximum multiplication factor is approximately 4096 with a resolution of 0.954 PPM in this configuration. See "Calculating the User Defined Ratio" on page 23 for more information.

The status of internal dividers, such as the internal timing reference clock divider, are automatically taken into account. Therefore R_{UD} is simply the desired ratio of the output to input clock frequencies.

Referenced Control	Register Location
Ratio	"Ratio (Address 06h - 09h)" on page 21

5.2.2 Manual Ratio Modifier (R-Mod)

The manual Ratio Modifier is used to internally multiply/divide the R_{UD} (the *Ratio* stored in the register space remains unchanged). The available options for R_{MOD} are summarized in Table 1 on page 12.

The R-Mod value selected by *RModSel[2:0]* is always used in the calculation for the Effective Ratio (R_{EFF}), see "Effective Ratio (REFF)" on page 13. If R-Mod is not desired, *RModSel[2:0]* should be left at its default value of '000', which corresponds to an R-Mod value of 1, thereby effectively disabling the ratio modifier.

RModSel[2:0]	Ratio Modifier
000	1
001	2
010	4
011	8
100	0.5
101	0.25
110	0.125
111	0.0625

Table 1. Ratio Modifier

Referenced Control	Register Location
Ratio	"Ratio (Address 06h - 09h)" on page 21
RModSel[2:0]	"R-Mod Selection (RModSel[2:0])" section on page 20

5.2.3 Effective Ratio (R_{EFF})

The Effective Ratio (R_{EFF}) is an internal calculation comprised of R_{UD} and the appropriate modifiers, as previously described. R_{EFF} is calculated as follows:

$R_{EFF} = R_{UD} \bullet R_{MOD}$

To simplify operation the device handles some of the ratio calculation functions automatically (such as when the internal timing reference clock divider is set). For this reason, the Effective Ratio does not need to be altered to account for internal dividers.

Ratio modifiers which would produce an overflow or truncation of R_{EFF} should not be used; For example if R_{UD} is 1024 an R_{MOD} of 8 would produce an R_{EFF} value of 8192 which exceeds the 4096 limit of the 12.20 format. In all cases, the maximum and minimum allowable values for R_{EFF} are dictated by the frequency limits for both the input and output clocks as shown in the "AC Electrical Characteristics" on page 7.

5.2.4 Ratio Configuration Summary

The R_{UD} is the user defined ratio stored in the register space. R-Mod is applied if selected. The user defined ratio and ratio modifier make up the effective ratio R_{EFF}, the final calculation used to determine the output to input clock ratio. The effective ratio is then corrected for the internal dividers. The conceptual diagram in Figure 7 summarizes the features involved in the calculation of the ratio values used to generate the fractional-N value which controls the Frequency Synthesizer.

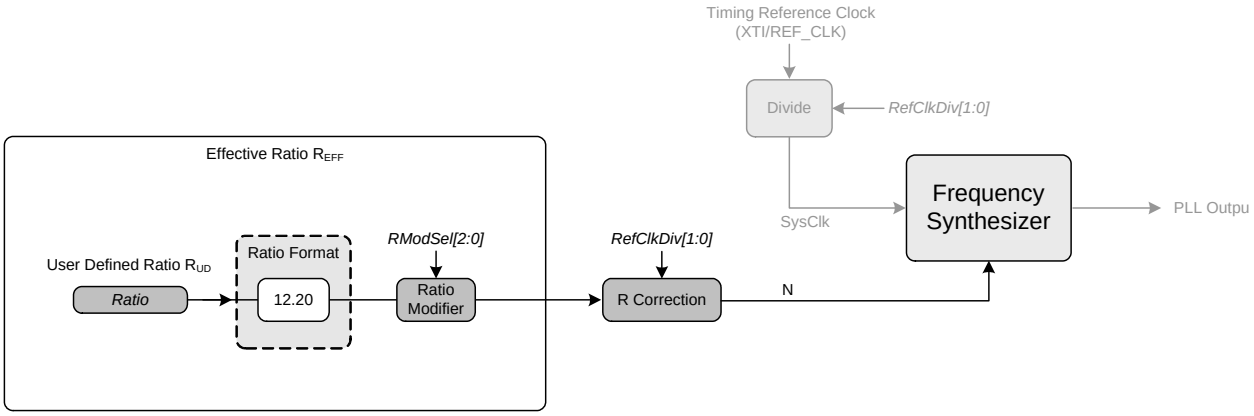


Figure 7. Ratio Feature Summary

Referenced Control	Register Location
Ratio	"Ratio (Address 06h - 09h)" on page 21
RModSel[2:0]	"R-Mod Selection (RModSel[2:0])" section on page 20
RefClkDiv[1:0]	"Reference Clock Input Divider (RefClkDiv[1:0])" on page 22

5.3 PLL Clock Output

The PLL clock output pin (CLK_OUT) provides a buffered version of the output of the frequency synthesizer. The driver can be set to high-impedance with the *ClkOutDis* bit.

The output from the PLL automatically drives a static low condition while the PLL is un-locked (when the clock may be unreliable). This feature can be disabled by setting the *ClkOutUnl* bit, however the state CLK_OUT may then be unreliable during an unlock condition.

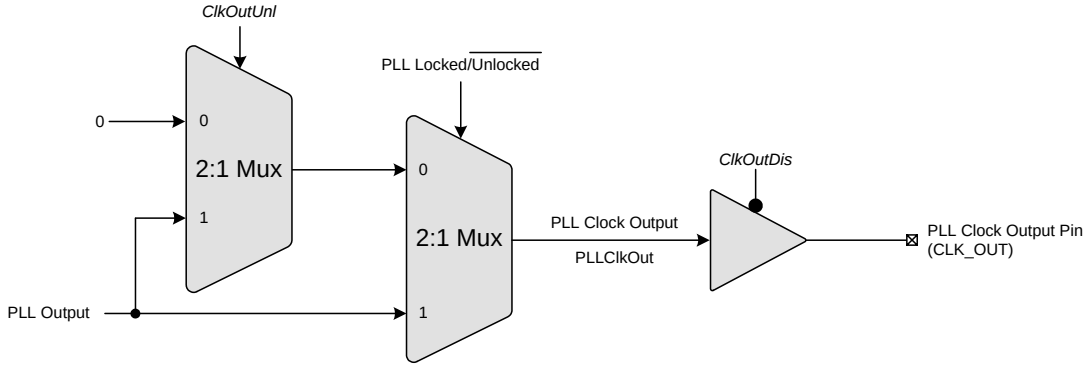


Figure 8. PLL Clock Output Options

Referenced Control	Register Location
ClkOutUnl	"Enable PLL Clock Output on Unlock (ClkOutUnl)" on page 22
ClkOutDis	"PLL Clock Output Disable (ClkOutDis)" on page 20

5.4 Auxiliary Output

The auxiliary output pin (AUX_OUT) can be mapped, as shown in Figure 9, to one of three signals: reference clock (RefClk), additional PLL clock output (CLK_OUT), or a PLL lock indicator (Lock). The mux is controlled via the *AuxOutSrc[1:0]* bits. If AUX_OUT is set to Lock, the *AuxLockCfg* bit is then used to control the output driver type and polarity of the LOCK signal (see section 8.6.1 on page 22). If AUX_OUT is set to CLK_OUT the phase of the PLL Clock Output signal on AUX_OUT may differ from the CLK_OUT pin. The driver for the pin can be set to high-impedance using the *AuxOutDis* bit.

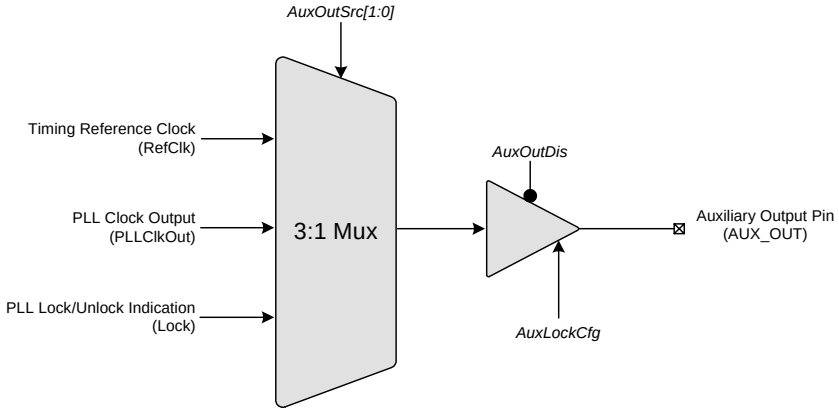


Figure 9. Auxiliary Output Selection

Referenced Control	Register Location
AuxOutSrc[1:0]	"Auxiliary Output Source Selection (AuxOutSrc[1:0])" on page 20
AuxOutDis	"Auxiliary Output Disable (AuxOutDis)" on page 19
AuxLockCfg	"AUX PLL Lock Output Configuration (AuxLockCfg)" section on page 22

5.5 Clock Output Stability Considerations

5.5.1 Output Switching

CS2200 is designed such that re-configuration of the clock routing functions do not result in a partial clock period on any of the active outputs (CLK_OUT and/or AUX_OUT). In particular, enabling or disabling an output, changing the auxiliary output source between REF_CLK and CLK_OUT, and the automatic disabling of the output(s) during unlock will not cause a runt or partial clock period.

The following exceptions/limitations exist:

- Enabling/disabling AUX_OUT when AuxOutSrc = 11 (unlock indicator).
- Switching AuxOutSrc[1:0] to or from 11 (unlock indicator)
  (Transitions between AuxOutSrc[1:0] = [00,10] will not produce a glitch).
- Changing the *ClkOutUnl* bit while the PLL is in operation.

When any of these exceptions occur, a partial clock period on the output may result.

5.5.2 PLL Unlock Conditions

Certain changes to the clock inputs and registers can cause the PLL to lose lock which will affect the presence the clock signal on CLK_OUT. The following outlines which conditions cause the PLL to go unlocked:

- Changes made to the registers which affect the Fraction-N value that is used by the Frequency Synthesizer. This includes all the bits shown in Figure 7 on page 13.
- Any discontinuities on the Timing Reference Clock, REF_CLK.

6. SPI / I²C CONTROL PORT

The control port is used to access the registers and allows the device to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to device inputs and outputs. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port operates with either the SPI or I²C interface, with the CS2200 acting as a slave device. SPI Mode is selected if there is a high-to-low transition on the AD0/$\overline{CS}$ pin after power-up. I²C Mode is selected by connecting the AD0/$\overline{CS}$ pin through a resistor to VD or GND, thereby permanently selecting the desired AD0 bit address state. In both modes the *EnDevCfg1* and *EnDevCfg2* bits must be set to 1 for normal operation.

WARNING: All "Reserved" registers must maintain their default state to ensure proper functional operation.

Referenced Control	Register Location
EnDevCfg1	"Enable Device Configuration Registers 1 (EnDevCfg1)" on page 20
EnDevCfg2	"Enable Device Configuration Registers 2 (EnDevCfg2)" section on page 21

6.1 SPI Control

In SPI Mode, $\overline{CS}$ is the chip select signal; CCLK is the control port bit clock (sourced from a microcontroller), and CDIN is the input data line from the microcontroller. Data is clocked in on the rising edge of CCLK. The device only supports write operations.

Figure 10 shows the operation of the control port in SPI Mode. To write to a register, bring $\overline{CS}$ low. The first eight bits on CDIN form the chip address and must be 10011110. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data which will be placed into the register designated by the MAP.

There is MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, the MAP will stay constant for successive read or writes. If INCR is set to a 1, the MAP will automatically increment after each byte is read or written, allowing block writes of successive registers.

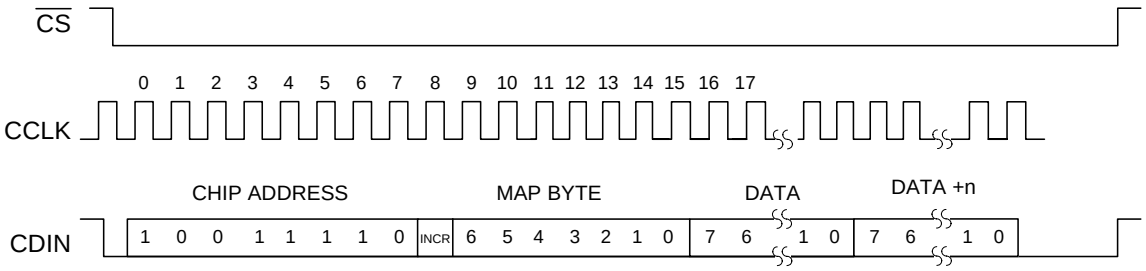


Figure 10. Control Port Timing in SPI Mode

6.2 I²C Control

In I²C Mode, SDA is a bidirectional data line. Data is clocked into and out of the device by the clock, SCL. There is no $\overline{CS}$ pin. The AD0 pin forms the least-significant bit of the chip address and should be connected to VD or GND as appropriate. The state of the AD0 pin should be maintained throughout operation of the device.

The signal timings for a read and write cycle are shown in Figure 11 and Figure 12. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS2200 after a Start condition consists of the 7-bit chip address field and a R/$\overline{W}$ bit (high for a read, low for a write). The upper 6 bits of the 7-bit address field are fixed at 100111 followed by the logic state of the AD0 pin. The

eighth bit of the address is the R/$\overline{W}$ bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS2200 after each input byte is read and is input from the microcontroller after each transmitted byte.

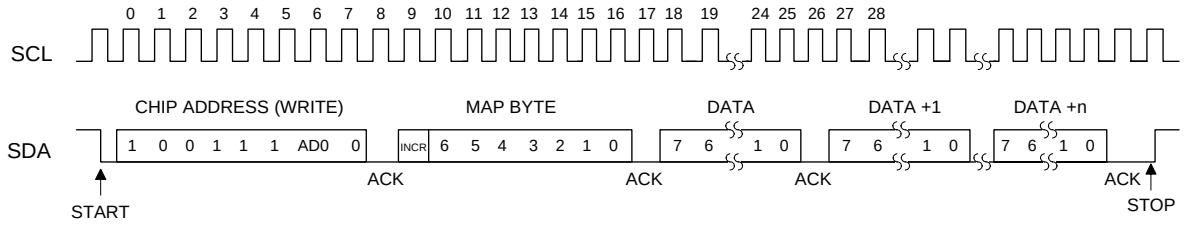


Figure 11. Control Port Timing, I²C Write

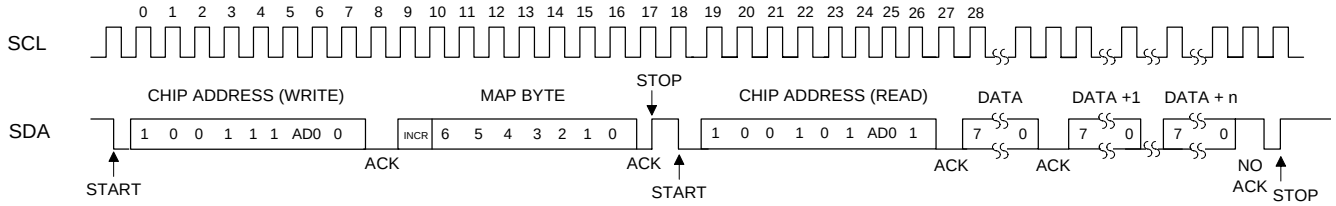


Figure 12. Control Port Timing, I²C Aborted Write + Read

Since the read operation cannot set the MAP, an aborted write operation is used as a preamble. As shown in Figure 11, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Send start condition.

Send 100111x0 (chip address & write operation).

Receive acknowledge bit.

Send MAP byte, auto increment off.

Receive acknowledge bit.

Send stop condition, aborting write.

Send start condition.

Send 100111x1(chip address & read operation).

Receive acknowledge bit.

Receive byte, contents of selected register.

Send acknowledge bit.

Send stop condition.

Setting the auto increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

6.3 Memory Address Pointer

The Memory Address Pointer (MAP) byte comes after the address byte and selects the register to be read or written. Refer to the pseudocode above for implementation details.

6.3.1 Map Auto Increment

The device has MAP auto increment capability enabled by the INCR bit (the MSB) of the MAP. If INCR is set to 0, MAP will stay constant for successive I²C writes or reads and SPI writes. If INCR is set to 1, MAP will auto increment after each byte is read or written, allowing block reads or writes of successive registers.

7. REGISTER QUICK REFERENCE

This table shows the register and bit names with their associated default values.
EnDevCfg1 and *EnDevCfg2* bits must be set to 1 for normal operation.

WARNING: All “Reserved” registers must maintain their default state to ensure proper functional operation.

Adr	Name	7	6	5	4	3	2	1	0
01h p 19	Device ID	Device4 0	Device3 0	Device2 0	Device1 0	Device0 0	Revision2 x	Revision1 x	Revision0 x
02h p 19	Device Ctrl	Unlock x	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	AuxOutDis 0	ClkOutDis 0
03h p 20	Device Cfg 1	RModSel2 0	RModSel1 0	RModSel0 0	Reserved 0	Reserved 0	AuxOutSrc1 0	AuxOutSrc0 0	EnDevCfg1 0
05h p 21	Global Cfg	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Freeze 0	Reserved 0	Reserved 0	EnDevCfg2 0
06h - 09h	32-Bit Ratio	MSB MSB-8 LSB+15 LSB+7	....						MSB-7 MSB-15 LSB+8 LSB
16h p 22	Funct Cfg 1	Reserved 0	AuxLockCfg 0	Reserved 0	RefClkDiv1 0	RefClkDiv0 0	Reserved 0	Reserved 0	Reserved 0
17h p 22	Funct Cfg 2	Reserved 0	Reserved 0	Reserved 0	ClkOutUnl 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0

8. REGISTER DESCRIPTIONS

In I²C Mode all registers are read/write unless otherwise stated. In SPI mode all registers are write only. All “Reserved” registers must maintain their default state to ensure proper functional operation. The default state of each bit after a power-up sequence or reset is indicated by the shaded row in the bit decode table and in the “Register Quick Reference” on page 18.

Control port mode is entered when the device recognizes a valid chip address input on its I²C/SPI serial control pins and the *EnDevCfg1* and *EnDevCfg2* bits are set to 1.

8.1 Device I.D. and Revision (Address 01h)

7	6	5	4	3	2	1	0
Device4	Device3	Device2	Device1	Device0	Revision2	Revision1	Revision0

8.1.1 Device Identification (Device[4:0]) - Read Only

I.D. code for the CS2200.

Device[4:0]	Device
00000	CS2200.

8.1.2 Device Revision (Revision[2:0]) - Read Only

CS2200 revision level.

REVID[2:0]	Revision Level
100	B2.

8.2 Device Control (Address 02h)

7	6	5	4	3	2	1	0
Unlock	Reserved	Reserved	Reserved	Reserved	Reserved	AuxOutDis	ClkOutDis

8.2.1 Unlock Indicator (Unlock) - Read Only

Indicates the lock state of the PLL.

Unlock	PLL Lock State
0	PLL is Locked.
1	PLL is Unlocked.

8.2.2 Auxiliary Output Disable (AuxOutDis)

This bit controls the output driver for the AUX_OUT pin.

AuxOutDis	Output Driver State
0	AUX_OUT output driver enabled.
1	AUX_OUT output driver set to high-impedance.
Application:	“Auxiliary Output” on page 14

8.2.3 PLL Clock Output Disable (ClkOutDis)

This bit controls the output driver for the CLK_OUT pin.

ClkOutDis	Output Driver State
0	CLK_OUT output driver enabled.
1	CLK_OUT output driver set to high-impedance.
Application:	"PLL Clock Output" on page 14

8.3 Device Configuration 1 (Address 03h)

7	6	5	4	3	2	1	0
RModSel2	RModSel1	RModSel0	Reserved	Reserved	AuxOutSrc1	AuxOutSrc0	EnDevCfg1

8.3.1 R-Mod Selection (RModSel[2:0])

Selects the R-Mod value, which is used as a factor in determining the PLL's Fractional N.

RModSel[2:0]	R-Mod Selection
000	Left-shift R-value by 0 (x 1).
001	Left-shift R-value by 1 (x 2).
010	Left-shift R-value by 2 (x 4).
011	Left-shift R-value by 3 (x 8).
100	Right-shift R-value by 1 (÷ 2).
101	Right-shift R-value by 2 (÷ 4).
110	Right-shift R-value by 3 (÷ 8).
111	Right-shift R-value by 4 (÷ 16).
Application:	"Manual Ratio Modifier (R-Mod)" on page 12

8.3.2 Auxiliary Output Source Selection (AuxOutSrc[1:0])

Selects the source of the AUX_OUT signal.

AuxOutSrc[1:0]	Auxiliary Output Source
00	RefClk.
01	Reserved.
10	CLK_OUT.
11	PLL Lock Status Indicator.
Application:	"Auxiliary Output" on page 14

Note: When set to 11, *AuxLckCfg* sets the polarity and driver type ("AUX PLL Lock Output Configuration (AuxLockCfg)" on page 22).

8.3.3 Enable Device Configuration Registers 1 (EnDevCfg1)

This bit, in conjunction with *EnDevCfg2*, enables control port mode. Both bits must be set to 1 during initialization.

EnDevCfg1	Register State
0	Disabled.
1	Enabled.
Application:	"SPI / I²C Control Port" on page 16

Note: *EnDevCfg2* must also be set to enable control port mode ("SPI / I²C Control Port" on page 16).

8.4 Global Configuration (Address 05h)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Freeze	Reserved	Reserved	EnDevCfg2

8.4.1 Device Configuration Freeze (Freeze)

Setting this bit allows writes to the Device Control and Device Configuration registers (address 02h - 04h) but keeps them from taking effect until this bit is cleared.

FREEZE	Device Control and Configuration Registers
0	Register changes take effect immediately.
1	Modifications may be made to Device Control and Device Configuration registers (registers 02h-04h) without the changes taking effect until after the FREEZE bit is cleared.

8.4.2 Enable Device Configuration Registers 2 (EnDevCfg2)

This bit, in conjunction with *EnDevCfg1*, enables control port mode. Both bits must be set to 1 during initialization.

EnDevCfg2	Register State
0	Disabled.
1	Enabled.
Application:	"SPI / I²C Control Port" on page 16

Note: *EnDevCfg1* must also be set to enable control port mode ("SPI / I²C Control Port" on page 16).

8.5 Ratio (Address 06h - 09h)

7	6	5	4	3	2	1	0
MSB	.....	.....	.....	.....	.....	.....	MSB-7
MSB-8	.....	.....	.....	.....	.....	.....	MSB-15
LSB+15	.....	.....	.....	.....	.....	.....	LSB+8
LSB+7	.....	.....	.....	.....	.....	.....	LSB

These registers contain the User Defined Ratio as shown in the "Register Quick Reference" section on page 18. These 4 registers form a single 32-bit ratio value as shown above. See "Output to Input Frequency Ratio Configuration" on page 12 and "Calculating the User Defined Ratio" on page 23 for more details.

8.6 Function Configuration 1 (Address 16h)

7	6	5	4	3	2	1	0
Reserved	AuxLockCfg	Reserved	RefClkDiv1	RefClkDiv0	Reserved	Reserved	Reserved

8.6.1 AUX PLL Lock Output Configuration (AuxLockCfg)

When the AUX_OUT pin is configured as a lock indicator (*AuxOutSrc[1:0]* = 11), this bit configures the AUX_OUT driver to either push-pull or open drain. It also determines the polarity of the lock signal. If AUX_OUT is configured as a clock output, the state of this bit is disregarded.

AuxLockCfg	AUX_OUT Driver Configuration
0	Push-Pull, Active High (output 'high' for unlocked condition, 'low' for locked condition).
1	Open Drain, Active Low (output 'low' for unlocked condition, high-Z for locked condition).
Application:	"Auxiliary Output" on page 14

Note: AUX_OUT is an **un**lock indicator, signalling an error condition when the PLL is unlocked. Therefore, the pin polarity is defined relative to the **un**lock condition.

8.6.2 Reference Clock Input Divider (RefClkDiv[1:0])

Selects the input divider for the timing reference clock.

RefClkDiv[1:0]	Reference Clock Input Divider	REF_CLK Frequency Range
00	÷ 4.	32 MHz to 75 MHz (50 MHz with XTI)
01	÷ 2.	16 MHz to 37.5 MHz
10	÷ 1.	8 MHz to 18.75 MHz
11	Reserved.	
Application:	"Internal Timing Reference Clock Divider" on page 11	

8.7 Function Configuration 2 (Address 17h)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	ClkOutUnl	Reserved	Reserved	Reserved	Reserved

8.7.1 Enable PLL Clock Output on Unlock (ClkOutUnl)

Defines the state of the PLL output during the PLL unlock condition.

ClkOutUnl	Clock Output Enable Status
0	Clock outputs are driven 'low' when PLL is unlocked.
1	Clock outputs are always enabled (results in unpredictable output when PLL is unlocked).
Application:	"PLL Clock Output" on page 14

9. CALCULATING THE USER DEFINED RATIO

Note: The software for use with the evaluation kit has built in tools to aid in calculating and converting the User Defined Ratio. This section is for those who are not interested in the software or who are developing their systems without the aid of the evaluation kit.

Most calculators do not interpret the fixed point binary representation which the CS2200 uses to define the output to input clock ratio (see Section 5.2.1 on page 12); However, with a simple conversion we can use these tools to generate a binary or hex value which can be written to the *Ratio* register.

9.1 12.20 Format

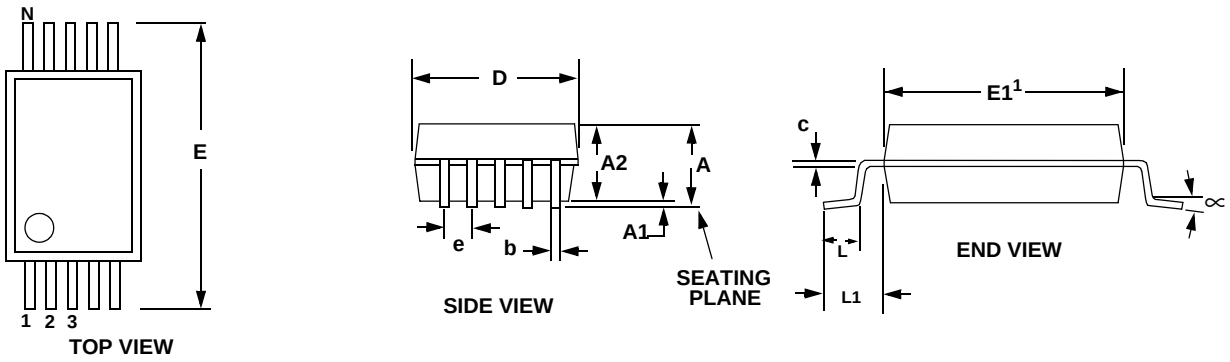
To calculate the User Defined Ratio (R_{UD}) to store in the register(s), divide the desired output clock frequency by the given input clock (RefClk). Then multiply the desired ratio by the scaling factor of 2^{20} to get the scaled decimal representation; then use the decimal to binary/hex conversion function on a calculator and write to the register. A few examples have been provided in Table 2.

Desired Output to Input Clock Ratio (output clock/input clock)	Scaled Decimal Representation = (output clock/input clock) • 2^{20}	Hex Representation of Binary R_{UD}
12.288 MHz/10 MHz=1.2288	1288490	00 13 A9 2A
11.2896 MHz/44.1 kHz=256	268435456	10 00 00 00

Table 2. Example 12.20 R-Values

10.PACKAGE DIMENSIONS

10L MSOP (3 mm BODY) PACKAGE DRAWING (Note 1)



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.0433	--	--	1.10	
A1	0	--	0.0059	0	--	0.15	
A2	0.0295	--	0.0374	0.75	--	0.95	
b	0.0059	--	0.0118	0.15	--	0.30	4, 5
c	0.0031	--	0.0091	0.08	--	0.23	
D	--	0.1181 BSC	--	--	3.00 BSC	--	2
E	--	0.1929 BSC	--	--	4.90 BSC	--	
E1	--	0.1181 BSC	--	--	3.00 BSC	--	3
e	--	0.0197 BSC	--	--	0.50 BSC	--	
L	0.0157	0.0236	0.0315	0.40	0.60	0.80	
L1	--	0.0374 REF	--	--	0.95 REF	--	

Notes: 1. Reference document: JEDEC MO-187

2. D does not include mold flash or protrusions which is 0.15 mm max. per side.
3. E1 does not include inter-lead flash or protrusions which is 0.15 mm max per side.
4. Dimension b does not include a total allowable dambar protrusion of 0.08 mm max.
5. Exceptions to JEDEC dimension.

THERMAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
Junction to Ambient Thermal Impedance	JEDEC 2-Layer	θ_{JA}	-	170	-	°C/W
	JEDEC 4-Layer	θ_{JA}	-	100	-	°C/W

11.ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order#
CS2200-CP	Clocking Device	10L-MSOP	Yes	Commercial	-10° to +70°C	Rail	CS2200-CP-CZZ
CS2200-CP	Clocking Device	10L-MSOP	Yes		-10° to +70°C	Tape and Reel	CS2200-CP-CZZR
CDK2000	Evaluation Platform	-	Yes	-	-	-	CDK-2000-CLK

12.REFERENCES

1. Audio Engineering Society AES-12id-2006: *"AES Information Document for digital audio measurements - Jitter performance specifications,"* May 2007.
2. Philips Semiconductor, "*The I²C-Bus Specification: Version 2*," Dec. 1998. http://www.semiconductors.philips.com

13.REVISION HISTORY

Release	Changes
A1	Initial Release
A2	Updated AC Electrical Characteristics
PP1	Updated "AC Electrical Characteristics" on page 7

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com