LOW-VOLTAGE MOTOR DRIVER WITH SERIAL INTERFACE

Check for Samples: DRV8830

FEATURES

- **H-Bridge Voltage-Controlled Motor Driver**
  - **Drives DC Motor, One Winding of a Stepper Motor, or Other Actuators / Loads**
  - **Efficient PWM Voltage Control for Constant Speed With Varying Supply Voltages**
  - **Low MOSFET On-Resistance: 500 mΩ**
- **1-A Maximum Continuous Drive Current**
- **2.75-V to 6-V Operating Supply Voltage Range**
- **Reference Voltage Output**
- **Serial I^2C-Compatible Interface**
  - **Multiple Address Selections Allow Up to 9 Devices on One I^2C Bus**
- **Current Limit Circuit and Fault Output**
- **Thermally Enhanced Surface Mount Packages**

APPLICATIONS

- **Battery-Powered:**
  - **Printers**
  - **Toys**
  - **Robotics**
  - **Cameras**
  - **Phones**
- **Small Actuators, Pumps, etc.**

DESCRIPTION

The DRV8830 provides an integrated motor driver solution for battery-powered toys, printers, and other low-voltage or battery-powered motion control applications. The device has one H-bridge driver, and can drive one DC motor or one winding of a stepper motor, as well as other loads like solenoids. The output driver block consists of N-channel and P-channel power MOSFET's configured as an H-bridge to drive the motor winding.

Provided with sufficient PCB heatsinking, the DRV8830 can supply up to 1-A of continuous output current. It operates on power supply voltages from 2.75 V to 6 V.

To maintain constant motor speed over varying battery voltages while maintaining long battery life, a PWM voltage regulation method is provided. The output voltage is programmed via an I^2C-comnpatible interface, using an internal voltage reference and DAC.

Internal protection functions are provided for over current protection, short circuit protection, under voltage lockout and overtemperature protection.

The DRV8830 is available in 10-pin MSOP and WSON packages with PowerPAD™ (Eco-friendly: RoHS & no Sb/Br).

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PowerPAD™ (WSON) - DRC	Reel of 3000	DRV8830DRCR	8830
		Tube of 120	DRV8830DRC	8830
	PowerPAD™ (MSOP) - DGQ	Reel of 2000	DRV8830DGQR	8830
		Tube of 80	DRV8830DGQ	8830

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

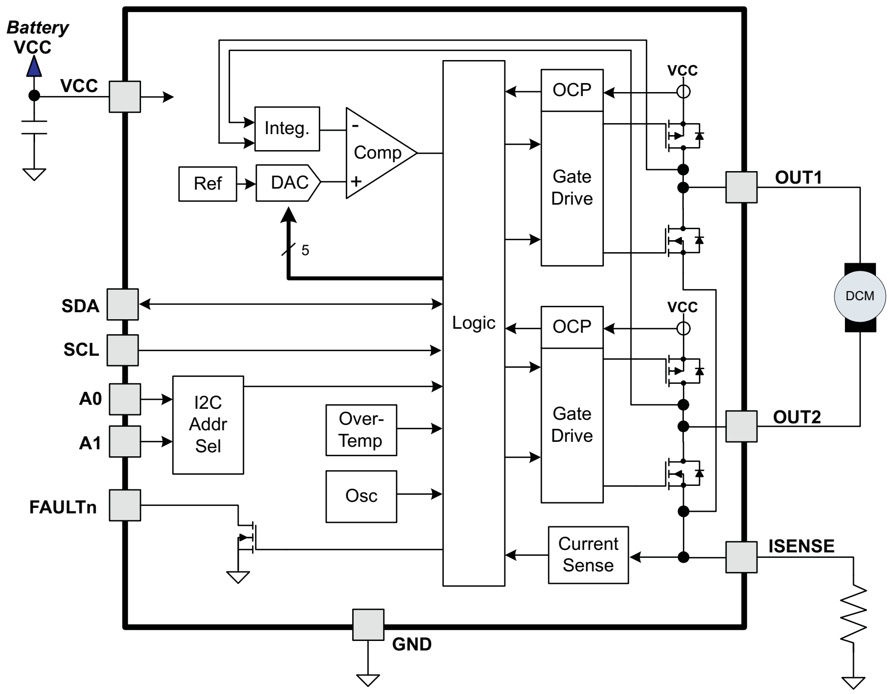
PRODUCT PREVIEW

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DEVICE INFORMATION

Functional Block Diagram



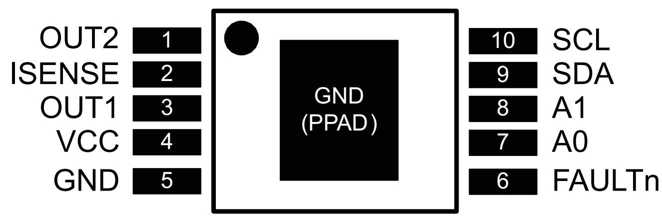
PRODUCT PREVIEW

Table 1. TERMINAL FUNCTIONS

NAME	PIN	I/O [1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
GND	5	-	Device ground	
VCC	4	-	Device and motor supply	Bypass to GND with a 0.1-µF (minimum) ceramic capacitor.
SDA	9	IO	Serial data	Data line of I^2C serial bus
SCL	10	I	Serial clock	Clock line of I^2C serial bus
A0	7	I	Address set 0	Connect to GND, VCC, or open to set I^2C base address. See serial interface description.
A1	8	I	Address set 1	
FAULTn	6	OD	Fault output	Open-drain output driven low if fault condition present
OUT1	3	O	Bridge output 1	Connect to motor winding
OUT2	1	O	Bridge output 2	
ISENSE	2	IO	Current sense resistor	Connect current sense resistor to GND. Resistor value sets current limit level.

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

DRC OR DGQ PACKAGE
(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) [1] [2]

		VALUE	UNIT
VCC	Power supply voltage range	–0.3 to 7	V
	Input pin voltage range	–0.5 to 7	V
	Peak motor drive output current [3]	Internally limited	A
	Continuous motor drive output current [3]	1	A
	Continuous total power dissipation	See Dissipation Ratings table	
T_J	Operating virtual junction temperature range	–40 to 150	°C
T_A	Operating ambient temperature range	–40 to 85	°C
T_{stg}	Storage temperature range	–60 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	T_A < 25°C	T_A = 70°C	T_A = 85°C
High-K [1]	DRC	50.2°C/W	20 mW/°C	2.49 W	1.59 W	1.29 W
High-K [1]	DGQ	69.3°C/W	14.3 mW/°C	1.80 W	1.15 W	0.94 W

(1) This data is based on using a JEDEC High-K board and the exposed die pad is connected to a copper pad on the board. The pad is connected to the ground plane by a 2 x 3 via matrix.

PRODUCT PREVIEW

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Motor power supply voltage range	2.75		6	V
I_{OUT}	Continuous H-bridge output current(1)	0		1	A

(1) Power dissipation and thermal limits must be observed.

ELECTRICAL CHARACTERISTICS

V_{CC} = 2.9 V to 6 V, T_A = -40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VCC}	VCC operating supply current	V_{CC} = 5 V		1.4	2	mA
I_{VCCQ}	VCC sleep mode supply current	V_{CC} = 5 V		0.3	1	µA
V_{UVLO}	VCC undervoltage lockout voltage	V_{CC} rising	2.4	2.575	2.75	V
		V_{CC} falling		2.47		
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage		0.25 x VCC	0.38 x VCC		V
V_{IH}	Input high voltage			0.46 x VCC	0.5 x VCC	V
V_{HYS}	Input hysteresis			0.1		V
I_{IL}	Input low current	V_{IN} = 0	-10		10	µA
I_{IH}	Input high current	V_{IN} = 3.3 V			50	µA
H-BRIDGE FETS						
$R_{DS(ON)}$	HS FET on resistance	V_{CC} = 5 V, I_O = 0.8 A, T_J = 25°C		290	TBD	mΩ
		V_{CC} = 5 V, I_O = 0.8 A, T_J = 85°C		250		
$R_{DS(ON)}$	LS FET on resistance	V_{CC} = 5 V, I_O = 0.8 A, T_J = 25°C		230	TBD	mΩ
		V_{CC} = 5 V, I_O = 0.8 A, T_J = 85°C		200		
I_{OFF}	Off-state leakage current		–20		20	µA
MOTOR DRIVER						
t_R	Rise time	V_{CC} = 3 V, load = 4 Ω	50		300	ns
t_F	Fall time	V_{CC} = 3 V, load = 4 Ω	50		300	ns
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level	V_{CC} = 5 V	1.1		3	A
t_{OCP}	OCP deglitch time			1.3		µs
T_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C
VOLTAGE CONTROL						
V_{REF}	Reference output voltage		1.235	1.285	1.335	V
ΔV_{LINE}	Line regulation	V_{CC} = 3.3 V to 6 V, V_{OUT} = 3 V, I_{OUT} = 500 mA		±1		%
ΔV_{LOAD}	Load regulation	V_{CC} = 5 V, V_{OUT} = 3 V, I_{OUT} = 200 mA to 800 mA		±1		%
CURRENT LIMIT						
V_{ILIM}	Current limit sense voltage		160	200	240	mV
t_{ILIM}	Current limit fault deglitch time			250		ms
R_{ILIM}	Current limit set resistance		0		1	Ω

I²C TIMING REQUIREMENTS

V_{CC} = 2.9 V to 6 V, T_A = -40°C to 85°C (unless otherwise noted)

		STANDARD MODE			FAST MODE			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
f_{scl}	I²C clock frequency	0		100	0		400	kHz
t_{sch}	I²C clock high time	4			0.6			µs
t_{scl}	I²C clock low time	4.7			1.3			µs
t_{sp}	I²C spike time	0		50	0		50	ns
t_{sds}	I²C serial data setup time	250			100			ns
t_{sdh}	I²C serial data hold time	0			0			ns
t_{icr}	I²C input rise time			1000	20+0.1Cb(1)		300	ns
t_{icf}	I²C input fall time			300	20+0.1Cb(1)		300	ns
t_{ocf}	I²C output fall time			300	20+0.1Cb(1)		300	ns
t_{buf}	I²C bus free time	4.7			1.3			µs
t_{sts}	I²C Start setup time	4.7			0.6			µs
t_{sth}	I²C Start hold time	4			0.6			µs
t_{sps}	I²C Stop setup time	4			0.6			µs
t_{vd} (data)	Valid data time (SCL low to SDA valid)			1			1	µs
t_{vd} (ack)	Valid data time of ACK (ACK signal from SCL low to SDA low)			1			1	µs

(1) C_b = total capacitance of one bus line in pF

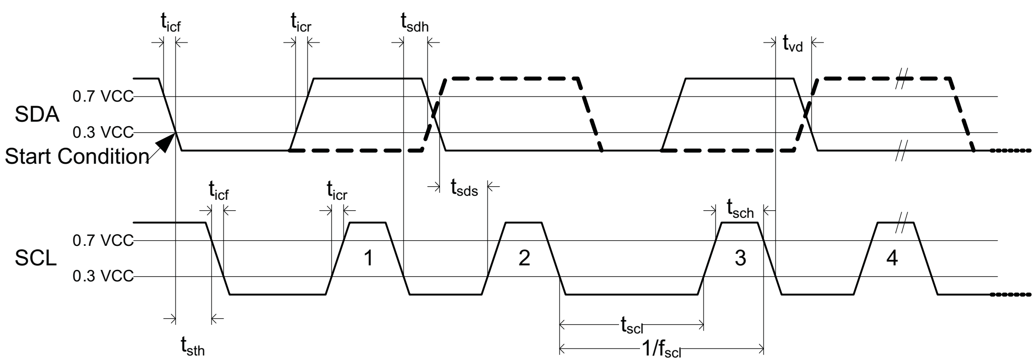


Figure 1. I²C Timing Requirements

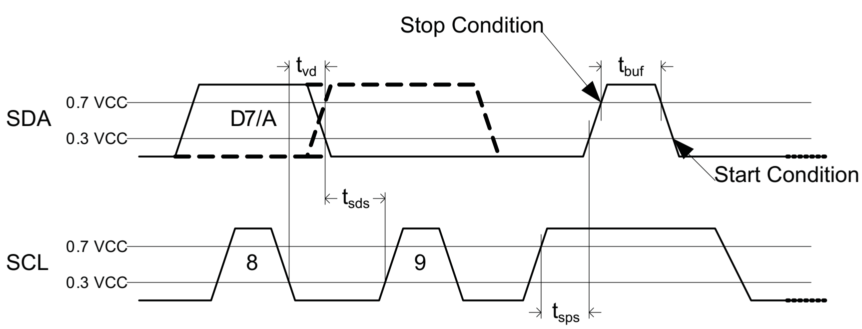


Figure 2. I²C Timing Requirements

TYPICAL PERFORMANCE GRAPHS

**EFFICIENCY
vs
LOAD CURRENT**

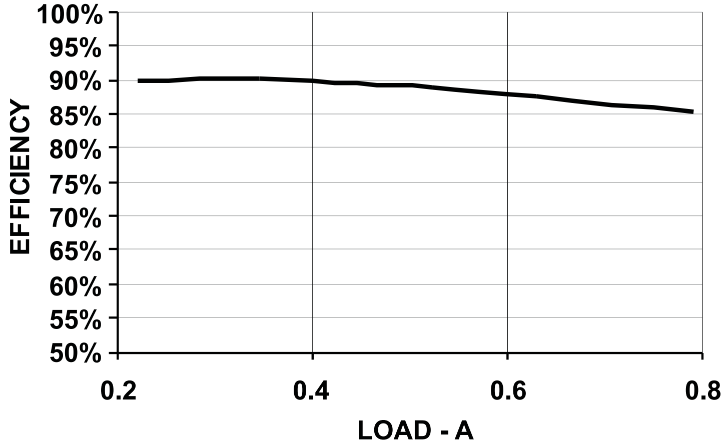


Figure 3.

**EFFICIENCY
vs
OUTPUT VOLTAGE**

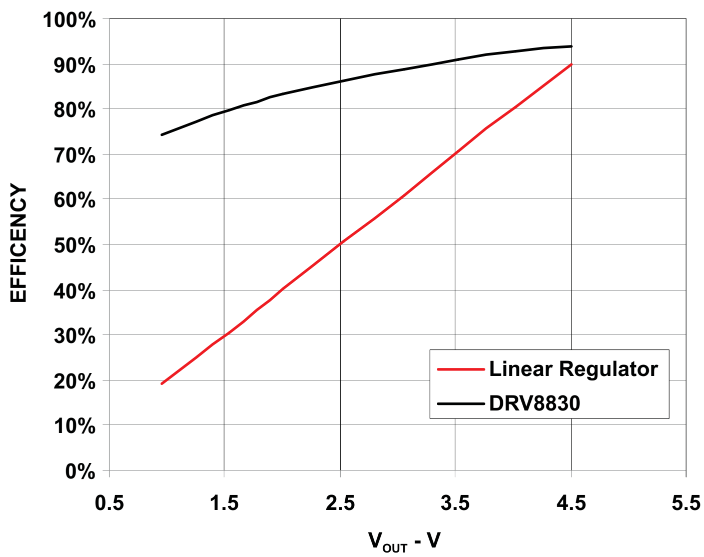


Figure 4.

PRODUCT PREVIEW

FUNCTIONAL DESCRIPTION

PWM Motor Driver

The DRV8830 contains an H-bridge motor driver with PWM voltage-control circuitry with current limit circuitry. A block diagram of the motor control circuitry is shown below.

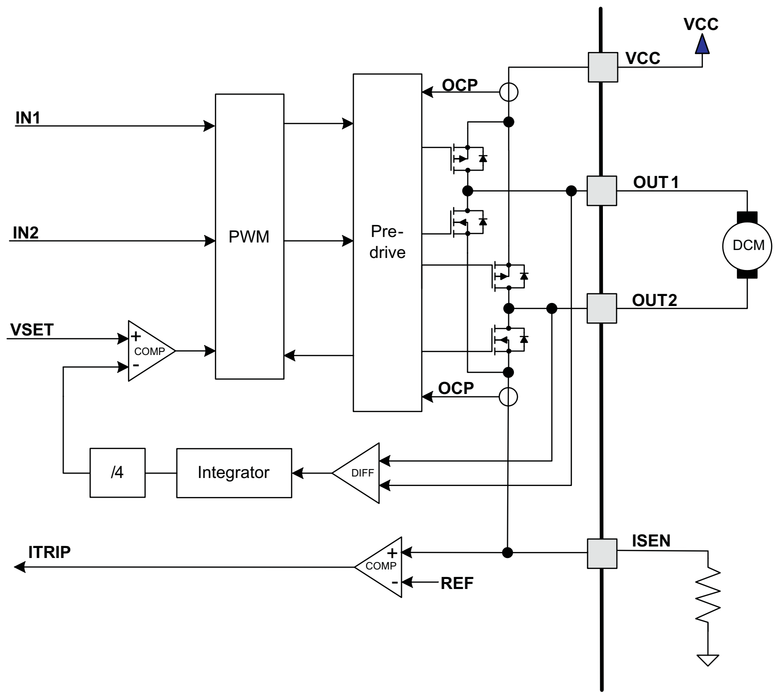


Figure 5. Motor Control Circuitry

Bridge Control

The IN1 and IN2 control bits in the serial interface register enable the H-bridge outputs. The following table shows the logic:

Table 2. H-Bridge Logic

IN1	IN2	OUT1	OUT2	Function
0	0	Z	Z	Standby/coast
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	H	H	Brake

When both bits are zero, the output drivers are disabled and the device is placed into a low-power shutdown state. The current limit fault condition (if present) is also cleared.

At initial power-up, the device will enter the low-power shutdown state.

PRODUCT PREVIEW

Voltage Regulation

The DRV8830 provides the ability to regulate the voltage applied to the motor winding. This feature allows constant motor speed to be maintained even when operating from a varying supply voltage such as a discharging battery.

The DRV8830 uses a pulse-width modulation (PWM) technique instead of a linear circuit to minimize current consumption and maximize battery life.

The circuit monitors the voltage difference between the output pins and integrates it, to get an average DC voltage value. This voltage is divided by 4 and compared to the output voltage of the VSET DAC, which is set through the serial interface. If the averaged output voltage (divided by 4) is lower than VSET, the duty cycle of the PWM output is increased; if the averaged output voltage (divided by 4) is higher than VSET, the duty cycle is decreased.

During PWM regulation, the H-bridge is enabled to drive current through the motor winding during the PWM on time. This is shown in the diagram below as case 1. The current flow direction shown indicates the state when IN1 is high and IN2 is low.

Note that if the programmed output voltage is greater than the supply voltage, the device will operate at 100% duty cycle and the voltage regulation feature will be disabled. In this mode the device behaves as a conventional H-bridge driver.

During the PWM off time, winding current is re-circulated by enabling both of the high-side FETs in the bridge. This is shown as case 2 below.

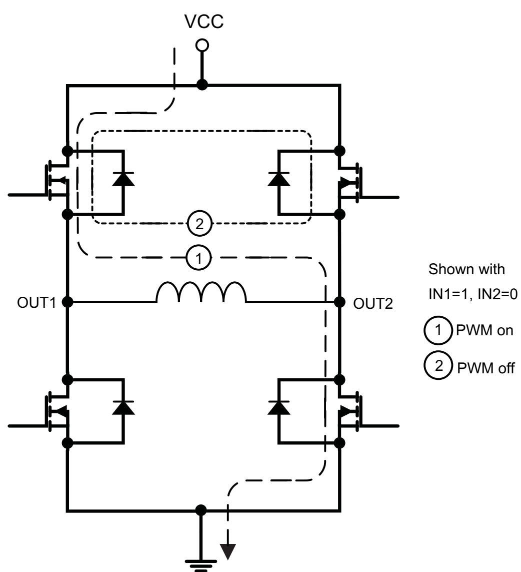


Figure 6. Voltage Regulation

PRODUCT PREVIEW

Voltage Setting (VSET DAC)

The DRV8830 includes an internal reference voltage that is connected to a DAC. This DAC generates a voltage which is used to set the PWM regulated output voltage as described above.

The DAC is controlled by the VSET bits from the serial interface. The commanded output voltage is as follows:

VSET[5..0]	Output Voltage		VSET[5..0]	Output Voltage
0x00h	Reserved		0x20h	2.57
0x01h	Reserved		0x21h	2.65
0x02h	Reserved		0x22h	2.73
0x03h	Reserved		0x23h	2.81
0x04h	Reserved		0x24h	2.89
0x05h	Reserved		0x25h	2.97
0x06h	0.48		0x26h	3.05
0x07h	0.56		0x27h	3.13
0x08h	0.64		0x28h	3.21
0x09h	0.72		0x29h	3.29
0x0Ah	0.80		0x2Ah	3.37
0x0Bh	0.88		0x2Bh	3.45
0x0Ch	0.96		0x2Ch	3.53
0x0Dh	1.04		0x2Dh	3.61
0x0Eh	1.12		0x2Eh	3.69
0x0Fh	1.20		0x2Fh	3.77
0x10h	1.29		0x30h	3.86
0x11h	1.37		0x31h	3.94
0x12h	1.45		0x32h	4.02
0x13h	1.53		0x33h	4.10
0x14h	1.61		0x34h	4.18
0x15h	1.69		0x35h	4.26
0x16h	1.77		0x36h	4.34
0x17h	1.85		0x37h	4.42
0x18h	1.93		0x38h	4.50
0x19h	2.01		0x39h	4.58
0x1Ah	2.09		0x3Ah	4.66
0x1Bh	2.17		0x3Bh	4.74
0x1Ch	2.25		0x3Ch	4.82
0x1Dh	2.33		0x3Dh	4.90
0x1Eh	2.41		0x3Eh	4.98
0x1Fh	2.49		0x3Fh	5.06

The voltage can be calculated as 4 x VREF x (VSET +1) / 64, where VREF is the internal 1.285-V reference.

PRODUCT PREVIEW

Current Limit

A current limit circuit is provided to protect the system in the event of an overcurrent condition, such as what would be encountered if driving a DC motor at start-up or with an abnormal mechanical load (stall condition).

The motor current is sensed by monitoring the voltage across an external sense resistor. When the voltage exceeds a reference voltage of 100 mV, the PWM duty cycle is reduced to limit the current through the motor to this value. This current limit allows for starting the motor while controlling the current.

If the current limit condition persists for some time, it is likely that a fault condition has been encountered, such as the motor being run into a stop or a stalled condition. An overcurrent event must persist for approximately 250 ms before the fault is registered. After 250 ms, a fault signaled to the host by driving the FAULTn signal low and setting the FAULT and ILIMIT bits in the serial interface register. Operation of the motor driver will continue.

The current limit fault condition is cleared by setting both IN1 and IN2 to zero to disable the motor current, by putting the device into the shutdown state (IN1 and IN2 both set to 1), by setting the CLEAR bit in the fault register, or by removing and re-applying power to the device.

The resistor used to set the current limit must be less than 1 Ω. If the current limit feature is not needed, the ISENSE pin may be directly connected to ground.

Protection Circuits

The DRV8830 is fully protected against undervoltage, overcurrent and overtemperature events. A FAULTn pin is available to signal a fault condition to the system, as well as a FAULT register in the serial interface that allows determination of the fault source.

Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge will be disabled, the FAULTn signal will be driven low, and the FAULT and OCP bits in the FAULT register will be set. The device will remain disabled until the CLEAR bit in the FAULT register is written to 1, or VCC is removed and re-applied.

Overcurrent conditions on both high and low side devices. A short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Note that OCP is independent of the current limit function, which is typically set to engage at a lower current level; the OCP function is intended to prevent damage to the device under abnormal (e.g., short-circuit) conditions.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled, the FAULTn signal will be driven low, and the FAULT and OTS bits in the serial interface register will be set. Once the die temperature has fallen to a safe level operation will automatically resume.

Undervoltage Lockout (UVLO)

If at any time the voltage on the VCC pins falls below the undervoltage lockout threshold voltage, all FETs in the H-bridge will be disabled, the FAULTn signal will be driven low, and the FAULT and UVLO bits in the FAULT register will be set. Operation will resume when VCC rises above the UVLO threshold.

I^2C-Compatible Serial Interface

The I^2C interface allows control and monitoring of the DRV8830 by a microcontroller. I^2C is a two-wire serial interface developed by Philips Semiconductor (see I^2C – Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with off-chip pull-up resistors. When the bus is idle, both SDA and SCL lines are pulled high.

A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer.

A slave device receives and/or transmits data on the bus under control of the master device. This device operates only as a slave device.

I²C communication is initiated by a master sending a start condition, a high-to-low transition on the SDA I/O while SCL is held high. After the start condition, the device address byte is sent, most-significant bit (MSB) first, including the data direction bit (R/W). After receiving a valid address byte, this device responds with an acknowledge, a low on the SDA I/O during the high of the acknowledge-related clock pulse.

The lower three bits of the device address are input from pins A0 - A1, which can be tied to VCC (logic high), GND (logic low), or left open. These three address bits are latched into the device at power-up, so cannot be changed dynamically.

The upper address bits of the device address are fixed at 0xC0h, so the device address is as follows:

A1 PIN	A0 PIN	A3..A0 BITS (as below)	ADDRESS (WRITE)	ADDRESS (READ)
0	0	0000	0xC0h	0xC1h
0	open	0001	0xC2h	0xC3h
0	1	0010	0xC4h	0xC5h
open	0	0011	0xC6h	0xC7h
open	open	0100	0xC8h	0xC9h
open	1	0101	0xCAh	0xCBh
1	0	0110	0xCCh	0xCDh
1	open	0111	0xCEh	0xCFh
1	1	1000	0xD0h	0xD1h

The DRV8830 does not respond to the general call address.

A data byte follows the address acknowledge. If the R/W bit is low, the data is written from the master. If the R/W bit is high, the data from this device are the values read from the register previously selected by a write to the subaddress register. The data byte is followed by an acknowledge sent from this device. Data is output only if complete bytes are received and acknowledged. A stop condition, which is a low-to-high transition on the SDA I/O while the SCL input is high, is sent by the master to terminate the transfer.

A master bus device must wait at least 60 μs after power is applied to VCC to generate a START condition.

I²C transactions are shown in the timing diagrams below:

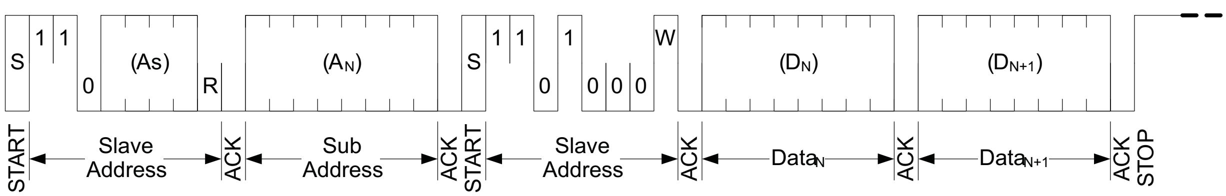


Figure 7. I²C Read Mode

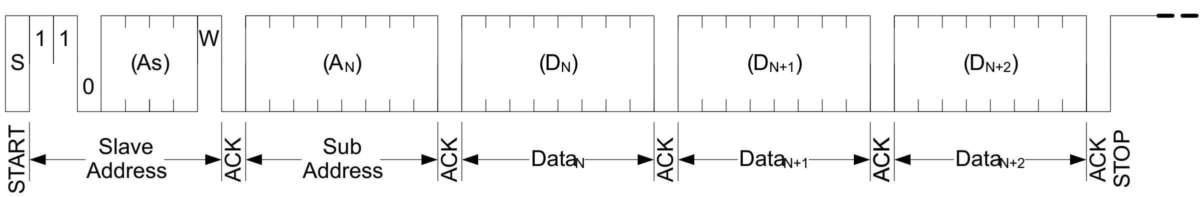


Figure 8. I²C Write Mode

PRODUCT PREVIEW

I²C Register Map

REGISTER	SUB ADDRESS (HEX)	REGISTER NAME	DEFAULT VALUE	DESCRIPTION
0	0x00	CONTROL	0x00h	Sets state of outputs and output voltage
1	0x01	FAULT	0x00h	Allows reading and clearing of fault conditions

REGISTER 0 – CONTROL

The CONTROL register is used to set the state of the outputs as well as the DAC setting for the output voltage. The register is defined as follows:

D7 - D2	D1	D0
VSET[5..0]	IN2	IN1

VSET[5..0]: Sets DAC output voltage. Refer to Voltage Setting above.

IN2: Along with IN1, sets state of outputs. Refer to Bridge Control above.

IN1: Along with IN2, sets state of outputs. Refer to Bridge Control above.

REGISTER 1 – FAULT

The FAULT register is used to read the source of a fault condition, and to clear the status bits that indicated the fault. The register is defined as follows:

D7	D6 - D5	D4	D3	D2	D1	D0
CLEAR	Unused	ILIMIT	OTS	UVLO	OCP	FAULT

CLEAR: When written to 1, clears the fault status bits

ILIMIT: If set, indicates the fault was caused by an extended current limit event

OTS: If set, indicates that the fault was caused by an overtemperature (OTS) condition

UVLO: If set, indicates the fault was caused by an undervoltage lockout

OCP: If set, indicates the fault was caused by an overcurrent (OCP) event

FAULT: Set if any fault condition exists

PRODUCT PREVIEW

THERMAL INFORMATION

Thermal Protection

The DRV8830 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Power Dissipation

Power dissipation in the DRV8830 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation when running a stepper motor can be roughly estimated by Equation 1.

$$P_{TOT} = 2 \bullet R_{DS(ON)} \bullet (I_{OUT(RMS)})^2 \quad (1)$$

where P_{TOT} is the total power dissipation, $R_{DS(ON)}$ is the resistance of each FET, and $I_{OUT(RMS)}$ is the RMS output current being applied to each winding. $I_{OUT(RMS)}$ is equal to the approximately 0.7x the full-scale output current setting. The factor of 2 comes from the fact that at any instant two FETs are conducting winding current for each winding (one high-side and one low-side).

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report SLMA002, " PowerPAD™ Thermally Enhanced Package" and TI application brief SLMA004, " PowerPAD™ Made Easy", available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

PRODUCT PREVIEW

IMPORTANT NOTICE

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