

PSRAM

2-Mbit (128K x 16)

Pseudo Static RAM

Features

- Wide voltage range: 2.7V–3.6V
- Access Time: 55 ns, 70 ns
- Ultra-low active power
 - Typical active current: 1mA @ f = 1 MHz
 - Typical active current: 14 mA @ f = fmax (For 55-ns)
 - Typical active current: 8 mA @ f = fmax (For 70-ns)
- Ultra low standby power
- Automatic power-down when deselected
- CMOS for optimum speed/power

Functional Description

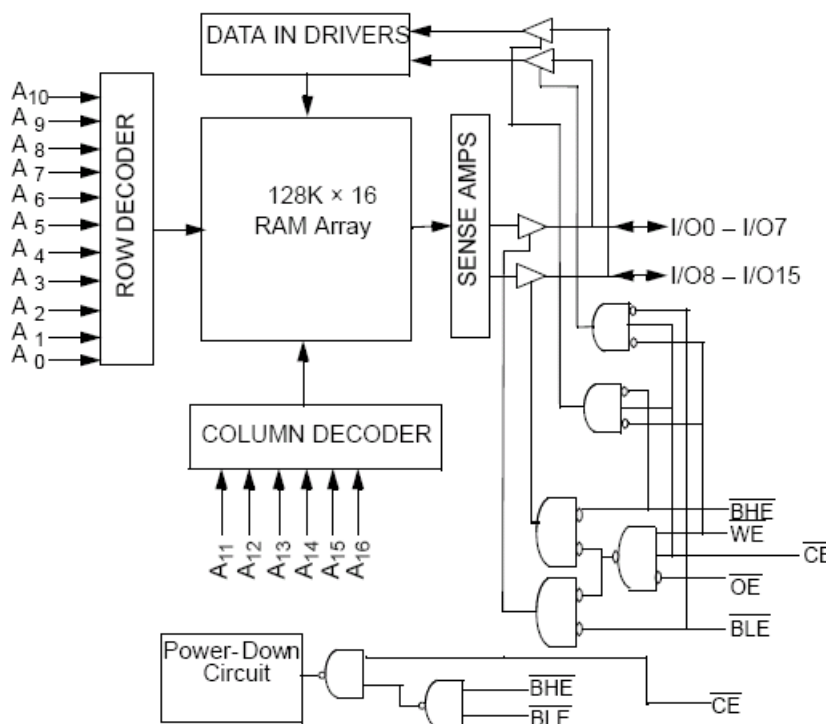
The M24L216128SA is a high-performance CMOS Pseudo Static RAM organized as 128K words by 16 bits that supports an asynchronous memory interface. This device features advanced circuit design to provide ultra-low active current. This is ideal for portable applications such as cellular telephones. The device can be put into standby mode when deselected ($\overline{CE}$ HIGH or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when the chip is deselected ($\overline{CE}$ HIGH), or when the outputs are disabled ($\overline{OE}$ HIGH), or

when both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

Writing to the device is accomplished by asserting Chip Enable ($\overline{CE}$ LOW) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₆). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₆).

Reading from the device is accomplished by asserting Chip Enable ($\overline{CE}$ LOW) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. Refer to the truth table for a complete description of read and write modes.

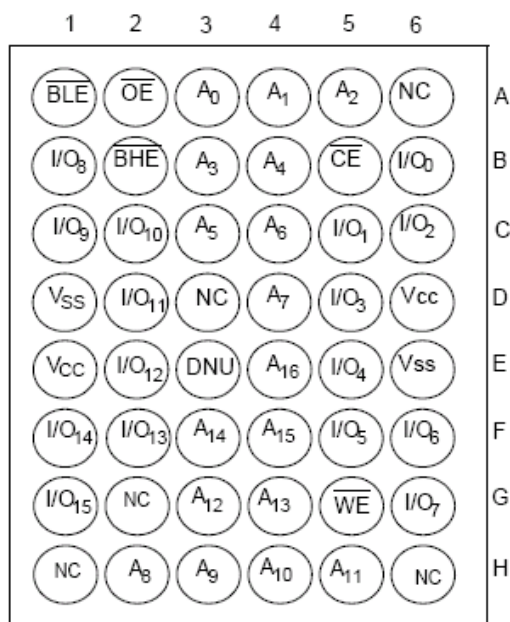
Logic Block Diagram



Pin Configuration[2, 3, 4]

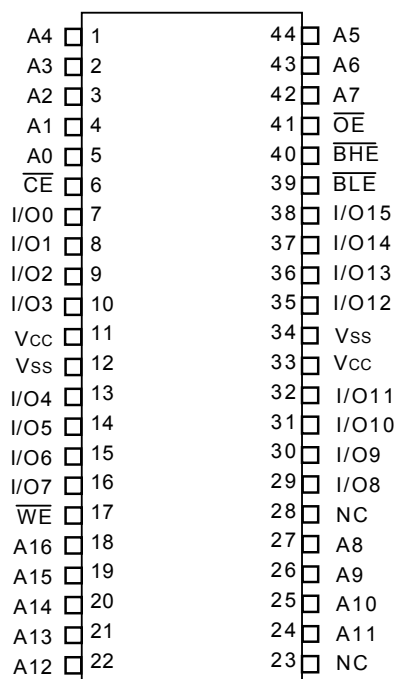
48-ball VFBGA

Top View



44-pin TSOPII

Top View



Product Portfolio Product

Product	V _{CC} Range (V)			Speed(ns)	Power Dissipation					
					Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
					f = 1MHz		f = fmax			
	Min.	Typ.	Max.		Typ.[5]	Max.	Typ.[5]	Max.	Typ. [5]	Max.
M24L216128SA	2.7	3.0	3.6	55	1	5	14	22	9	40
				70			8	15		

Notes:

- 2.Ball D3, H1, G2 and ball H6 for the FBGA package can be used to upgrade to a 4-Mbit, 8-Mbit, 16-Mbit and a 32-Mbit density, respectively.
- 3.NC "no connect"—not connected internally to the die.
- 4.DNU (Do Not Use) pins have to be left floating or tied to V_{SS} to ensure proper application.
- 5.Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25°C.

Maximum Ratings

(Above which the useful life may be impaired. For user guide-lines, not tested.)

Storage Temperature-65°C to +150°C
Ambient Temperature with
Power Applied-55°C to +125°C
Supply Voltage to Ground Potential-0.4V to 4.6V
DC Voltage Applied to Outputs
in High-Z State[3, 4, 5]-0.4V to 3.7V
DC Input Voltage[3, 4, 5]-0.4V to 3.7V
Output Current into Outputs (LOW)20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)
Latch-up Current> 200 mA

Operating Range

Range	Ambient Temperature(T _A)	V _{CC}
Extended	-25°C to +85°C	2.7V to 3.6V
Industrial	-40°C to +85°C	2.7V to 3.6V

Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions		-55			-70			Unit
				Min.	Typ. [5]	Max.	Min.	Typ. [5]	Max.	
V _{CC}	Supply Voltage			2.7	3.0	3.6	2.7	3.0	3.6	V
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA	V _{CC} = 2.70V	V _{CC} -0.4			V _{CC} -0.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA	V _{CC} = 2.70V			0.4			0.4	V
V _{IH}	Input HIGH Voltage	V _{CC} = 2.7V to 3.6V		0.8* V _{CC}		V _{CC} +0.4V	0.8* V _{CC}		V _{CC} +0.4V	V
V _{IL}	Input LOW Voltage			-0.4		0.4	-0.4		0.4	V
I _{IX}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CC}		-1		+1	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled		-1		+1	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC}	V _{CC} = V _{CCmax} I _{OUT} = 0mA CMOS levels		14	22		8	15	mA
		f = 1 MHz			1	5		1	5	mA
I _{SB1}	Automatic $\overline{\text{CE}}$ Power-Down Current —CMOS Inputs	$\overline{\text{CE}} \geq V_{\text{CC}} - 0.2\text{V}$ $V_{\text{IN}} \geq V_{\text{CC}} - 0.2\text{V}$, $V_{\text{IN}} \leq 0.2\text{V}$, $f = f_{\text{MAX}}$ (Address and Data Only), $f = 0$ ($\overline{\text{OE}}$, $\overline{\text{WE}}$, $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$), $V_{\text{CC}}=3.6\text{V}$			40	250		40	250	μA
I _{SB2}	Automatic $\overline{\text{CE}}$ Power-Down Current —CMOS Inputs	$\overline{\text{CE}} \geq V_{\text{CC}}-0.2\text{V}$ $V_{\text{IN}} \geq V_{\text{CC}} - 0.2\text{V}$ or $V_{\text{IN}} \leq 0.2\text{V}$, $f = 0$, $V_{\text{CC}} =3.6\text{V}$			9	40		9	40	μA

Capacitance[9]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	TA = 25°C, f = 1 MHz	8	pF
C _{OUT}	Output Capacitance	V _{CC} = V _{CC(typ)}	8	pF

Thermal Resistance[9]

Parameter	Description	Test Conditions	BGA	Unit
ΘJA	Thermal Resistance(Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/ JESD51.	55	°C/W
ΘJC	Thermal Resistance (Junction to Case)		17	°C/W

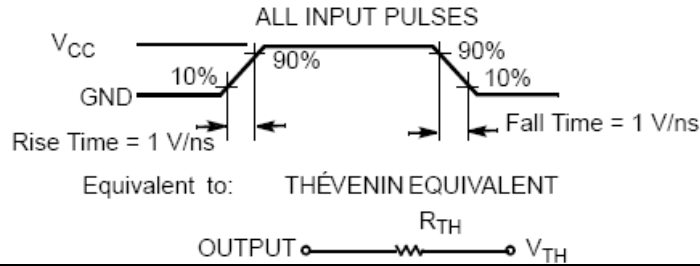
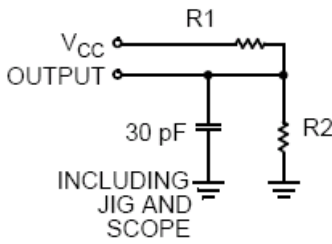
Notes: 6.V_{IL(MIN)} = -0.5V for pulse durations less than 20 ns.

7.V_{IH(Max)} = V_{CC} + 0.5V for pulse durations less than 20 ns.

8.Overshoot and undershoot specifications are characterized and are not 100% tested.

9.Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Parameters	3.0V V _{CC}	Unit
R1	22000	Ω
R2	22000	Ω
R _{TH}	11000	Ω
V _{TH}	1.50	V

Switching Characteristics Over the Operating Range[10]

Parameter	Description	-55 [14]		-70		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t _{RC}	Read Cycle Time	55[14]		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	5		10		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		55		70	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		25		35	ns
t _{LZOE}	$\overline{OE}$ LOW to LOW Z[11, 13]	5		5		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z[11, 13]		25		25	ns
t _{LZCE}	$\overline{CE}$ LOW to Low Z[11, 13]	2		5		ns
t _{HZCE}	$\overline{CE}$ HIGH to High Z[11, 13]		25		25	ns
t _{DBE}	$\overline{BLE} / \overline{BHE}$ LOW to Data Valid		55		70	ns
t _{LZBE}	$\overline{BLE} / \overline{BHE}$ LOW to Low Z[11, 13]	5		5		ns
t _{HZBE}	$\overline{BLE} / \overline{BHE}$ HIGH to HIGH Z[11, 13]		10		25	ns
t _{SK} [14]	Address Skew		0		10	ns
Write Cycle[12]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	45		60		ns
t _{AW}	Address Set-Up to Write End	45		60		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	40		45		ns

Notes:

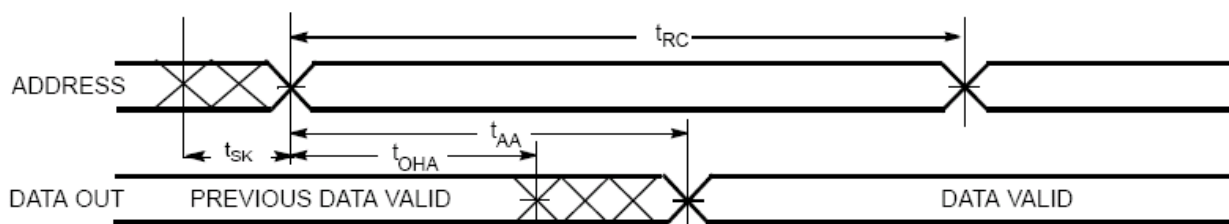
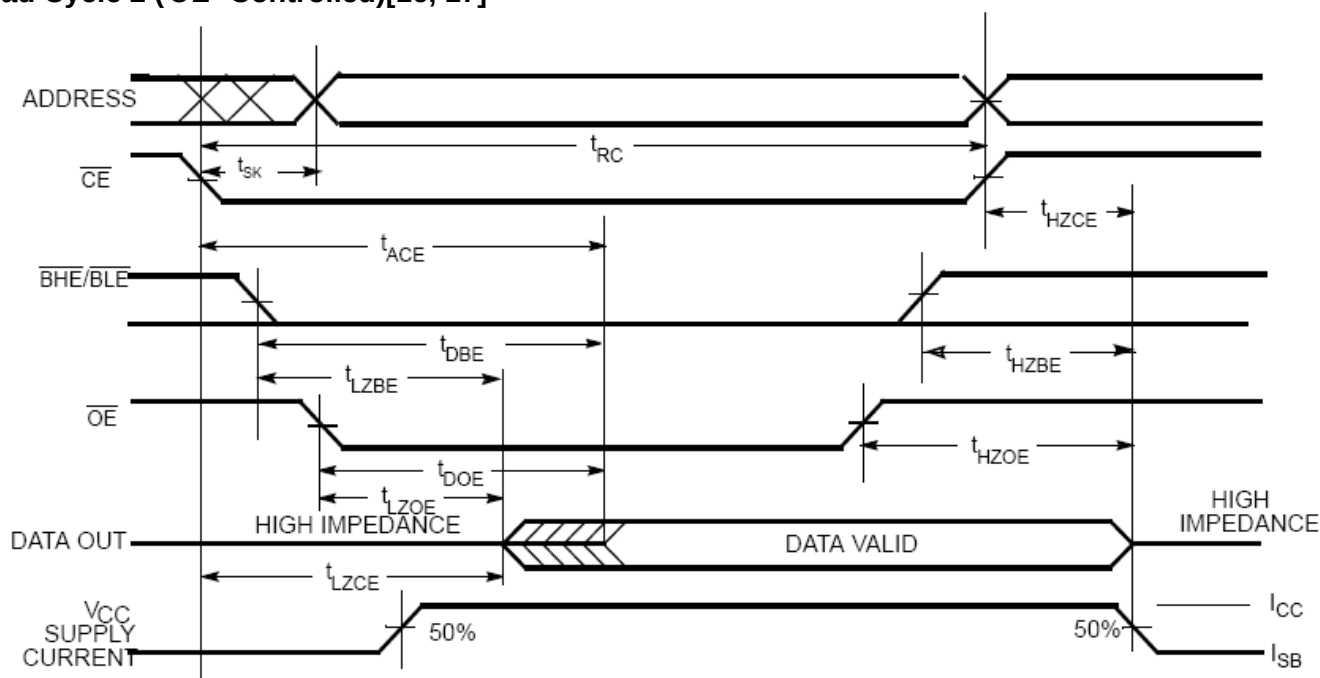
- Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 ns/V, timing reference levels of V_{CC(typ)}/2, input pulse levels of 0V to V_{CC(typ)}, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
- t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
- The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
- High-Z and Low-Z parameters are characterized and are not 100% tested.
- To achieve 55-ns performance, the read access should be $\overline{CE}$ controlled. In this case t_{ACE} is the critical parameter and t_{SK} is satisfied when the addresses are stable prior to chip enable going active. For the 70-ns cycle, the addresses must be stable within 10 ns after the start of the read cycle.

Switching Characteristics Over the Operating Range (continued)[10]

Parameter	Description	-55 [14]		-70		Unit
		Min.	Max.	Min.	Max.	
t_{BW}	BLE/BHE LOW to Write End	50		60		ns
t_{SD}	Data Set-Up to Write End	25		45		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[11, 13]		25		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[11, 13]	5		5		ns

Switching Waveforms

Read Cycle 1 (Address Transition Controlled)[15, 16, 17]

Read Cycle 2 ($\overline{OE}$ Controlled)[16, 17]

Notes:

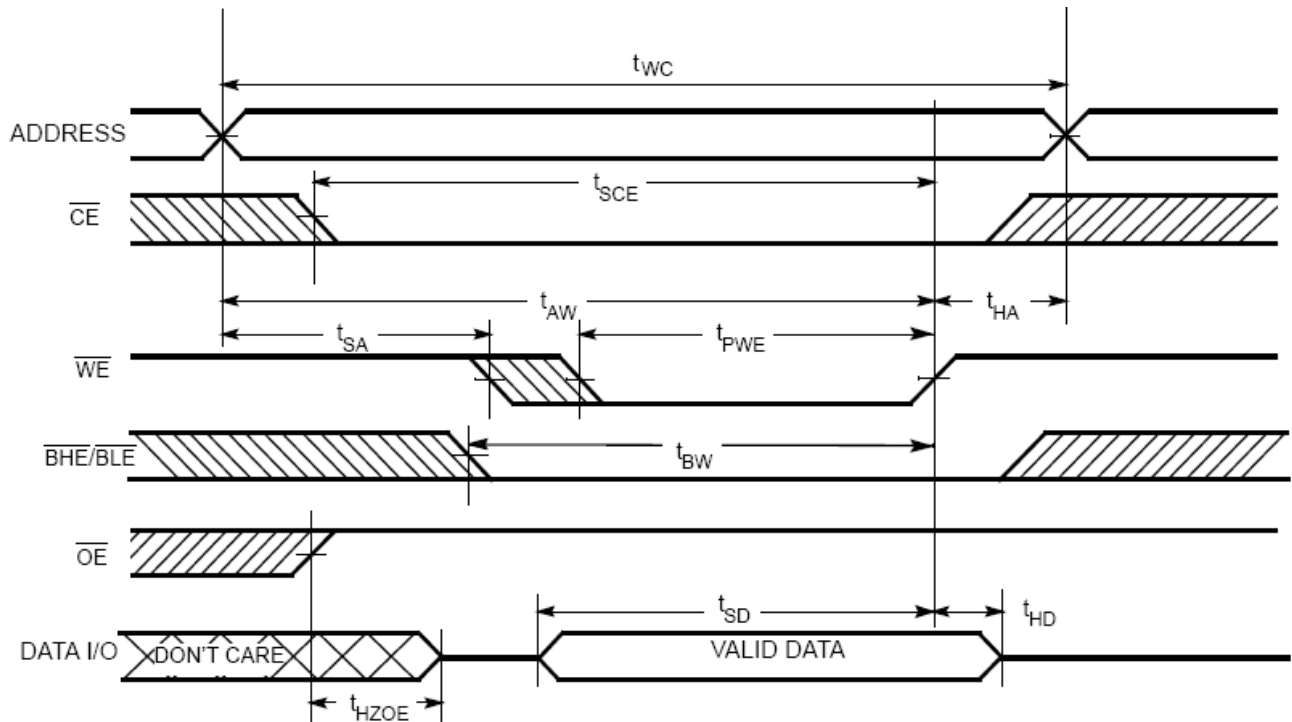
15. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL} .

16. $\overline{WE}$ is HIGH for Read Cycle.

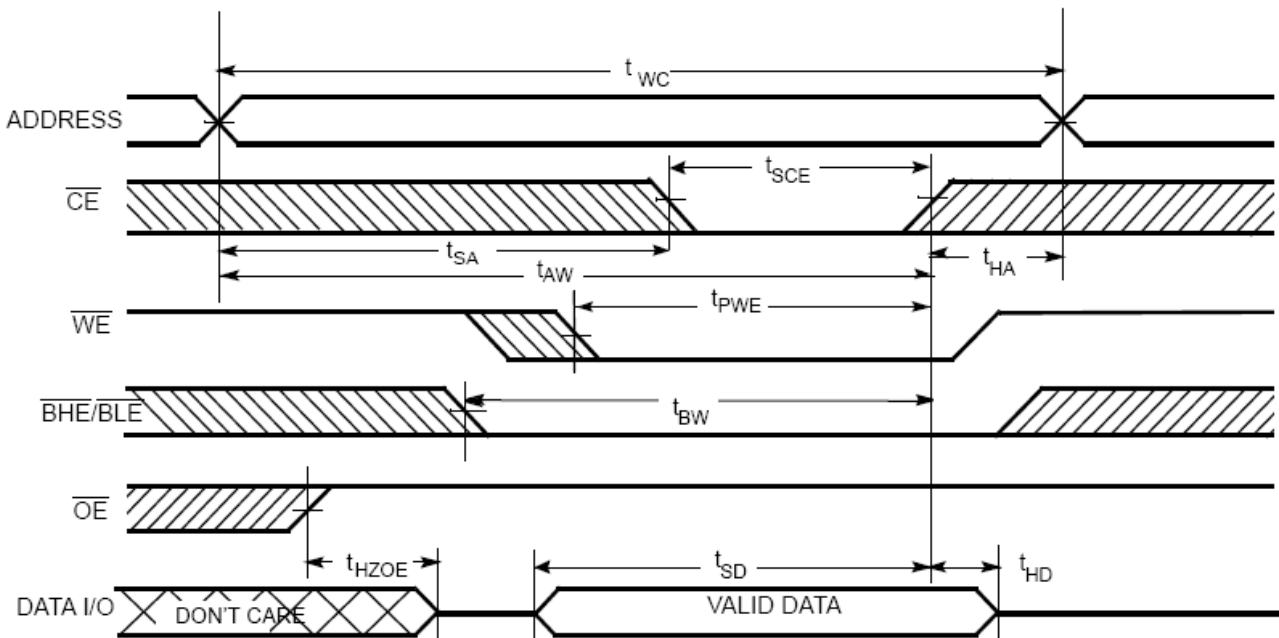
17. For the 55-ns Cycle, the addresses must not toggle once the read is started on the device. For the 70-ns Cycle, the addresses must be stable within 10 ns after the start of the read cycle.

Switching Waveforms (continued)

Write Cycle 1 ($\overline{WE}$ Controlled)[12, 13, 18, 19, 20]



Write Cycle 2 ($\overline{CE}$ Controlled)[12, 13, 18, 19, 20]



Notes:

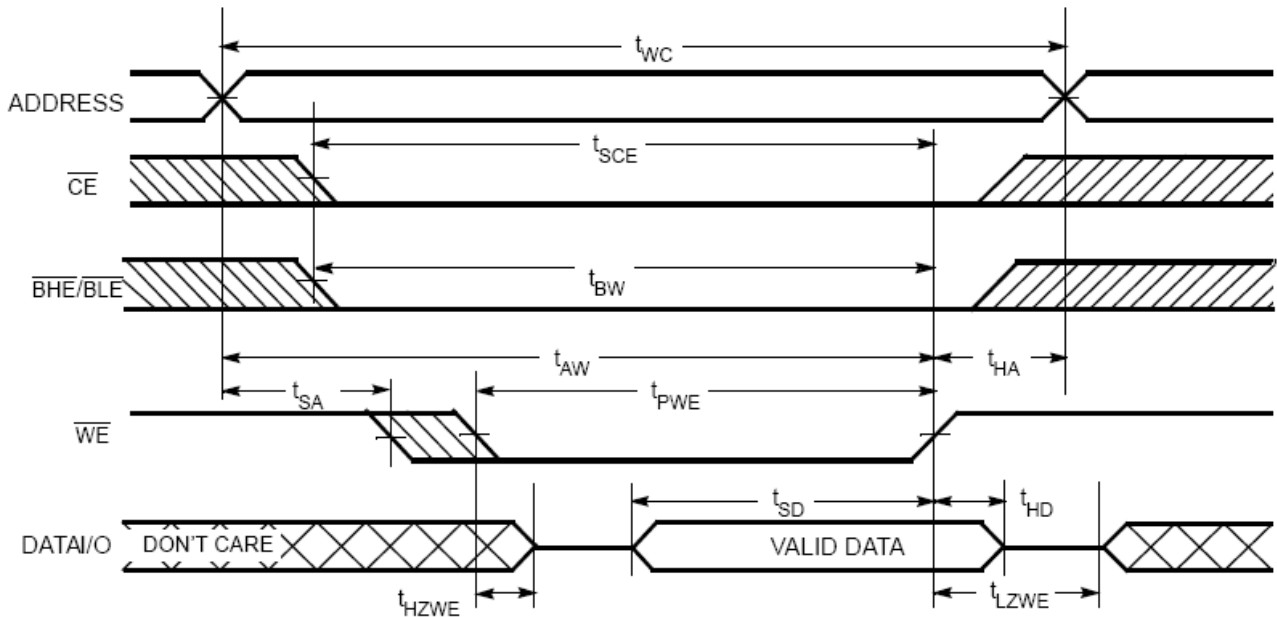
18.Data I/O is high impedance if $\overline{OE} \geq V_{IH}$.

19.If Chip Enable goes INACTIVE with $\overline{WE} = V_{IH}$, the output remains in a high-impedance state.

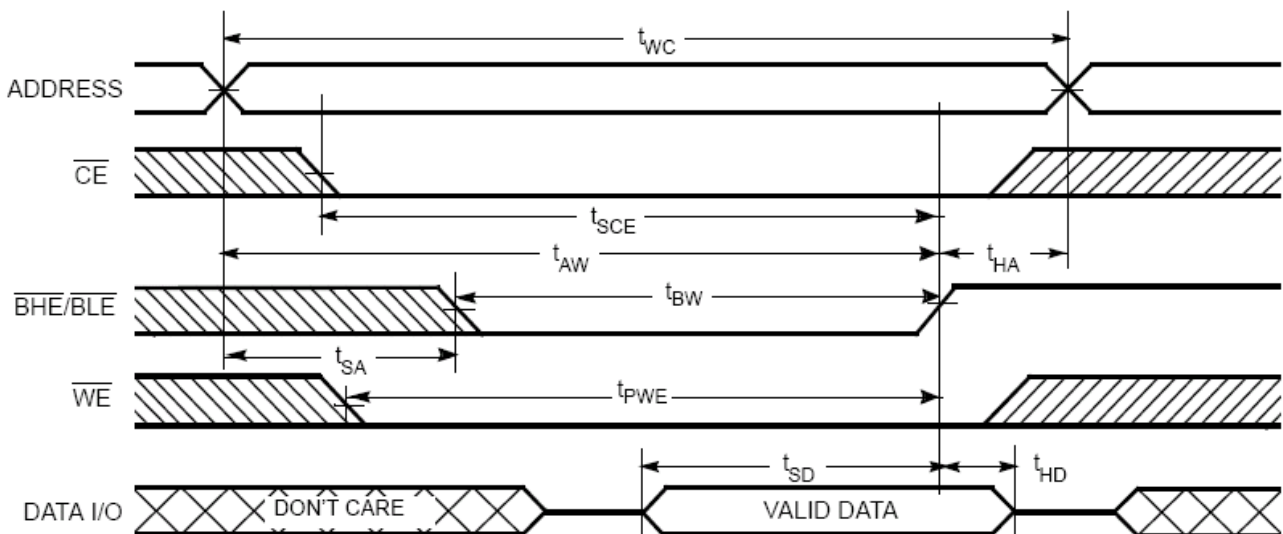
20.During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[19, 20]



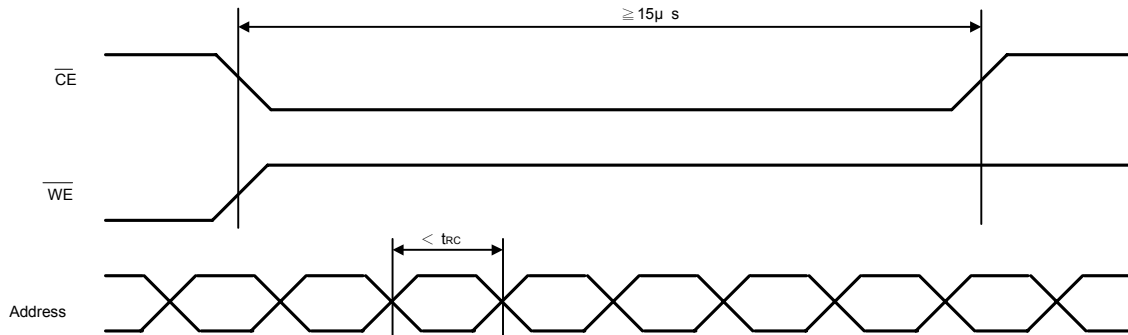
Write Cycle 4 ($\overline{BHE/BLER}$ Controlled, $\overline{OE}$ LOW)[19, 20]



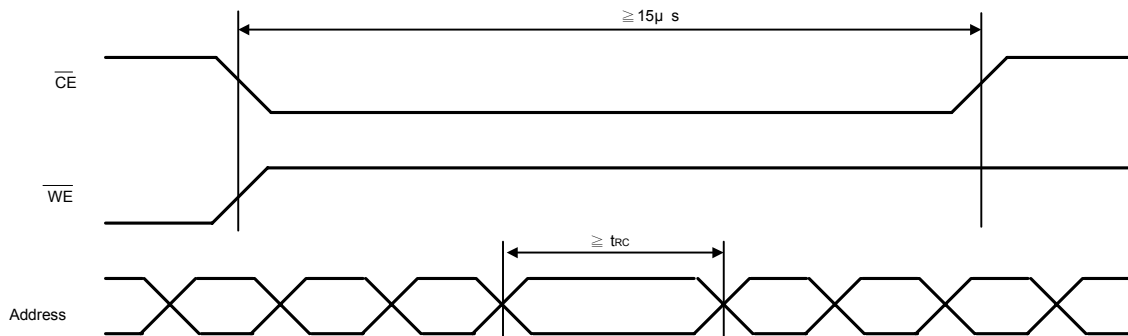
Avoid Timing

ESMT Pseudo SRAM has a timing which is not supported at read operation, If your system has multiple invalid address signal shorter than t_{RC} during over $15\mu s$ at read operation shown as in Abnormal Timing, it requires a normal read timing at least during $15\mu s$ shown as in Avoidable timing 1 or toggle $\overline{CE}$ to high ($\geq t_{RC}$) one time at least shown as in Avoidable Timing 2.

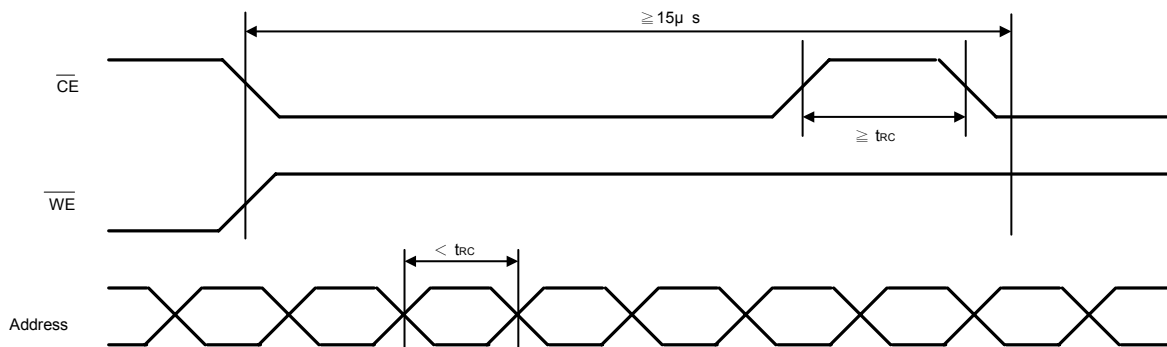
Abnormal Timing



Avoidable Timing 1



Avoidable Timing 2



Truth Table[21]

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_0 – I/O_7); High Z (I/O_8 – I/O_{15})	Read	Active (I_{CC})
L	H	L	L	H	High Z (I/O_0 – I/O_7); Data Out (I/O_8 – I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_0 – I/O_7); High Z (I/O_8 – I/O_{15})	Write	Active (I_{CC})
L	L	X	L	H	High Z (I/O_0 – I/O_7); Data In (I/O_8 – I/O_{15})	Write	Active (I_{CC})

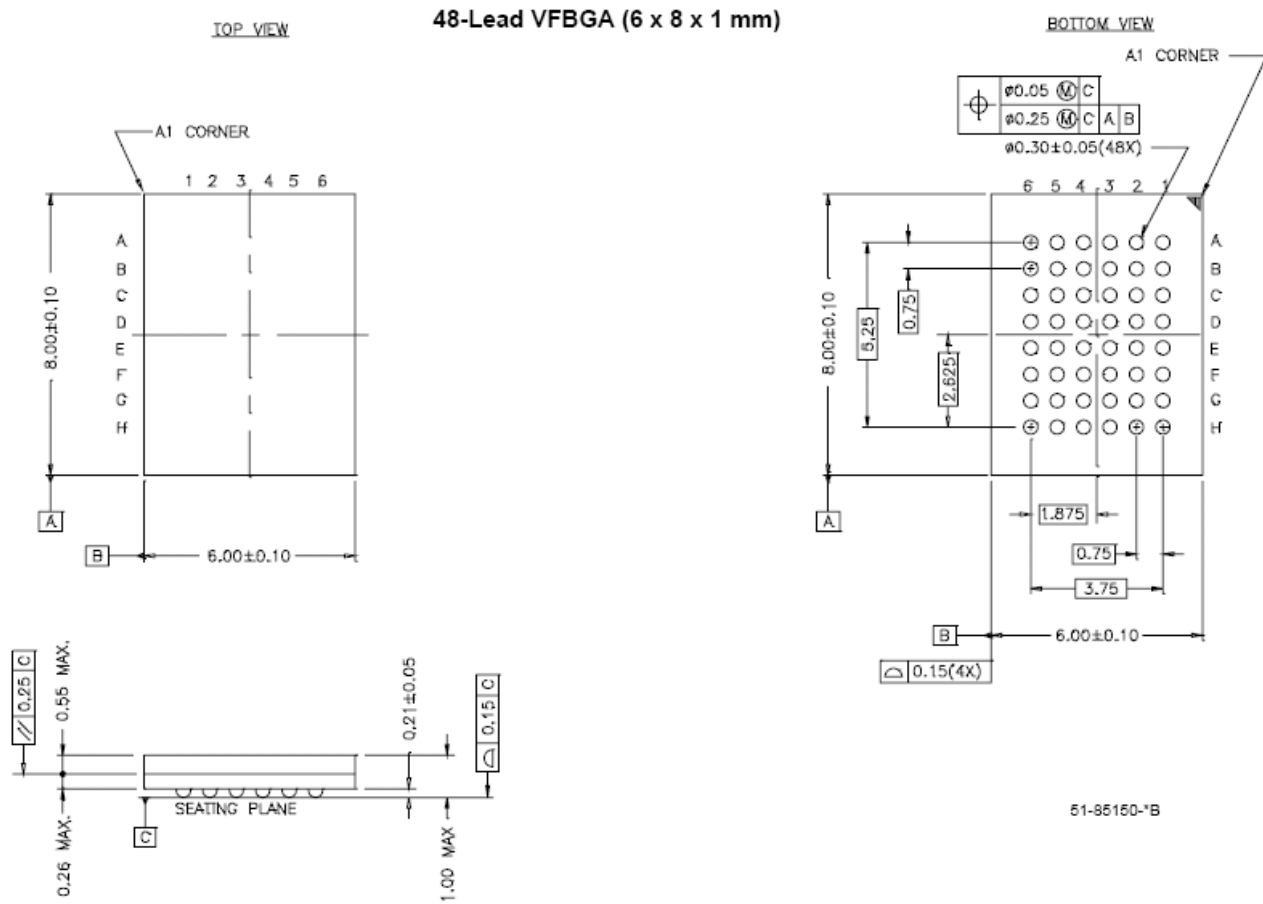
Note:

21.H = Logic HIGH, L = Logic LOW, X = Don't Care.

Ordering information

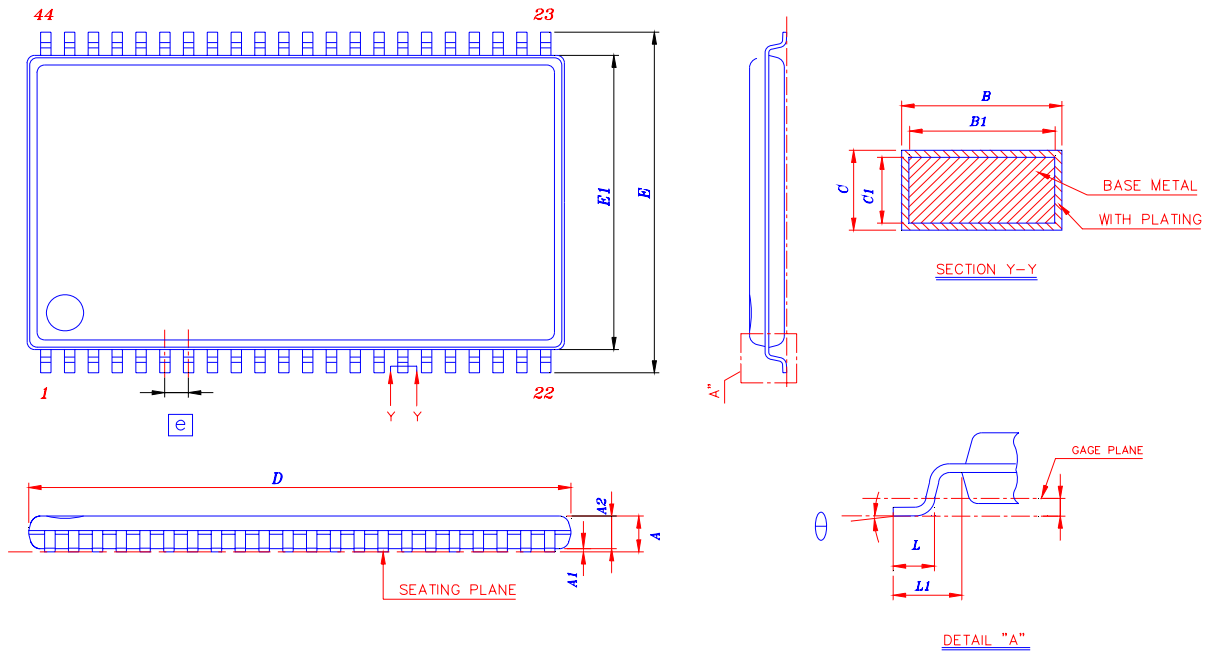
Speed(ns)	Ordering Code	Package Type	Operating Range
55	M24L216128SA-55BEG	48-ball Very Fine Pitch BGA (6.0x8.0x1.0mm) (Pb-free)	Extended
70	M24L216128SA-70BEG	48-ball Very Fine Pitch BGA (6.0x8.0x1.0mm) (Pb-free)	Extended
55	M24L216128SA-55TEG	44-pin TSOPII (Pb-free)	Extended
70	M24L216128SA-70TEG	44-pin TSOPII (Pb-free)	Extended
55	M24L216128SA-55BIG	48-ball Very Fine Pitch BGA (6.0x8.0x1.0mm) (Pb-free)	Industrial
70	M24L216128SA-70BIG	48-ball Very Fine Pitch BGA (6.0x8.0x1.0mm) (Pb-free)	Industrial
55	M24L216128SA-55TIG	44-pin TSOPII (Pb-free)	Industrial
70	M24L216128SA-70TIG	44-pin TSOPII (Pb-free)	Industrial

Package Diagram



44-LEAD TSOP(II)

PRAM(400mil)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.042
B	0.30	—	0.45	0.012	—	0.018
B1	0.30	0.35	0.40	0.012	0.014	0.016
C	0.12	—	0.21	0.005	—	0.008
C1	0.10	—	0.16	0.004	—	0.006
D	18.28	18.41	18.54	0.720	0.725	0.730
ZD	0.805 REF			0.0317 REF		
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.4
L	0.40	0.59	0.69	0.016	0.023	0.027
L1	0.80 REF			0.031 REF		
e	0.80 BSC			0.0315 BSC		
θ	0°	—	8°	0°	—	8°

Revision History

Revision	Date	Description
1.0	2007.05.11	Original
1.1	2008.02.29	1. Add 44-pin TSOPII package 2. Add Avoid timing
1.2	2008.07.04	1. Move Revision History to the last 2. Modify voltage range 2.7V~3.3V to 2.7V~3.6V 3. Add Industrial grade

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