16-BIT 40-KSPS LOW POWER SAMPLING ANALOG-TO-DIGITAL CONVERTER WITH INTERNAL REFERENCE AND PARALLEL/SERIAL INTERFACE

FEATURES

- 40-kHz Min Sampling Rate
- Very Low Power: 25 mW
- ±3.33-V, ±5-V, ±10-V, 4-V, and 10-V Input Ranges
- 89.9-dB SINAD with 10-kHz Input
- ±1.5 LSB Max INL
- ±1 LSB Max DNL, 16-Bit NMC
- ±5-mV BPZ, ±0.4 PPM/°C BPZ Drift
- 87-dB Min SINAD, 96-dB Min SFDR
- Uses Internal or External 2.5-V Reference
- No External Calibration Resistors Required
- Single 5-V Analog Supply
  - 40-mW Max Power Dissipation
  - 50-µW Max Power-Down Mode
- 20-Mhz Compatible SPI
- Global CONV and 3-Stated Bus for Multi-Chip Simultaneous S/H Operation
- Pin-Compatible with ADS7813 and 12-Bit ADS7812/8512
- SO-16 Package

APPLICATIONS

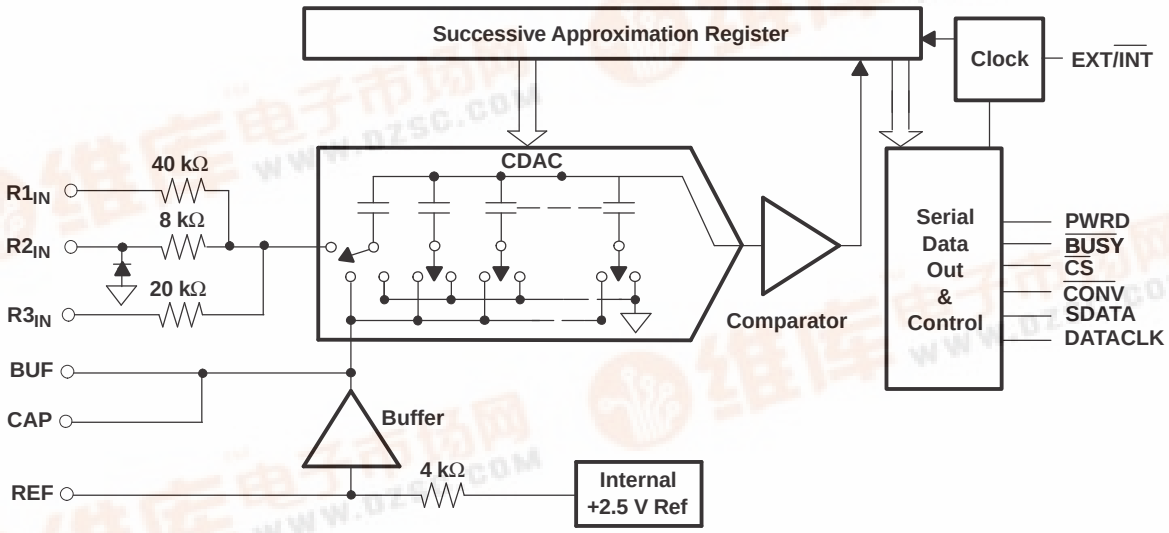
- Industrial Process Control
- Test Equipment
- Robotics
- DSP Servo Control
- Medical Instrumentation
- Portable Data Acquisition Systems

DESCRIPTION

The ADS8513 is a complete low-power, single 5-V supply, 16-bit sampling analog-to-digital (A/D) converter. It contains a complete 16-bit capacitor-based, successive approximation register (SAR) A/D converter with sample and hold, clock, reference, and serial data interface. The converter can be configured for a variety of input ranges including ±10 V, ±5 V, 0 V to 10 V, and 0.5 V to 4.5 V. A high-impedance, 0.3-V to 2.8-V input is also available with input impedance greater than 10 MΩ. For most input ranges, the input voltage can swing to 25 V or –25 V without damage to the converter.

An SPI-compatible serial interface allows data to be synchronized to an internal or external clock. The ADS8513 is specified at 40-kHz sampling rate over the industrial –40°C to 85°C temperature range.

PRODUCT PREVIEW



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PACKAGE/ORDERING INFORMATION

PRODUCT	MINIMUM INL (LSB)	NO MISSING CODE	MINIMUM SINAD (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA, QTY
ADS8513IB	±1.5	16	89.9	-40°C to 85°C	SO-16	DW	ADS8513IBDW	Tube, 20
							ADS8513IBDWR	Tape and Reel, 1000
ADS8513I	±3	15	88	-40°C to 85°C	SO-16	DW	ADS8513IDW	Tube, 20
							ADS8513IDWR	Tape and Reel, 1000

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
Analog inputs	$R1_{IN}$	±25 V
	$R2_{IN}$	±25 V
	$R3_{IN}$	±25 V
	REF	$+V_{ANA}$ + 0.3 V to AGND2 - 0.3 V
Ground voltage differences	DGND, AGND, GND	±0.3 V
	$+V_A$, V_S	6 V
	$+V_{BD}$ to $+V_A$	0.3 V
	$+V_{BD}$	6 V
Digital inputs		-0.3 V to $+V_{DIG}$ + 0.3 V
Maximum junction temperature		165°C
Storage temperature range		–65°C to 150°C
Internal power dissipation		700 mW
Lead temperature (soldering, 1.6 mm from case 10 seconds)		260°C

(1) All voltage values are with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS

At T_A = -40°C to 85°C, f_S = 40 kHz, $+V_A$ = $+V_{BD}$ = 5 V or V_S = 5 V, and using internal reference and fixed resistors, unless otherwise specified.

PARAMETER		TEST CONDITIONS	ADS8513I			ADS8513IB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Resolution				16			16	Bits
ANALOG INPUT									
	Voltage ranges (see Table 1)								V
	Impedance								
	Capacitance			45			45		pF
THROUGHPUT SPEED									
	Conversion time	Acquire and convert			20			20	µs
	Complete cycle				25			25	
	Throughput rate		40			40			kHz
DC ACCURACY									
INL	Integral linearity error		-3		3	-1.5		1.5	LSB(1)
DNL	Differential linearity error		-2		2	-1		1	LSB
	No missing codes		15			16			Bits

(1) LSB means Least Significant Bit. One LSB for the ±10 V input range is 305 µV.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

At T_A = -40°C to 85°C, f_S = 40 kHz, $+V_A = +V_{BD}$ = 5 V or V_S = 5 V, and using internal reference and fixed resistors, unless otherwise specified.

PARAMETER		TEST CONDITIONS	ADS8513I			ADS8513IB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Transition noise(2)			0.8			0.8		LSB
	Gain Error			±0.2			±0.1		%
	Full scale error(3)(4)		-0.5		0.5	-0.25		0.25	%
	Full scale error drift			±7			±5		ppm/°C
	Full scale error(3)(4)	Ext. 2.5-V Ref	-0.5		0.5	-0.25		0.25	%
	Full scale error drift	Ext. 2.5-V Ref		±0.5			±0.5		ppm/°C
	Bipolar zero error(3)	Bipolar ranges	-10		10	-5		5	mV
	Bipolar zero error drift	Bipolar ranges		±0.5			±0.5		ppm/°C
	Unipolar zero error(3)	Unipolar ranges	-6		6	-6		6	mV
	Unipolar zero error drift	Unipolar ranges		±0.5			±0.5		ppm/°C
	Recovery time to rated accuracy from power down(5)	2.2-µF Capacitor to CAP		1			1		ms
	Power supply sensitivity ($V_{DIG} = V_{ANA} = V_S$)	+4.75 V < V_S < +5.25 V or +4.75 V < $+V_A$ < +5.25 V			±8			±8	LSB
AC ACCURACY									
SFDR	Spurious-free dynamic range	f_{IN} = 1 kHz, ±10 V	90	100		96	102		dB(6)
THD	Total harmonic distortion	f_{IN} = 1 kHz, ±10 V		-100	-90		-100	-96	dB
SINAD	Signal-to-(noise+distortion)	f_{IN} = 1 kHz, ±10 V	83	88		87	89.9		dB
		-60 dB Input		30			32		
SNR	Signal-to-noise	f_{IN} = 1 kHz, ±10 V	83	88		87	89.9		dB
	Usable bandwidth(7)			130			130		kHz
	Full-power bandwidth (-3 dB)			600			600		kHz
SAMPLING DYNAMICS									
	Aperture delay			40			40		ns
	Aperture jitter			20			20		ps
	Transient response	FS Step			5			5	µs
	Overvoltage recovery(8)			750			750		ns
REFERENCE									
	Internal reference voltage	No load	2.48	2.5	2.52	2.48	2.5	2.52	V
	Internal reference source current (must use external buffer)			1			1		µA
	Internal reference drift			8			8		ppm/°C
	External reference voltage range for specified linearity		2.3	2.5	2.7	2.3	2.5	2.7	V
	External reference current drain	External 2.5-V Ref			100			100	µA
DIGITAL INPUTS									
V_{IL}	Low-level input voltage		-0.3		+0.8	-0.3		+0.8	V
V_{IH}	High-level input voltage	$V_D = V_S$ or $V_D = +V_{BD}$	2.0		V_D +0.3 V	2.0		V_D +0.3 V	V
I_{IL}	Low-level input current	V_{IL} = 0 V			±10				µA
I_{IH}	High-level input current	V_{IH} = 5 V			±10				µA
DIGITAL OUTPUTS									
	Data format - Serial								
	Data coding - Binary 2's complement								

(2) Typical rms noise at worst case transitions.
(3) As measured with fixed resistors. Adjustable to zero with external potentiometer.
(4) Full scale error is the worst case of -Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error.
(5) This is the time delay after the ADS8513 is brought out of Power-Down mode until all internal settling occurs and the analog input is acquired to rated accuracy. A Convert command after this delay will yield accurate results.
(6) All specifications in dB are referred to a full-scale input.
(7) Usable bandwidth defined as full-scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60 dB.
(8) Recovers to specified performance after 2 x FS input overvoltage.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

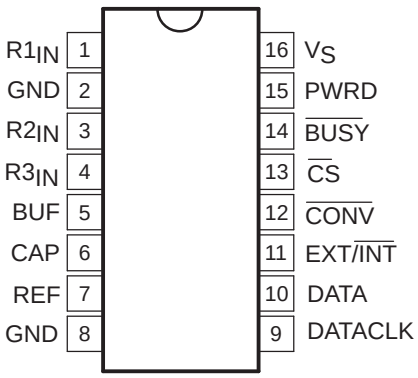
At T_A = -40°C to 85°C, f_S = 40 kHz, $+V_A$ = $+V_{BD}$ = 5 V or V_S = 5 V, and using internal reference and fixed resistors, unless otherwise specified.

PARAMETER		TEST CONDITIONS	ADS8513I			ADS8513IB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OL}	Low-level output voltage	I_{SINK} = 1.6 mA			0.4			0.4	V
V_{OH}	High-level output voltage	I_{SOURCE} = 500 µA	4			4			V
	Leakage Current	High-Z state, V_{OUT} = 0 V to V_S or $+V_{BD}$			±5			±5	µA
	Output capacitance	High-Z state			15			15	pF
DIGITAL TIMING									
	Bus access time	R_L = 3.3 kΩ, C_L = 50 pF			83			83	ns
	Bus relinquish time	R_L = 3.3 kΩ, C_L = 10 pF			83			83	ns
POWER SUPPLIES									
V_{BD}	Digital voltage	Must be ≤ $+V_A$	4.75	5	5.25	4.75	5	5.25	V
V_A or V_S	Analog voltage		4.75	5	5.25	4.75	5	5.25	V
I_{DIG}	Digital current			0.6			0.6		mA
I_{ANA}	Analog current			4.2			4.2		mA
	Power dissipation	V_S = 5 V or $+V_A$ = $+V_{BD}$ = 5 V, f_S = 40 kHz		24	32.5		24	32.5	mW
		PWRD and REFD high		50			50		µW
TEMPERATURE RANGE									
	Specified performance		-40		85	-40		85	°C
	Derated performance		-55		125	-55		125	°C
	Storage temperature		-65		150	-65		150	°C
SO	Thermal resistance (Θ_{JA})			46			46		°C/W

PRODUCT PREVIEW

DEVICE INFORMATION

SO (DW) PACKAGE
(TOP VIEW)



DEVICE INFORMATION (continued)

Terminal Functions

TERMINAL		DIGITAL I/O	DESCRIPTION
NAME	SO NO.		
$R1_{IN}$	1		Analog Input. See Table 1 and Table 3.
$R2_{IN}$	3		Analog Input. See Table 1 and Table 3.
$R3_{IN}$	4		Analog Input. See Table 1 and Table 3.
BUF	5		Reference buffer output. Connect to R1IN, R2IN, or R3IN as needed
CAP	6		Reference buffer compensationnode. Decouple to ground with a 1-µF tantalum capacitor in parallel with a 0.01-µF ceramic capacitor.
REF	7		Reference input/output. Outputs internal 2.5-V reference via a series 4-kΩ resisitor. Decouple this voltage with a 1-µF to 2.2-µF tantalum capacitor to ground. If an external reference voltage is applied to this pin, it will override the internal reference.
DGND	14		Digital ground
DATACLK	9	I/O	Data clock pin. With EXT/$\overline{INT}$ low, this pin is an output and provides the synchrnous clock for the serial data. The output is 3-stated when $\overline{CS}$ is high. With EXT/$\overline{INT}$ high, this pin is an input and the serial data clock must be provided externally.
DATA	10	O	Serial data output. The serial data is always the result of the last completed conversion and is synchronized to DATACLK. If DATACLK is from the internal clock (EXT/$\overline{INT}$ low), the serial data is valid on both the rising and falling edges of DATACLK. Data is 3-stated when $\overline{CS}$ is high.
EXT/$\overline{INT}$	11	I	External/Internal DATACLK pin. Selects the source of the synchronous clock for serial data. if high, the clock must be provided externally. If low, the clock is derived from the internal conversion clock. Note that the clock used to time the conversion is always internal regardless of the status of EXT/$\overline{INT}$.
$\overline{CONV}$	12		Convert input. A faaling edge on this input puts the internal sample/hold into the hold state and starts a conversion regardless of the state of $\overline{CS}$. If a conversion is already in progress, the falling edge is ignored. If EXT/$\overline{INT}$ is low, data from the previous conversion will be serially transmitted during the current conversion.
$\overline{CS}$	13	I	Chip select. This input 3-states all outputs when high and enables all outputs when low. This includes DATA, $\overline{BUSY}$, and DATACLK (when EXT/$\overline{INT}$ is low). Note that a falling edge on $\overline{CONV}$ will initiate a conversion even when $\overline{CS}$ is high.
$\overline{BUSY}$	14	O	Busy output. When a conversion is started, $\overline{BUSY}$ goes low and remains low throughout the conversion. If EXT/$\overline{INT}$ is low, data is serially transmitted while $\overline{BUSY}$ is low. $\overline{BUSY}$ is 3-stated when $\overline{CS}$ is high.
PWRD	15	I	Power down input. When high, the majority of the ADS851 is placed in a low power mode and power consumption is significantly reduced. $\overline{CONV}$ must be taken low prior to PWRD going low in order to achieve the lowest power consumption. The time required for the ADS8513 to return to normal operation after power down depends on a number of factors. Consult the POWER DOWN section for more information.
GND	2, 8		Ground.
V_S	16		+5-V Supply input. For best performance, decouple to ground with a 0.1-µF ceramic capacitor in parallel with a 10-µF tantalum capacitor.

PRODUCT PREVIEW

Table 1. Input Ranges

ANALOG INPUT RANGE	CONNECT $R1_{IN}$TO	CONNECT $R2_{IN}$ TO	CONNECT $R3_{IN}$ TO	INPUT IMPEDANCE
±10 V	V_{IN}	BUF	GND	45.7 kΩ
0.3125V to 2.8125 V	V_{IN}	V_{IN}	V_{IN}	> 10,000
±5 V	GND	BUF	V_{IN}	26.7 kΩ
0 V to 10 V	BUF	GND	V_{IN}	26.7 kΩ
0 V to 4 V	BUF	V_{IN}	GND	21.3
±3.33 V	V_{IN}	BUF	V_{IN}	21.3
0.5 V to 4.5 V	GND	V_{IN}	GND	21.3

TYPICAL CHARACTERISTICS

BASIC OPERATION

INTERNAL DATACLK

Figure 1 shows a basic circuit to operate the ADS8513 with a ±10-V input range. To begin a conversion and serial transmission of the results from the previous conversion, a falling edge must be provided to the $\overline{CONV}$ input. $\overline{BUSY}$ will go LOW indicating that a conversion has started and will stay LOW until the conversion is complete. During the conversion, the results of the previous conversion will be transmitted via DATA while DATACLK provides the synchronous clock for the serial data. The data format is 16-bit, Binary Two's Complement, and MSB first. Each data bit is valid on both the rising and falling edge of DATACLK. $\overline{BUSY}$ is LOW during the entire serial transmission and can be used as a frame synchronization signal.

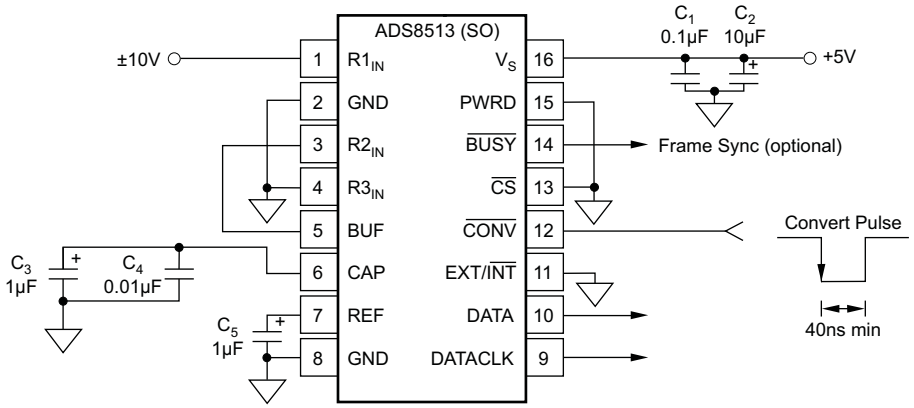
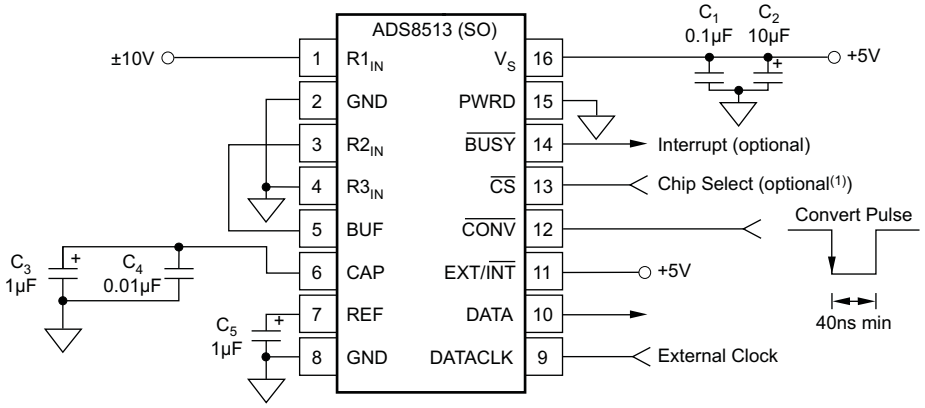


Figure 1. Basis Operation, ±10-V Input Range, Internal DATACLK

EXTERNAL DATACLK

Figure 2 shows a basic circuit to operate the ADS8513 with a ±10-V input range. To begin a conversion, a falling edge must be provided to the $\overline{CONV}$ input. $\overline{BUSY}$ will go LOW indicating that a conversion has started and will stay LOW until the conversion is complete. Just prior to $\overline{BUSY}$ rising near the end of the conversion, the internal working register holding the conversion result will be transferred to the internal shift register.

The internal shift register is clocked via the DATACLK input. The recommended method of reading the conversion result is to provide the serial clock after the conversion has completed. See External DATACLK under the Reading Data section of this data sheet for more information.



NOTE: (1) Tie $\overline{CS}$ to GND if the outputs will always be active.

Figure 2. Basic Operation, ±10-V Input Range, External DATACLK

BASIC OPERATION (continued)

STARTING A CONVERSION

If a conversion is not currently in progress, a falling edge on the $\overline{CONV}$ input places the sample and hold into the hold mode and begins a conversion, as shown in Figure 3 and with the timing given in Table 2. During the conversion, the $\overline{CONV}$ input is ignored. Starting a conversion does not depend on the state of $\overline{CS}$. A conversion can be started once every 25 µs (40-kHz maximum conversion rate). There is no minimum conversion rate.

Even though the $\overline{CONV}$ input is ignored while a conversion is in progress, this input should be held static during the conversion period. Transitions on this digital input can easily couple into sensitive analog portions of the converter, adversely affecting the conversion results (see the Sensitivity to External Digital Signals section of this data sheet for more information).

Ideally, the $\overline{CONV}$ input should go LOW and remain LOW throughout the conversion. It should return HIGH sometime after $\overline{BUSY}$ goes HIGH. In addition, it should be HIGH prior to the start of the next conversion for a minimum time period given by t_5. This will ensure that the digital transition on the $\overline{CONV}$ input will not affect the signal that is acquired for the next conversion.

An acceptable alternative is to return the $\overline{CONV}$ input HIGH as soon after the start of the conversion as possible. For example, a negative going pulse 100ns wide would make a good $\overline{CONV}$ input signal. It is strongly recommended that from time t_2 after the start of a conversion until $\overline{BUSY}$ rises, the $\overline{CONV}$ input should be held static (either HIGH or LOW). During this time, the converter is more sensitive to external noise.

Table 2. Conversion and Data Timing, T_A = –40°C to 85°C

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Conversion Plus Acquisition Time			25	µs
t_2	$\overline{CONV}$ LOW to All Digital Inputs Stable			19	µs
t_3	$\overline{CONV}$ LOW to Initiate a Conversion	0.04		12	µs
t_4	$\overline{BUSY}$ Rising to Any Digital Input Active	5			ns
t_5	$\overline{CONV}$ HIGH Prior to Start of Conversion ($\overline{CONV}$ high time)	15			ns
t_6	$\overline{BUSY}$ LOW		18	20	µs
t_7	$\overline{CONV}$ LOW to $\overline{BUSY}$ LOW		12	20	ns
t_8	Aperture Delay ($\overline{CONV}$ falling edge to actual conversion start)		5		ns
t_9	Conversion Time		18	20	µs
t_{10}	Conversion Complete to $\overline{BUSY}$ Rising		90		ns
t_{11}	Acquisition Time		5		µs
t_{12}	$\overline{CONV}$ LOW to Rising Edge of First Internal DATACLK		0.27		µs
t_{13}	Internal DATACLK HIGH	300	410	425	ns
t_{14}	Internal DATACLK LOW	300	410	425	ns
t_{15}	Internal DATACLK Period	0.6	0.82	0.85	µs
t_{16}	DATA Valid to Internal DATACLK Rising	15	35		ns
t_{17}	Internal DATACLK Falling to DATA Not Valid	22	37		ns
t_{18}	Falling Edge of Last DATACLK to $\overline{BUSY}$ Rising			1	µs
t_{19}	External DATACLK Rising to DATA Not Valid	4	14		ns
t_{20}	External DATACLK Rising to DATA Valid	2	12	20	ns
t_{21}	External DATACLK HIGH	15			ns
t_{22}	External DATACLK LOW	15			ns
t_{23}	External DATACLK Period	35			ns
t_{24}	$\overline{CONV}$ LOW to External DATACLK Active	15			ns
t_{25}	External DATACLK LOW or $\overline{CS}$ HIGH to $\overline{BUSY}$ Rising			1	µs
t_{26}	$\overline{CS}$ LOW to Digital Outputs Enabled	15			ns
t_{27}	$\overline{CS}$ HIGH to Digital Outputs Disabled	15			ns

PRODUCT PREVIEW

Table 3. Output Codes and Ideal Input Voltages

DESCRIPTION	ANALOG INPUT		DIGITAL OUTPUT	
			BINARY 2's COMPLEMENT	
			BINARY CODE	HEX CODE
Full-scale range	±10	0.5 V to 4.5 V		
Least significant bit (LSB)	305 µV	61 µV		
+Full-Scale (FS - 1LSB)	9.999695 V	4.499939 V	0111 1111 1111 1111	7FFF
Midscale	0 V	2.5 V	0000 0000 0000 0000	0000
One LSB Below Midscale	-305 µV	2.499939 µV	1111 1111 1111 1111	FFFF
-Full-Scale-	-10 V	0.5 V	1000 0000 0000 0000	8000

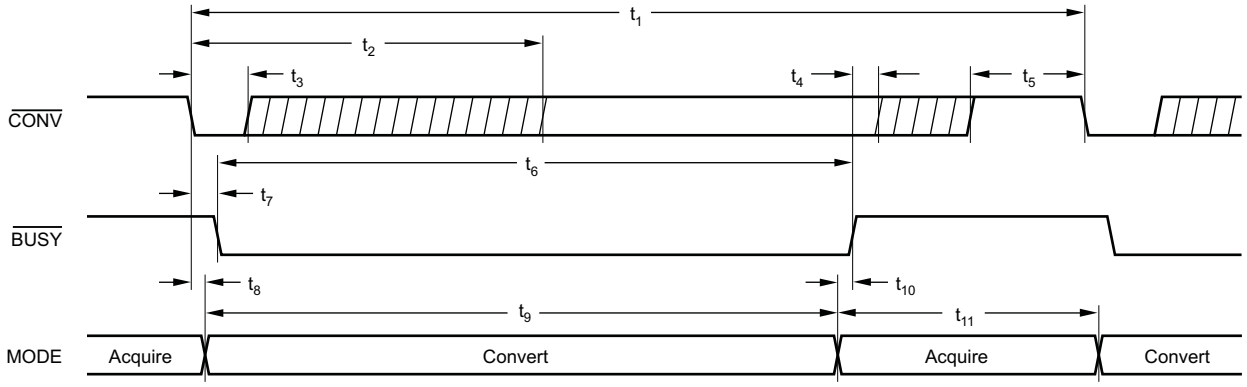


Figure 3. Basic Conversion Timing

PRODUCT PREVIEW

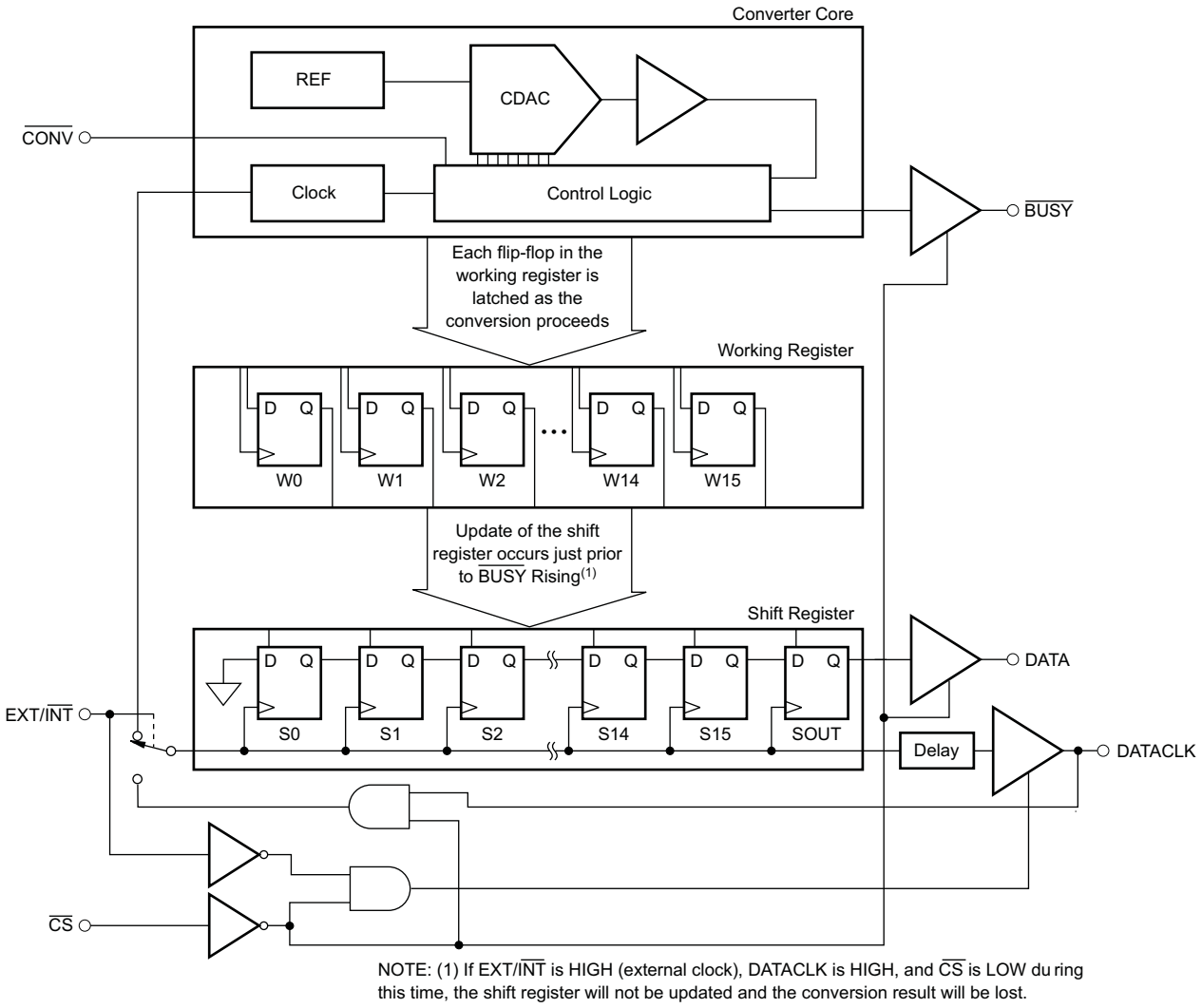
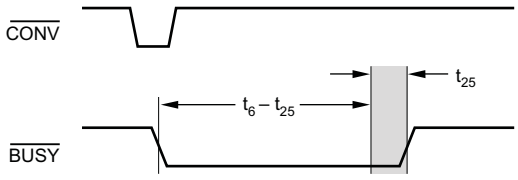


Figure 4. Block Diagram of the ADS8513 Digital Inputs and Outputs



NOTE: Update of the internal shift register occurs in the shaded region. If EXT/INT is HIGH, then DATACLK must be LOW or CS must be HIGH during this time.

Figure 5. Timing of the Shift Register Update

READING DATA

The ADS8513 digital output is in Binary Two's Complement (BTC) format. Table 3 shows the relationship between the digital output word and the analog input voltage under ideal conditions.

PRODUCT PREVIEW

Figure 5 shows the relationship between the various digital inputs, digital outputs, and internal logic of the ADS8513. Figure 6 shows when the internal shift register of the ADS8513 is updated and how this relates to a single conversion cycle. Together, these two figures point out a very important aspect of the ADS8513: the conversion result is not available until after the conversion is complete. The implications of this are discussed in the following sections.

INTERNAL DATACLK

With EXT/$\overline{INT}$ tied LOW, the result from conversion 'n' is serially transmitted during conversion 'n+1', as shown in Figure 4 and with the timing given in Table 2. Serial transmission of data occurs only during a conversion. When a transmission is not in progress, DATA and DATACLK are LOW.

During the conversion, the results of the previous conversion will be transmitted via DATA, while DATACLK provides the synchronous clock for the serial data. The data format is 16-bit, Binary Two's Complement, and MSB first. Each data bit is valid on both the rising and falling edges of DATACLK. $\overline{BUSY}$ is LOW during the entire serial transmission and can be used as a frame synchronization signal.

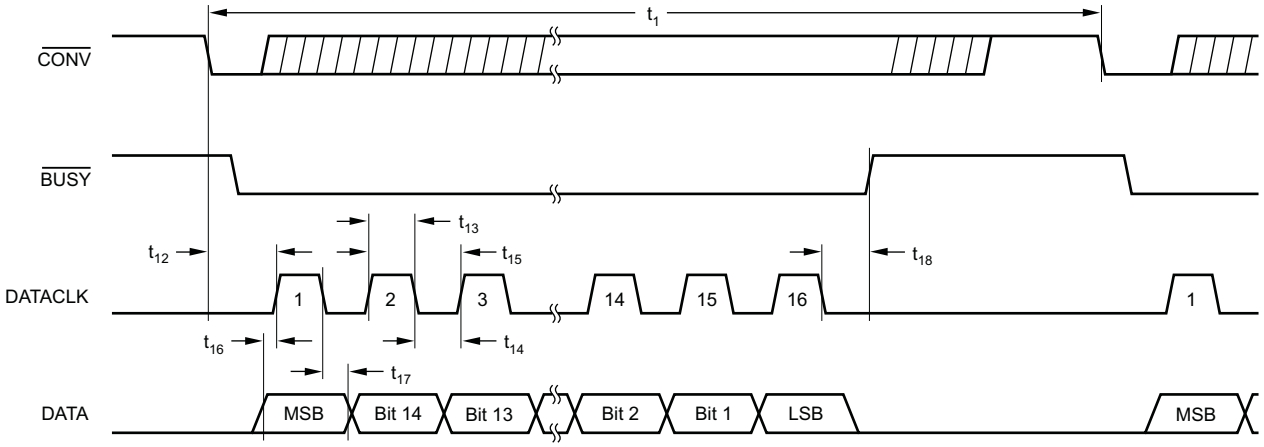


Figure 6. Serial Data Timing, Internal Clock (EXT/$\overline{INT}$ and $\overline{CS}$ Low)

EXTERNAL DATACLK

With EXT/$\overline{INT}$ tied HIGH, the result from conversion 'n' is clocked out after the conversion has completed, during the next conversion ('n+1'), or a combination of these two. Figure 7 shows the case of reading the conversion result after the conversion is complete. Figure 8 describes reading the result during the next conversion. Figure 9 combines the important aspects of Figure 7 and Figure 8 as to reading part of the result after the conversion is complete and the remainder during the next conversion.

The serial transmission of the conversion result is initiated by a rising edge on DATACLK. The data format is 16-bit, Binary Two's Complement, and MSB first. Each data bit is valid on the falling edge of DATACLK. In some cases, it might be possible to use the rising edge of the DATACLK signal. However, one extra clock period (not shown in Figure 7, Figure 8), and Figure 9 is needed for the final bit.

The external DATACLK signal must be LOW or $\overline{CS}$ must be HIGH prior to $\overline{BUSY}$ rising (see time t_{25} in Figure 8 and Figure 9). If this is not observed during this time, the output shift register of the ADS8513 will not be updated with the conversion result. Instead, the previous contents of the shift register will remain and the new result will be lost.

Before reading the next three paragraphs, consult the Sensitivity to External Digital Signals section of this data sheet. This will explain many of the concerns regarding how and when to apply the external DATACLK signal.

EXTERNAL DATACLK ACTIVE AFTER THE CONVERSION

The preferred method of obtaining the conversion result is to provide the DATACLK signal after the conversion has been completed and before the next conversion starts—as shown in Figure 7. Note that the DATACLK signal should be static before the start of the next conversion. If this is not observed, the DATACLK signal could affect the voltage that is acquired.

PRODUCT PREVIEW

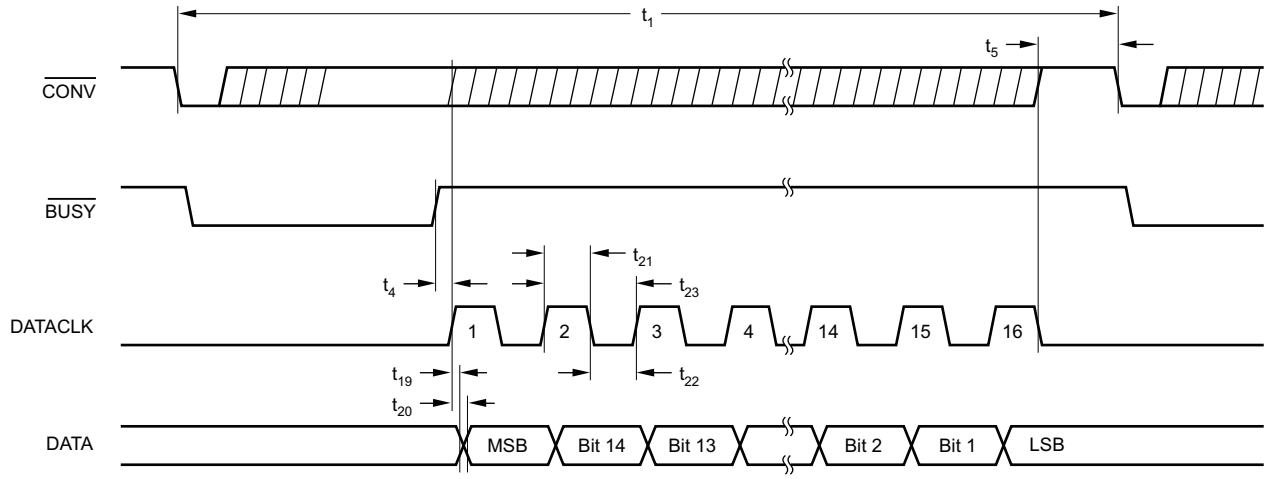


Figure 7. Serial Data Timing, External Clock, Clocking After the Conversion Completes (EXT/$\overline{INT}$ High, $\overline{CS}$ Low)

EXTERNAL DATACLK ACTIVE DURING THE NEXT CONVERSION

Another method of obtaining the conversion result is shown in Figure 8. Since the output shift register is not updated until the end of the conversion, the previous result remains valid during the next conversion. If a fast clock (≥ 2MHz) can be provided to the ADS8513, the result can be read during time t_2. During this time, the noise from the DATACLK signal is less likely to affect the conversion result.

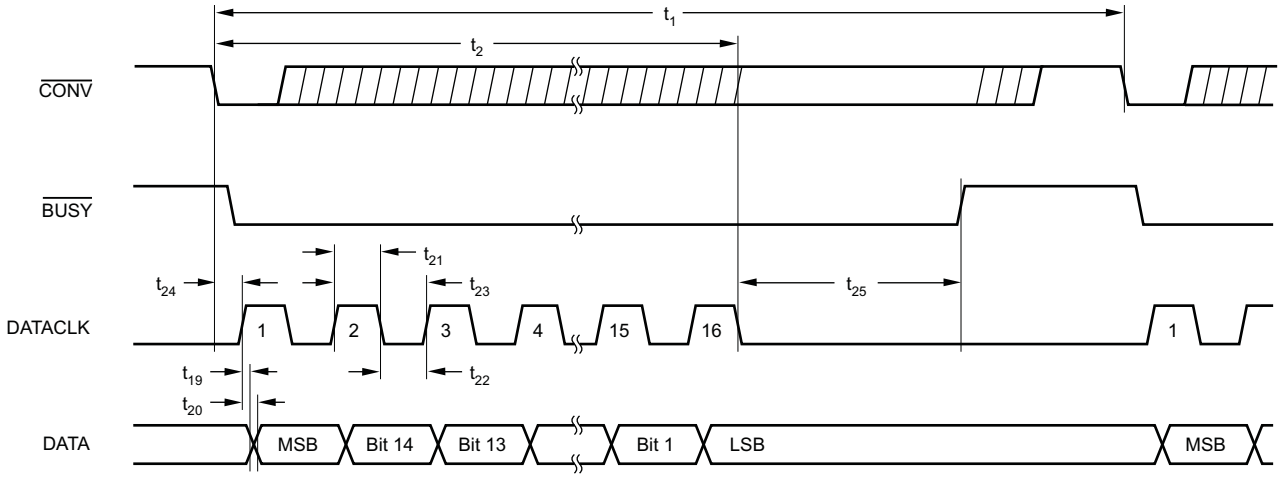


Figure 8. Serial Data Timing, External Clock, Clocking During the Next Conversion (EXT/$\overline{INT}$ High, $\overline{CS}$ Low)

EXTERNAL DATACLK ACTIVE AFTER THE CONVERSION AND DURING THE NEXT CONVERSION

Figure 9 shows a method that is a hybrid of the two previous approaches. This method works very well for microcontrollers that do serial transfers 8 bits at a time and for slower microcontrollers. For example, if the fastest serial clock that the microcontroller can produce is 1 µs, the approach shown in Figure 7 would result in a diminished throughput (26-kHz maximum conversion rate). The method described in Figure 8 could not be used without risk of affecting the conversion result (the clock would have to be active after time t_2). The approach in Figure 9 results in an improved throughput rate (33 kHz maximum with a 1-µs clock) and DATACLK is not active after time t_2.

PRODUCT PREVIEW

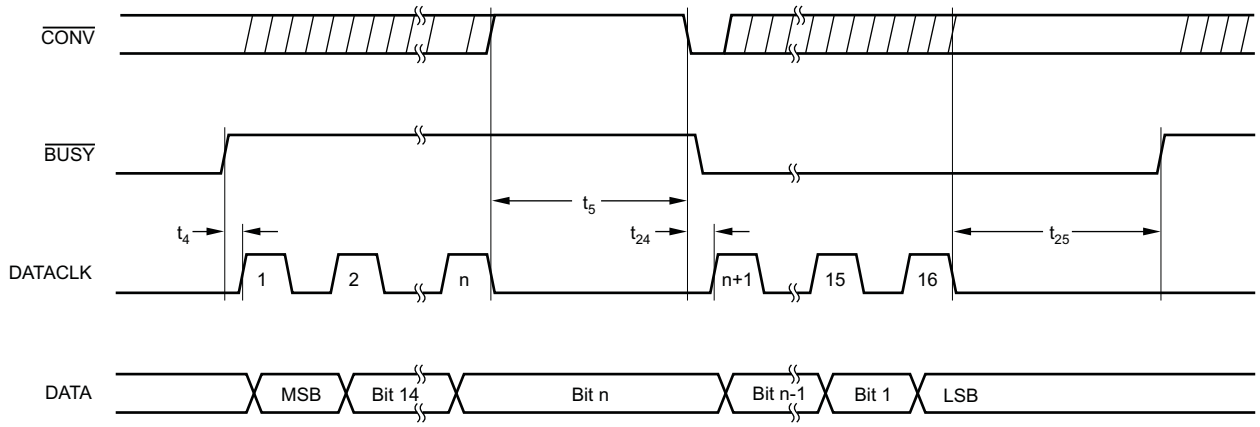
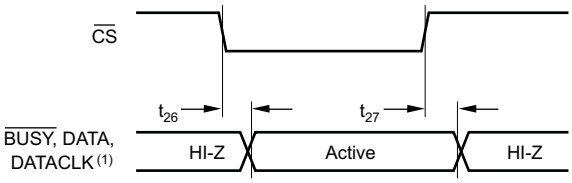


Figure 9. Serial Data Timing, External Clock, Clocking After the Conversion Completes and During the Next Conversion (EXT/INT High, CS Low)

CHIP SELECT

The CS input allows the digital outputs of the ADS8513 to be disabled and gates the external DATACLK signal when EXT/INT is HIGH. See Figure 10 for the enable and disable time associated with CS and Figure 4 for a block diagram of the ADS8513's logic. The digital outputs can be disabled at any time.

Note that a conversion is initiated on the falling edge of CONV even if CS is HIGH. If the EXT/INT input is LOW (internal DATACLK) and CS is HIGH during the entire conversion, the previous conversion result will be lost (the serial transmission occurs but DATA and DATACLK are disabled).



NOTE: (1) DATACLK is an output only when EXT/INT is LOW.

Figure 10. Enable and Disable Timing for Digital Outputs

ANALOG INPUT

The ADS8513 offers a number of input ranges. This is accomplished by connecting the three input resistors to either the analog input (VIN), to ground (GND), or to the 2.5-V reference buffer output (BUF). Table 1 shows the input ranges that are typically used in most data acquisition applications. These ranges are all specified to meet the specifications given in the Specifications table. Table 4contains a complete list of ideal input ranges, associated input connections, and comments regarding the range.

Table 4. Complete list of Ideal Input Ranges

ANALOG INPUT RANGE (V)	CONNECT R1IN TO	CONNECT R2IN TO	CONNECT R3IN TO	INPUT IMPEDANCE (kΩ)	COMMENT
0.3125 to 2.8125	VIN	VIN	VIN	> 10,000	Specified offset and gain
–0.417 to 2.916	VIN	VIN	BUF	26.7	VIN cannot go below GND – 0.3V
0.417 to 3.750	VIN	VIN	GND	26.7	Offset and gain not specified
±3.333	VIN	BUF	VIN	21.3	Specified offset and gain
–15 to 5	VIN	BUF	BUF	45.7	Offset and gain not specified

PRODUCT PREVIEW

ANALOG INPUT (continued)

Table 4. Complete list of Ideal Input Ranges (continued)

ANALOG INPUT RANGE (V)	CONNECT R1IN TO	CONNECT R2IN TO	CONNECT R3IN TO	INPUT IMPEDANCE (kΩ)	COMMENT
±10	VIN	BUF	GND	45.7	Specified offset and gain
0.833 to 7.5	VIN	GND	VIN	21.3	Offset and gain not specified
–2.5 to 17.5	VIN	GND	BUF	45.7	Exceeds absolute maximum VIN
2.5 to 22.5	VIN	GND	GND	45.7	Exceeds absolute maximum VIN
0 to 2.857	BUF	VIN	VIN	45.7	Offset and gain not specified
–1 to 3	BUF	VIN	BUF	21.3	VIN cannot go below GND – 0.3V
0 to 4	BUF	VIN	GND	21.3	Specified offset and gain
–6.25 to 3.75	BUF	BUF	VIN	26.7	Offset and gain not specified
0 to 10	BUF	GND	VIN	26.7	Specified offset and gain
0.357 to 3.214	GND	VIN	VIN	45.7	Offset and gain not specified
–0.5 to 3.5	GND	VIN	BUF	21.3	VIN cannot go below GND – 0.3V
0.5 to 4.5	GND	VIN	GND	21.3	Specified offset and gain
±5	GND	BUF	VIN	26.7	Specified offset and gain
1.25 to 11.25	GND	GND	VIN	26.7	Offset and gain not specified

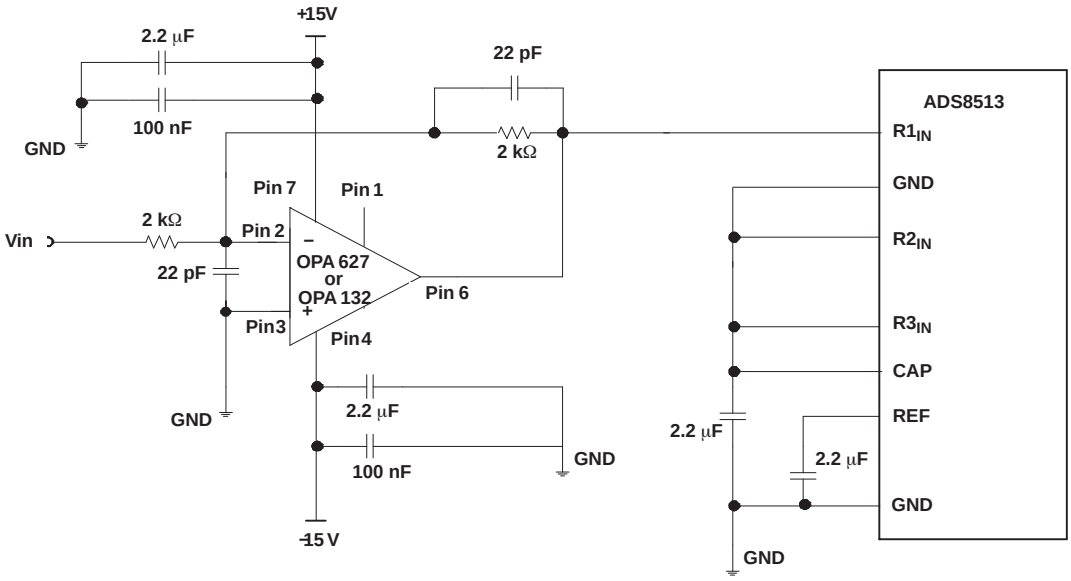


Figure 11. Typical Driving Circuit (±10 V, No Trim)

The input impedance results from the various connections and the internal resistor values (refer to the block diagram on the front page of this data sheet). The internal resistor values are typical and can change by ±30%, due to process variations. However, the ratio matching of the resistors is considerably better than this. Thus, the input range will vary only a few tenths of a percent from part to part, while the input impedance can vary up to ±30%.

The Specifications table contains the maximum limits for the variation of the analog input range, but only for those ranges where the comment field shows that the offset and gain are specified (this includes all the ranges listed in Table 1). For the other ranges, the offset and gain are not tested and are not specified.

Five of the input ranges in Table 4 are not recommended for general use. The upper-end of the –2.5V to +17.5V range and +2.5V to +22.5V range exceed the absolute maximum analog input voltage. These ranges can still be used as long as the input voltage remains under the absolute maximum, but this will moderately to significantly reduce the full-scale range of the converter.

PRODUCT PREVIEW

Likewise, three of the input ranges involve the connection at R2IN being driven below GND. This input has a reverse biased ESD protection diode connection to ground. If R2IN is taken below GND – 0.3V, this diode will be forward-biased and will clamp the negative input at –0.4V to –0.7V, depending on the temperature. Since the negative full-scale value of these input ranges exceed –0.4V, they are not recommended.

Note that Table 4 assumes that the voltage at the REF pin is +2.5V. This is true if the internal reference is being used or if the external reference is +2.5V. Other reference voltages will change the values inTable 4.

HIGH IMPEDANCE MODE

When R1IN, R2IN, and R3IN are connected to the analog input, the input range of the ADS8513 is 0.3125V to 2.8125V and the input impedance is greater than 10MΩ. This input range can be used to connect the ADS8513 directly to a wide variety of sensors. Figure 12 shows the impedance of the sensor versus the change in ILE and DLE of the ADS8513. The performance of the ADS8513 can be improved for higher sensor impedance by allowing more time for acquisition. For example, 10 s of acquisition time will approximately double sensor impedance for the same ILE/DLE performance.

The input impedance and capacitance of the ADS8513 are very stable with temperature. Assuming that this is true of the sensor as well, the graph shown in Figure 12 will vary less than a few percent over the ensured temperature range of the ADS8513. If the sensor impedance varies significantly with temperature, the worst-case impedance should be used.

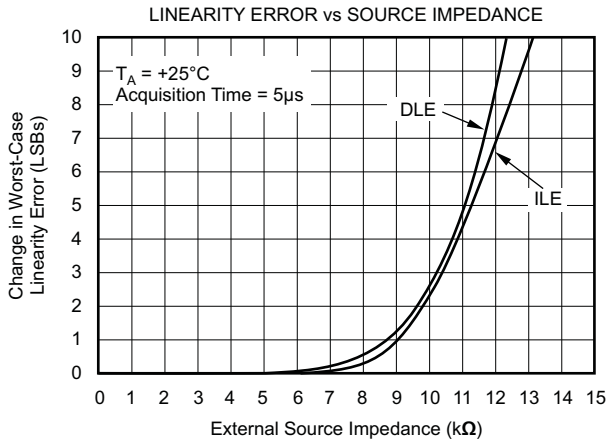


Figure 12. Linearity Error vs Source Impedance in the High Impedance Mode (R1IN = R2IN = R3IN = VIN)

DRIVING THE ADS8513 ANALOG INPUT

In general, any reasonably fast, high-quality operational or instrumentation amplifier can be used to drive the ADS8513 input. When the converter enters the acquisition mode, there is some charge injection from the converter input to the amplifier output. This can result in inadequate settling time with slower amplifiers. Be very careful with single-supply amplifiers, particularly if their output will be required to swing very close to the supply rails.

In addition, be careful in regards to the amplifier linearity. The outputs of single-supply and rail-to-rail amplifiers can saturate as they approach the supply rails. Rather than the amplifier transfer function being a straight line, the curve can become severely 'S' shaped. Also, watch for the point where the amplifier switches from sourcing current to sinking current. For some amplifiers, the transfer function can be noticeably discontinuous at this point, causing a significant change in the output voltage for a much smaller change on the input.

Texas Instruments manufactures a wide variety of operational and instrumentation amplifiers that can be used to drive the input of the ADS8513. These include the OPA627, OPA132, and INA110.

REFERENCE

The ADS8513 can be operated with its internal 2.5-V reference or an external reference. By applying an external reference voltage to the REF pin, the internal reference voltage is overdriven. The voltage at the REF input is internally buffered by a unity gain buffer. The output of this buffer is present at the BUF and CAP pins.

REF

The REF pin is the output of the internal 2.5-V reference or the input for an external reference. A 1-µF to 2.2-µF tantulum capacitor should be connected between this pin and ground. The capacitor should be placed as close to the ADS8513 as possible.

When using the internal reference, the REF pin should not be connected to any type of significant load. An external load will cause a voltage drop across the internal 4-kΩ resistor that is in series with the internal reference. Even a 40-MΩ external load to ground will cause a decrease in the full-scale range of the converter by 6 LSBs.

The range for the external reference is 2.3V to 2.7V. The voltage on REF determines the full-scale range of the converter and the corresponding LSB size. Increasing the reference voltage will increase the LSB size in relation to the internal noise sources which, in turn, can improve signal-tonoise ratio. Likewise, decreasing the reference voltage will reduce the LSB size and signal-to-noise ratio.

CAP

The CAP pin is used to compensate the internal reference buffer. A 1-µF tantalum capacitor in parallel with a 0.01-µF ceramic capacitor should be connected between this pin and ground, with the ceramic capacitor placed as close to the ADS8513 as possible. The total value of the capacitance on the CAP pin is critical to optimum performance of the ADS8513. A value larger than 2.0 µF could overcompensate the buffer while a value lower than 0.5 µF may not provide adequate compensation. The ESR (equivalent series resistance) of these compensation capacitors is also critical. Keep the total ESR under 3Ω. See the Typical Characteristic curve, |Worst-Case INL| vs ESR of Reference Buffer Compensation Capacitor, for how the worst-case INL is affected by ESR.

BUF

The voltage on the BUF pin is the output of the internal reference buffer. This pin is used to provide +2.5 V to the analog input or inputs for the various input configurations. The BUF output can provide up to 1 mA of current to an external load. The load should be constant as a variable load could affect the conversion result by modulating the BUF voltage. Also note that the BUF output will show significant glitches as each bit decision is made during a conversion. Between conversions, the BUF output is quiet.

PRODUCT PREVIEW

POWER DOWN

The ADS8513 has a power-down mode that is activated by taking $\overline{\text{CONV}}$ LOW and then PWRD HIGH. This will power down all of the analog circuitry including the reference, reducing power dissipation to under 50 µW. To exit the power-down mode, $\overline{\text{CONV}}$ is taken HIGH and then PWRD is taken LOW. Note that a conversion will be initiated if PWRD is taken HIGH while $\overline{\text{CONV}}$ is LOW.

While in the power-down mode, the voltage on the capacitors connected to CAP and REF will begin to leak off. The voltage on the CAP capacitor leaks off much more rapidly than on the REF capacitor (the REF input of the ADS8513 becomes high-impedance when PWRD is HIGH—this is not true for the CAP input). When the power-down mode is exited, these capacitors must be allowed to recharge and settle to a 16-bit level. Figure 13 shows the amount of time typically required to obtain a valid 16-bit result based on the amount of time spent in power down (at room temperature). This figure assumes that the total capacitance on the CAP pin is 1.01 µF.

Figure 14 provides a circuit which can significantly reduce the power up time if the power down time will be fairly brief (a few seconds or less). A low on-resistance MOSFET is used to disconnect the capacitance on the CAP pin from the leakage paths internal to the ADS8513. This allows the capacitors to retain their charge for a much longer period of time, reducing the time required to recharge them at power up. With this circuit, the power-down time can be extended to tens or hundreds of milliseconds with almost instantaneous power up.

POWER DOWN (continued)

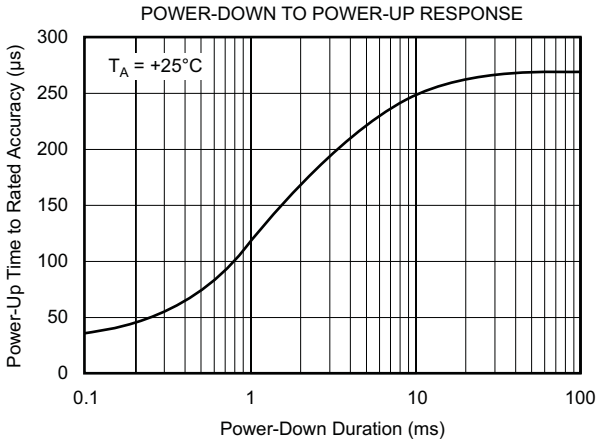


Figure 13. Power-Down to Power-Up Response

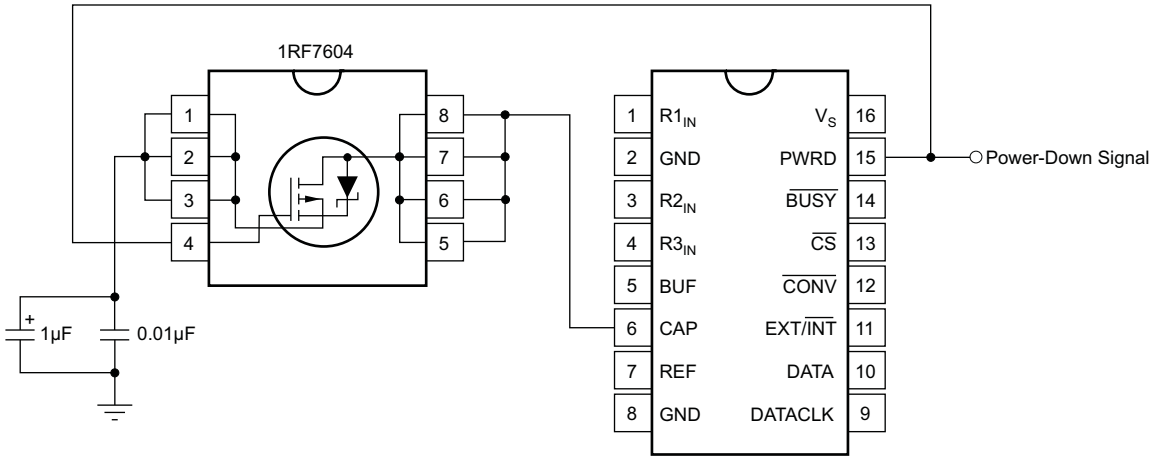


Figure 14. Improved Power-Up Response Circuit

LAYOUT

POWER FOR TSSOP-20 PACKAGE

For optimum performance, tie the analog and digital power pins to the same +5-V power supply and tie the analog and digital grounds together. As noted in the electrical characteristics, the ADS8507 uses 90% of its power for the analog circuitry. The ADS8507 should be considered as an analog component.

The +5-V power for the A/D converter should be separate from the +5 V used for the system's digital logic. Connecting $+V_{BD}$ directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5-V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12-V or +15-V supplies are present, a simple +5-V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both $+V_{BD}$ and $+V_A$ should be tied to the same +5-V source.

GROUNDING

Two types of ground pins are present on the TSSOP package ADS8507. DGND is the digital supply ground. AGND is the analog supply ground.

LAYOUT (continued)

All the ground pins of the A/D converter should be tied to an analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the *system* ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The amount of charge injection due to the sampling FET switch on the ADS8507 is approximately 5% to 10% of the amount on similar A/D converters with the charge redistribution digital-to-analog converter (DAC) CDAC architecture. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the drive capability on the signal conditioning preceding the A/D converter. Any op amp sufficient for the signal in an application will be sufficient to drive the ADS8507.

The resistive front end of the ADS8507 also provides a specified ±25-V overvoltage protection. In most cases, this eliminates the need for external over-voltage protection circuitry.

SENSITIVITY TO EXTERNAL DIGITAL SIGNALS

All successive approximation register-based A/D converters are sensitive to external sources of noise. The reason for this will be explained in the following paragraphs. For the ADS8513 and similar A/D converters, this noise most often originates due to the transition of external digital signals. While digital signals that run near the converter can be the source of the noise, the biggest problem occurs with the digital inputs to the converter itself.

In many cases, the system designer may not be aware that there is a problem or a potential for a problem. For a 12-bit system, these problems typically occur at the least significant bits and only at certain places in the converter's transfer function. For a 16-bit converter, the problem can be much easier to spot.

For example, the timing diagram in Figure 3 shows that the $\overline{\text{CONV}}$ signal should return HIGH sometime during time t_2. In fact, the $\overline{\text{CONV}}$ signal can return HIGH at any time during the conversion. However, after time t_2, the transition of the $\overline{\text{CONV}}$ signal has the potential of creating a good deal of noise on the ADS8513 die. If this transition occurs at just precisely the wrong time, the conversion results could be affected. In a similar manner, transitions on the DATACLK input could affect the conversion result.

For the ADS8513, there are 16 separate bit decisions which are made during the conversion. The most significant bit decision is made first, proceeding to the least significant bit at the end of the conversion. Each bit decision involves the assumption that the bit being tested should be set. This is combined with the result that has been achieved so far. The converter compares this combined result with the actual input voltage. If the combined result is too high, the bit is cleared. If the result is equal to or lower than the actual input voltage, the bit remains HIGH. This is why the basic architecture is referred to as successive approximation register (SAR).

If the result so far is getting very close to the actual input voltage, then the comparison involves two voltages which are very close together. The ADS8513 has been designed so that the internal noise sources are at a minimum just prior to the comparator result being latched. However, if an external digital signal transitions at this time, a great deal of noise will be coupled into the sensitive analog section of the ADS8513. Even if this noise produces a difference between the two voltages of only 2 mV, the conversion result will be off by 52 counts or least significant bits (LSBs). (The internal LSB size of the ADS8513 is 38 µV regardless of the input range.)

Once a digital transition has caused the comparator to make a wrong bit decision, the decision cannot be corrected (unless some type of error correction is employed). All subsequent bit decisions will then be wrong. Figure 15 shows a successive approximation process that has gone wrong. The dashed line represents what the correct bit decisions should have been. The solid line represents the actual result of the conversion.

Keep in mind that the time period when the comparator is most sensitive to noise is fairly small. Also, the peak portion of the noise event produced by a digital transition is fairly brief, as most digital signals transition in a few nanoseconds. The subsequent noise may last for a period of time longer than this and may induce further effects which require a longer settling time. However, in general, the event is over within a few tens of nanoseconds.

PRODUCT PREVIEW

LAYOUT (continued)

For the ADS8513, error correction is done when the tenth bit is decided. During this bit decision, it is possible to correct limited errors that may have occurred during previous bit decisions. However, after the tenth bit, no such correction is possible. Note that for the timing diagrams shown in Figure 3, Figure 6, Figure 7, Figure 8, and Figure 9 all external digital signals should remain static from 8 µs after the start of a conversion until $\overline{BUSY}$ rises. The tenth bit is decided approximately 10 µs to 11 µs into the conversion.

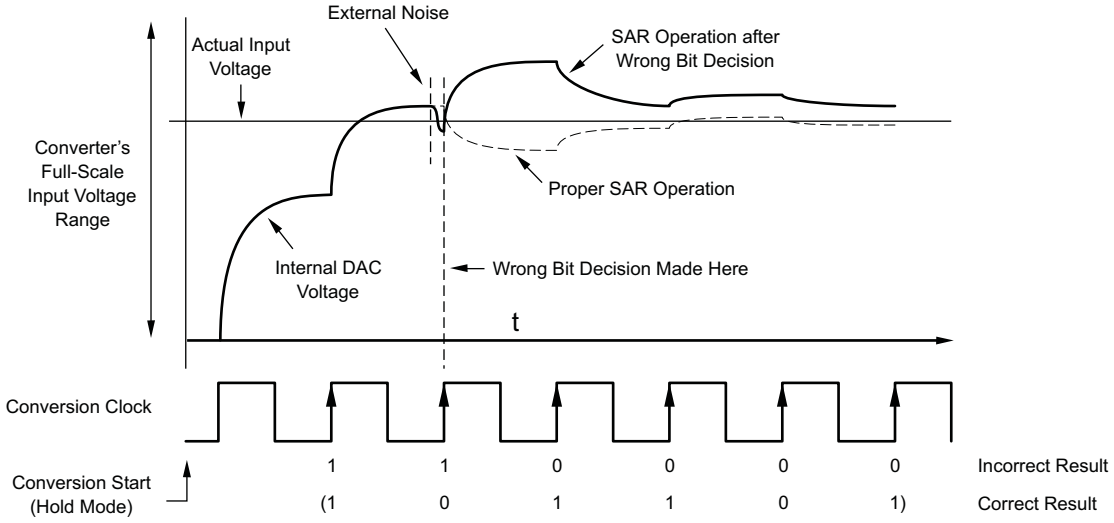


Figure 15. SAR Operation When External Noise Affects the Conversion

APPLICATION INFORMATION

TRANSITION NOISE

Apply a DC input to the ADS8513 and initiate 1000 conversions. The digital output of the converter varies in output codes due to the internal noise of the ADS8513. This is true for all 16-bit SAR converters. The transition noise specification found in the electrical characteristics section is a statistical figure which represents the one sigma limit or rms value of these output codes.

Using a histogram to plot the output codes, the distribution should appear bell-shaped with the peak of the bell curve representing the nominal output code for the input voltage value. The ±1σ, ±2σ, and ±3σ distributions represent 68.3%, 95.5%, and 99.7% of all codes. Multiplying TN by 6 yields the ±3σ distribution or 99.7% of all codes. Statistically, up to 3 codes could fall outside the 5 code distribution when executing 1000 conversions. The ADS8513 has a TN of 0.8 LSBs which yields 5 output codes for a ±3σ distribution. Figure 16 and Figure 17 show 1000 and 10000 conversion histogram results.

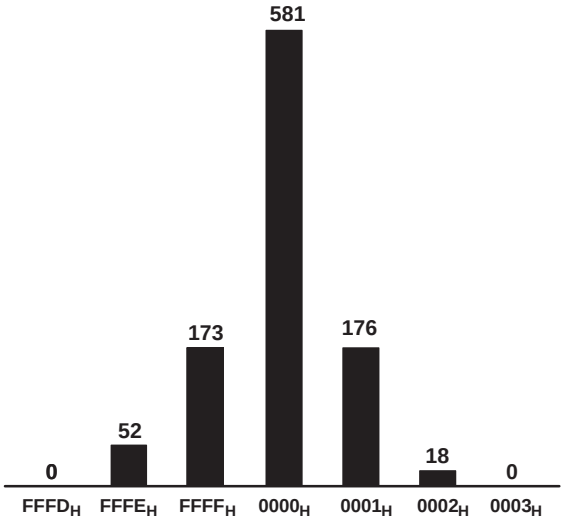


Figure 16. Histogram of 1000 Conversions With Input Grounded

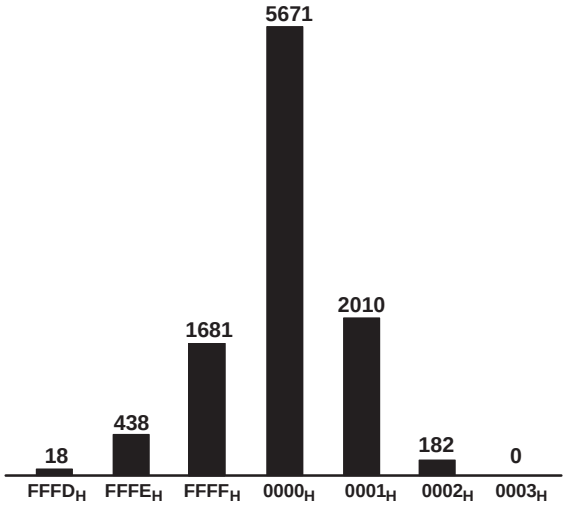


Figure 17. Histogram of 10000 Conversions With Input Grounded

PRODUCT PREVIEW

APPLICATION INFORMATION (continued)

AVERAGING

The noise of the converter can be compensated by averaging the digital codes. By averaging conversion results, transition noise is reduced by a factor of $1/\sqrt{Hz}$ where n is the number of averages. For example, averaging four conversion results reduces the TN by 1/2 to 0.4 LSBs. Averaging should only be used for input signals with frequencies near DC.

For AC signals, a digital filter can be used to low-pass filter and decimate the output codes. This works in a similar manner to averaging: for every decimation by 2, the signal-to-noise ratio improves 3 dB.

QSPI™ INTERFACE

Figure 18 shows a simple interface between the ADS8513 and any QSPI equipped microcontroller. This interface assumes that the convert pulse does not originate from the microcontroller and that the ADS8513 is the only serial peripheral.

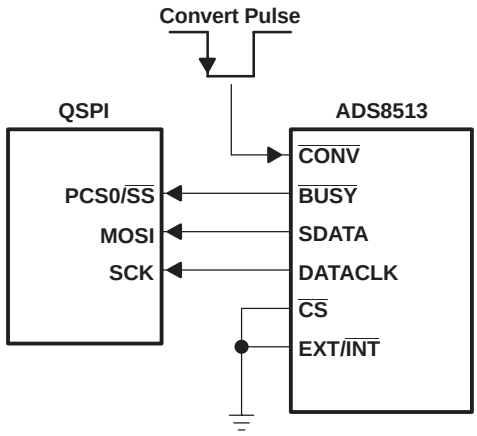


Figure 18. QSPI Interface to the ADS8513

Before enabling the QSPI interface, the microcontroller must be configured to monitor the slave select line. When a transition from low to high occurs on slave select ($\overline{SS}$) from $\overline{BUSY}$ (indicating the end of the current conversion), the port can be enabled. If this is not done, the microcontroller and the A/D converter may be *out-of-sync*.

Figure 19 shows another interface between the ADS8513 and a QSPI equipped microcontroller which allows the microcontroller to give the convert pulses while also allowing multiple peripherals to be connected to the serial bus. This interface and the following discussion assume a master clock for the QSPI interface of 16.78 MHz. Notice that the serial data input of the microcontroller is tied to the MSB (D7) of the ADS8513 instead of the serial output (SDATA). Using D7 instead of the serial port offers 3-state capability which allows other peripherals to be connected to the MISO pin. When communication is desired with those peripherals, PCS0 and PCS1 should be left high; that keeps D7 3-stated.

APPLICATION INFORMATION (continued)

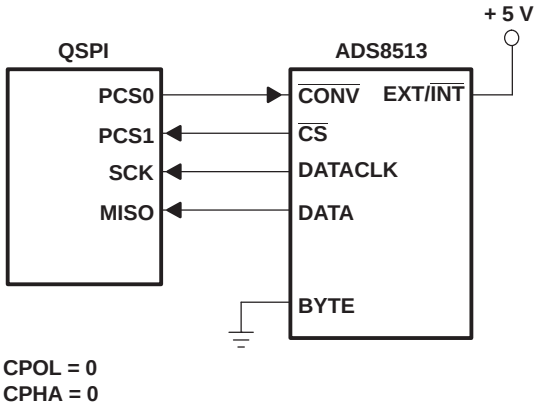


Figure 19. QSPI Interface to the ADS8513, Processor Initiates Conversions

In this configuration, the QSPI interface is actually set to do two different serial transfers. The first, an 8-bit transfer, causes PCS0 (R/$\overline{C}$) and PCS1 ($\overline{CS}$) to go low, starting a conversion. The second, a 16-bit transfer, causes only PCS1 (CS) to go low. This is when the valid data is transferred.

For both transfers, the DT register (delay after transfer) is used to cause a 19-µs delay. The interface is also set up to wrap to the beginning of the queue. In this manner, the QSPI is a state machine which generates the appropriate timing for the ADS8513. This timing is thus locked to the crystal-based timing of the microcontroller and not interrupt driven. So, this interface is appropriate for both AC and DC measurements.

For the fastest conversion rate, the baud rate should be set to 2 (4.19-MHz SCK), DT set to 10, the first serial transfer set to 8 bits, the second set to 16 bits, and DSCK disabled (in the command control byte). This allows for a 23-kHz maximum conversion rate. For slower rates, DT should be increased. Do not slow SCK as this may increase the chance of affecting the conversion results or accidently initiating a second conversion during the first 8-bit transfer.

In addition, CPOL and CPHA should be set to zero (SCK normally low and data captured on the rising edge). The command control byte for the 8-bit transfer should be set to 20_H and for the 16-bit transfer to 61_H.

SPI™ INTERFACE

The SPI interface is generally only capable of 8-bit data transfers. For some microcontrollers with SPI interfaces, it might be possible to receive data in a similar manner as shown for the QSPI interface in Figure 18. The microcontroller needs to fetch the 8 most significant bits before the contents are overwritten by the least significant bits.

A modified version of the QSPI interface shown in Figure 19 might be possible. For most microcontrollers with a SPI interface, the automatic generation of the start-of-conversion pulse is impossible and has to be done with software. This limits the interface to DC applications due to the insufficient jitter performance of the convert pulse itself.

PRODUCT PREVIEW

PACKAGING INFORMATION

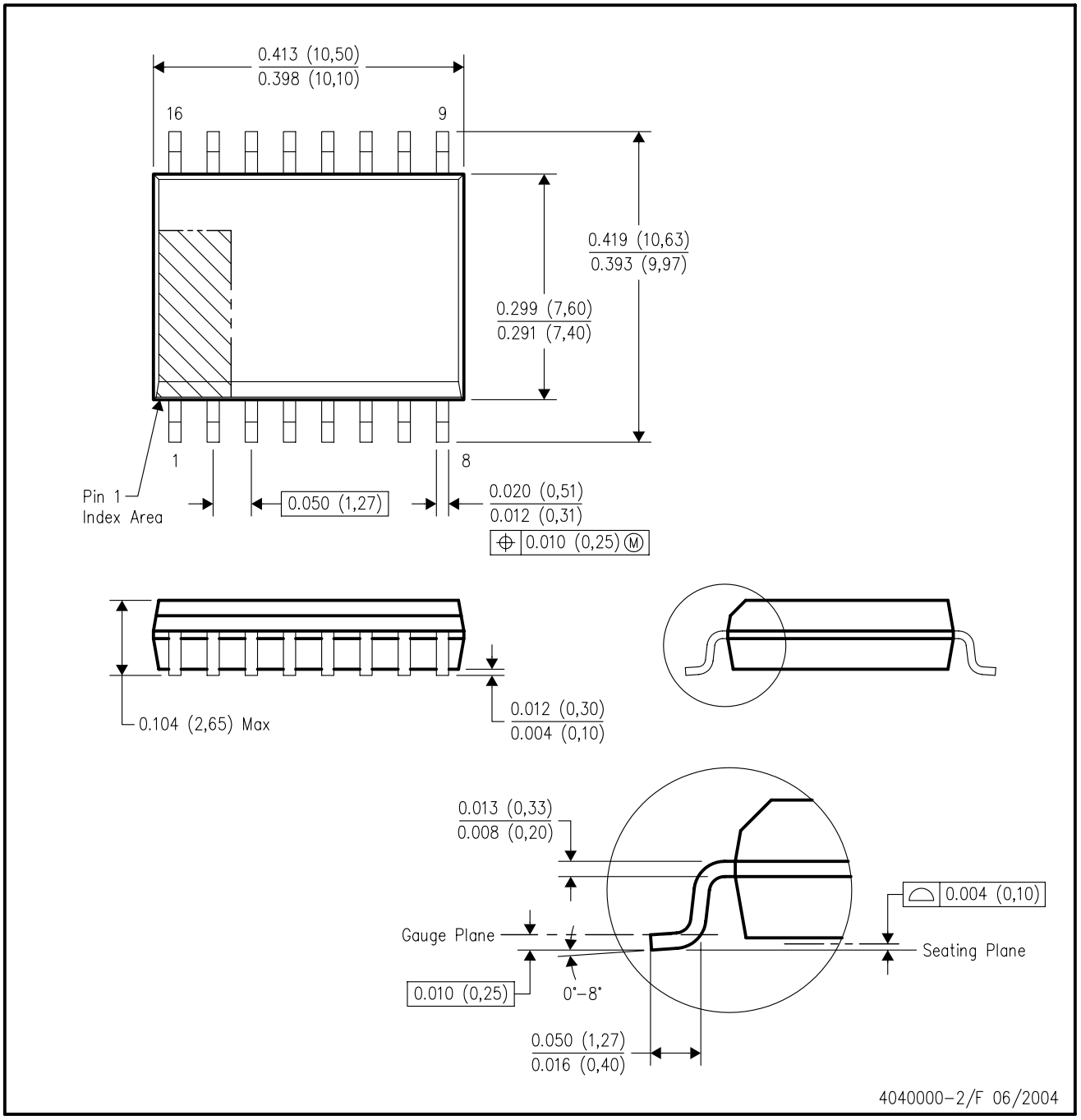
Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ADS8513IBDW	PREVIEW	SOIC	DW	16	40	TBD	Call TI	Call TI
ADS8513IBDWR	PREVIEW	SOIC	DW	16	2000	TBD	Call TI	Call TI
ADS8513IDW	PREVIEW	SOIC	DW	16	40	TBD	Call TI	Call TI
ADS8513IDWR	PREVIEW	SOIC	DW	16	2000	TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DW (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

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