

Power MOSFET

45 Amps, 25 Volts

N-Channel DPAK

Features

- Planar HD3e Process for Fast Switching Performance
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High-Efficiency DC-DC Converters
- Pb-Free Packages are Available

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	25	Vdc
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	Vdc
Thermal Resistance – Junction-to-Case	$R_{\theta JC}$	3.0	$^\circ\text{C/W}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	50	W
Drain Current	I_D	45	A
– Continuous @ $T_C = 25^\circ\text{C}$, Chip	I_D	32	A
– Continuous @ $T_A = 25^\circ\text{C}$, Limited by Wires	I_D	100	A
– Single Pulse ($t_p \leq 10 \mu\text{s}$)	I_D		
Thermal Resistance – Junction-to-Ambient (Note 1)	$R_{\theta JA}$	71.4	$^\circ\text{C/W}$
– Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	2.1	W
– Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	I_D	9.2	A
Thermal Resistance – Junction-to-Ambient (Note 2)	$R_{\theta JA}$	100	$^\circ\text{C/W}$
– Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.5	W
– Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	I_D	7.8	A
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$
Maximum Lead Temperature for Soldering Purposes, 1/8 in from case for 10 seconds	T_L	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using 0.5 sq. in pad size.
2. When surface mounted to an FR4 board using minimum recommended pad size.



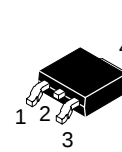
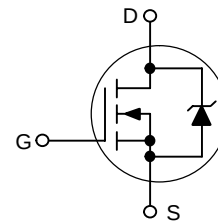
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<http://onsemi.com>

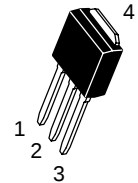
45 AMPERES, 25 VOLTS

$R_{DS(on)} = 12.6 \text{ m}\Omega$ (Typ)

N-CHANNEL

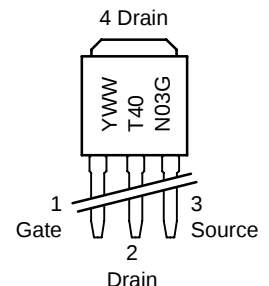
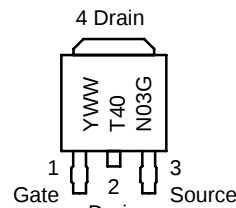


CASE 369AA
DPAK
(Surface Mount)
STYLE 2



CASE 369D
DPAK
(Straight Lead)
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENTS



Y = Year
 WW = Work Week
 T40N03 = Device Code
 G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTD40N03R

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V _{GS} = 0 Vdc, I _D = 250 μ Adc) Temperature Coefficient (Positive)	V(br) _{DSS}	25 –	28 –	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 20 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 20 Vdc, V _{GS} = 0 Vdc, T _J = 150°C)	I _{DSS}	– –	– –	1.0 10	μ Adc
Gate-Body Leakage Current (V _{GS} = $\pm$ 20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	–	–	$\pm$ 100	nAdc

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V _{DS} = V _{GS} , I _D = 250 μ Adc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	1.0 –	1.7 –	2.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V _{GS} = 4.5 Vdc, I _D = 10 Adc) (V _{GS} = 10 Vdc, I _D = 10 Adc)	R _{DS(on)}	– –	18.6 12.6	23 16.5	m Ω
Forward Transconductance (Note 3) (V _{DS} = 10 Vdc, I _D = 10 Adc)	g _{FS}	–	20	–	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 20 Vdc, V _{GS} = 0 V, f = 1 MHz)	C _{iss}	–	584	–	pF
Output Capacitance		C _{oss}	–	254	–	
Transfer Capacitance		C _{rss}	–	99	–	

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V _{GS} = 10 Vdc, V _{DD} = 10 Vdc, I _D = 10 Adc, R _G = 3 Ω)	t _{d(on)}	–	4.5	–	ns
Rise Time		t _r	–	19.5	–	
Turn-Off Delay Time		t _{d(off)}	–	16.7	–	
Fall Time		t _f	–	3.5	–	
Gate Charge	(V _{GS} = 4.5 Vdc, I _D = 10 Adc, V _{DS} = 10 Vdc) (Note 3)	Q _T	–	5.78	–	nC
		Q ₁	–	2.1	–	
		Q ₂	–	2.5	–	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = 10 Adc, V _{GS} = 0 Vdc) (Note 3) (I _S = 10 Adc, V _{GS} = 0 Vdc, T _J = 125°C)	V _{SD}	– –	0.85 0.71	1.2 –	Vdc
Reverse Recovery Time	(I _S = 10 Adc, V _{GS} = 0 Vdc, di _S /dt = 100 A/ μ s) (Note 3)	t _{rr}	–	20.4	–	ns
		t _a	–	8.25	–	
		t _b	–	12.1	–	
Reverse Recovery Stored Charge		Q _{RR}	–	0.007	–	μ C

3. Pulse Test: Pulse Width $\leq$ 300 μ s, Duty Cycle $\leq$ 2%.

4. Switching characteristics are independent of operating junction temperatures.

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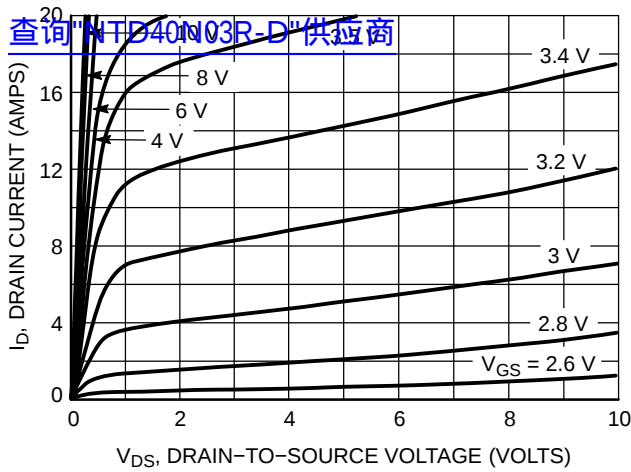


Figure 1. On-Region Characteristics

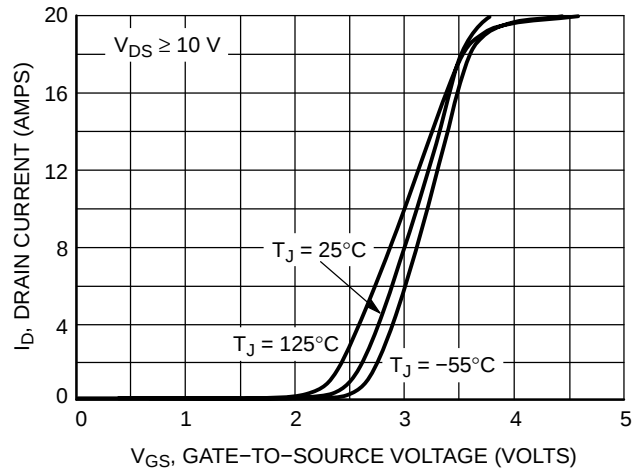


Figure 2. Transfer Characteristics

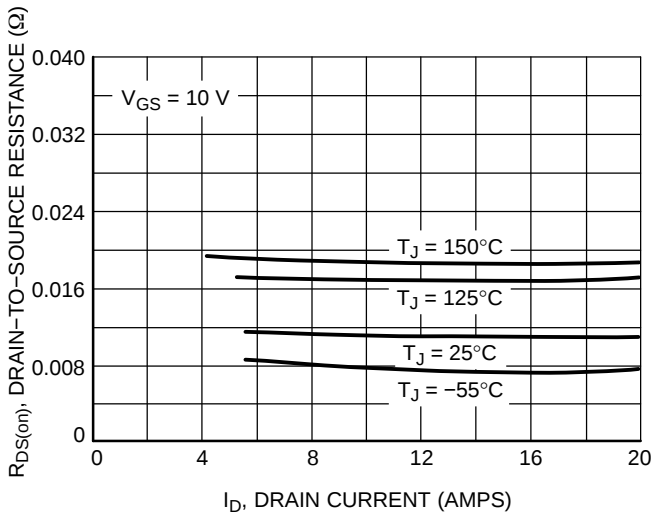


Figure 3. On-Resistance versus Drain Current and Temperature

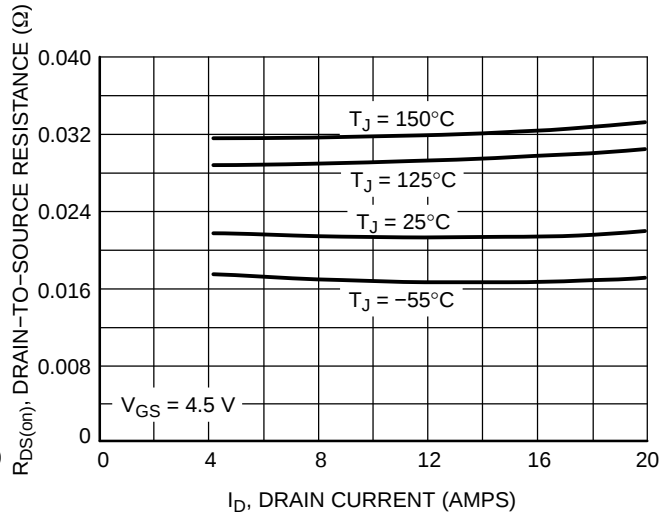


Figure 4. On-Resistance versus Drain Current and Temperature

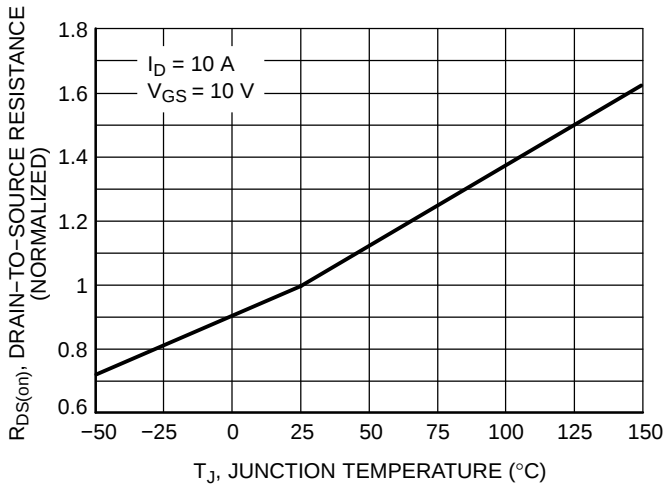


Figure 5. On-Resistance Variation with Temperature

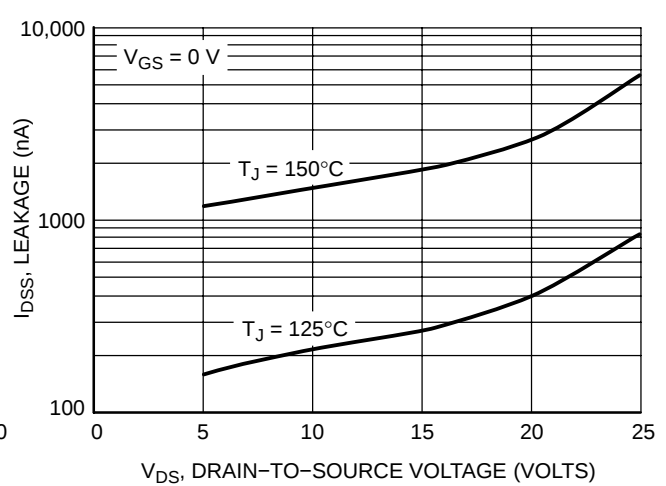


Figure 6. Drain-to-Source Leakage Current versus Voltage

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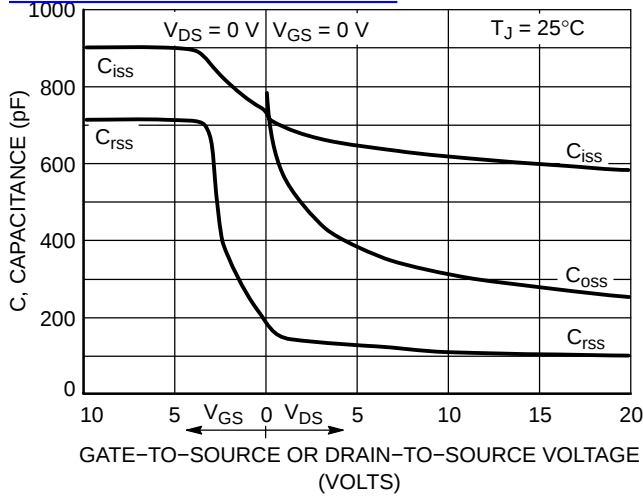


Figure 7. Capacitance Variation

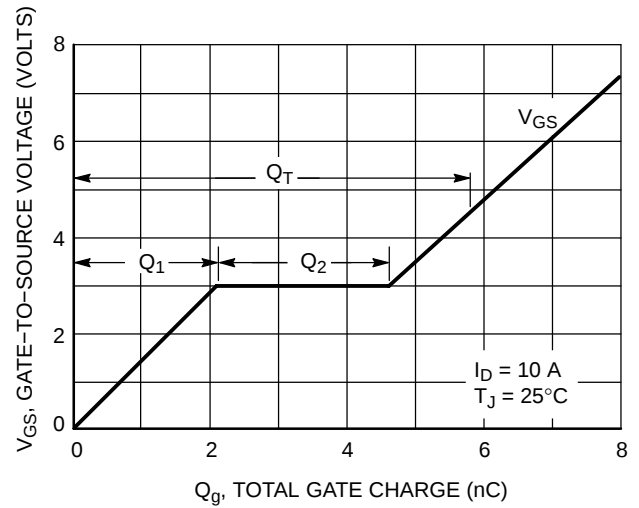


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

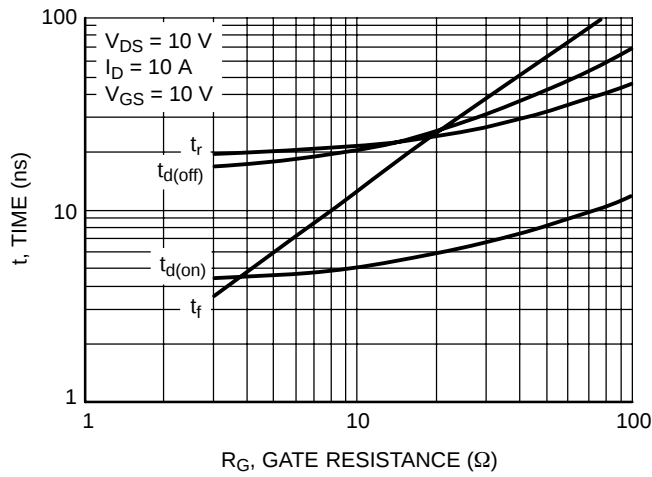


Figure 9. Resistive Switching Time Variation versus Gate Resistance

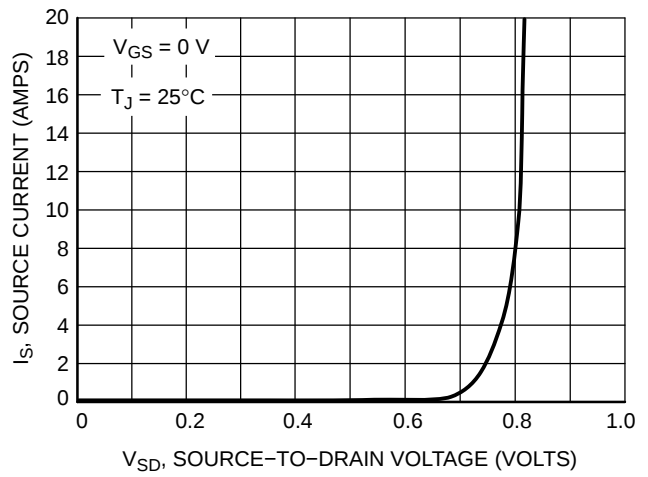


Figure 10. Diode Forward Voltage versus Current

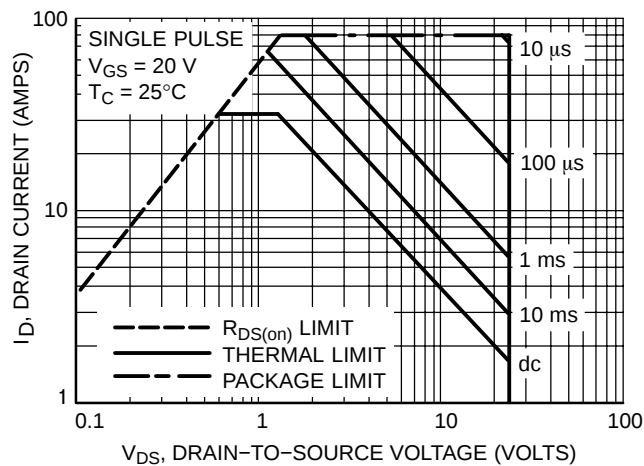


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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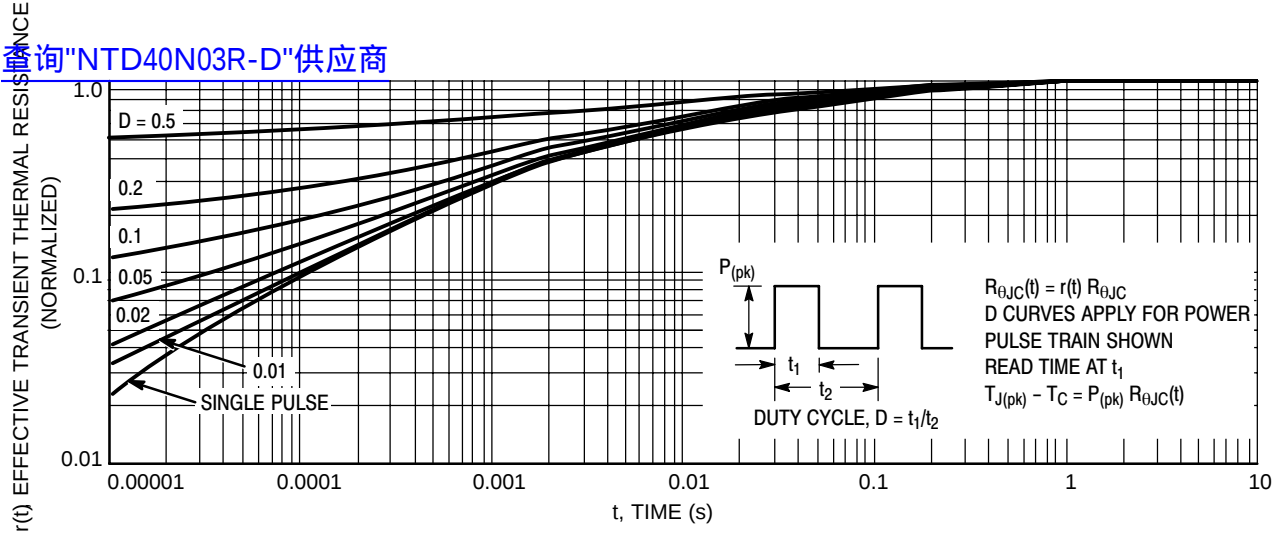


Figure 12. Thermal Response

ORDERING INFORMATION

Device	Package	Shipping [†]
NTD40N03R	DPAK	75 Units/Rail
NTD40N03RG	DPAK (Pb-Free)	75 Units/Rail
NTD40N03R-1	DPAK (Straight Lead)	75 Units/Rail
NTD40N03R-1G	DPAK (Straight Lead) (Pb-Free)	75 Units/Rail
NTD40N03RT4	DPAK	2500 Tape & Reel
NTD40N03RT4G	DPAK (Pb-Free)	2500 Tape & Reel

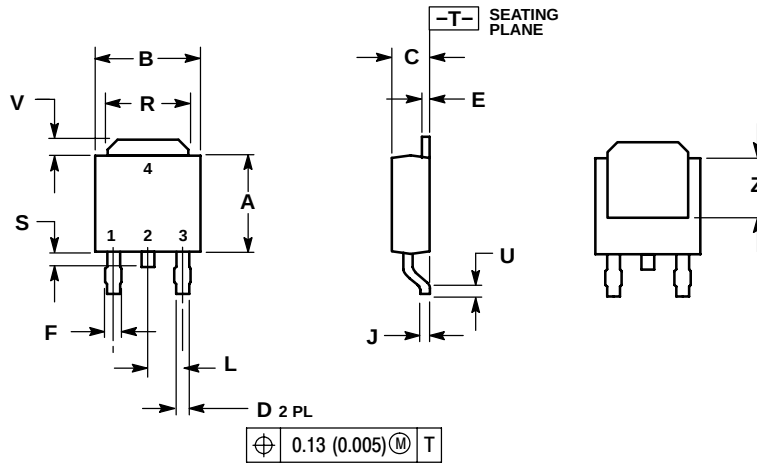
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTD40N03R

[查询"NTD40N03R-D"供应商](#)

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE) CASE 369AA-01 ISSUE O

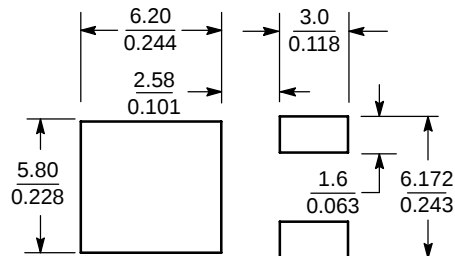


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.88
E	0.018	0.024	0.46	0.61
F	0.033	0.045	0.83	1.14
J	0.018	0.023	0.46	0.58
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}} \right)$

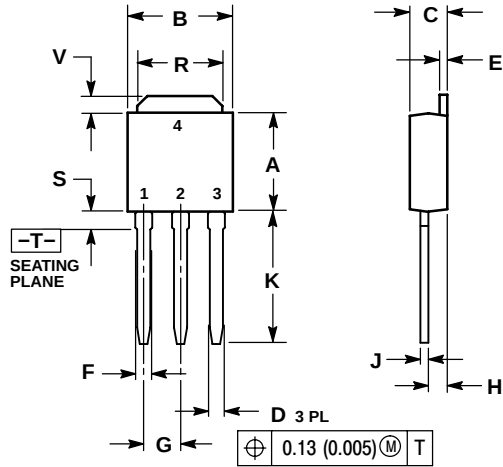
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTD40N03R

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PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE)
CASE 369D-01
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:

- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

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