National Semiconductor



# F100155
# Quad Multiplexer/Latch

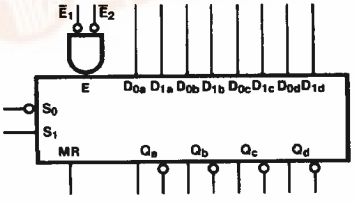
## General Description

The F100155 contains four transparent latches, each of which can accept and store data from two sources. When both Enable ($\overline{E}_n$) inputs are LOW, the data that appears at an output is controlled by the Select ($S_n$) inputs, as shown in the Operating Mode table. In addition to routing data from either $D_0$ or $D_1$, the Select inputs can force the outputs LOW for the case where the latch is transparent (both Enables are LOW) and can steer a HIGH signal from either $D_0$ or $D_1$ to an output. The Select inputs can be tied together for applications requiring only that data be steered from either $D_0$ or $D_1$. A positive-going signal on either Enable input latches the outputs. A HIGH signal on the Master Reset (MR) input overrides all the other inputs and forces the Q outputs LOW. All inputs have 50 kΩ pulldown resistors.

Refer to the F100355 datasheet for:
- PCC packaging
- Lower power
- Military versions
- Extended voltage specs (−4.2V to −5.7V)

## Ordering Code: See Section 8

## Logic Symbol

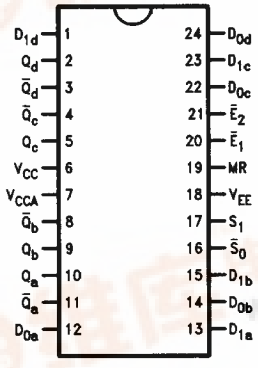



TL/F/9860–3

| Pin Names | Description |
|---|---|
| $\overline{E}_1$, $\overline{E}_2$ | Enable Inputs (Active LOW) |
| $\overline{S}_0$, $S_1$ | Select Inputs |
| MR | Master Reset |
| $D_{na}$–$D_{nd}$ | Data Inputs |
| $Q_a$–$Q_d$ | Data Outputs |
| $\overline{Q}_a$–$\overline{Q}_d$ | Complementary Data Outputs |

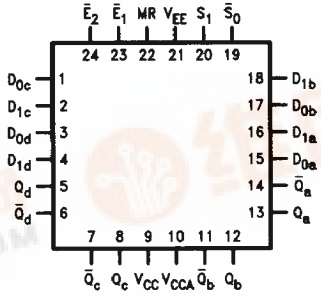
## Connection Diagrams

**24-Pin DIP**




TL/F/9860–1

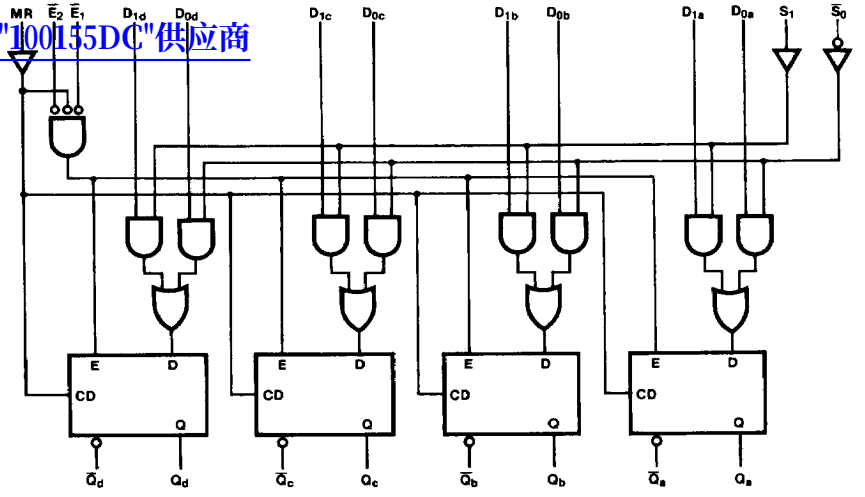
**24-Pin Quad Cerpak**




TL/F/9860–2

## Logic Diagram






TL/F/9860–5

### Operating Mode Table

| Controls | | | | Outputs |
|---|---|---|---|---|
| $\overline{E}_1$ | $\overline{E}_2$ | $S_1$ | $\overline{S}_0$ | $Q_n$ |
| H | X | X | X | Latched* |
| X | H | X | X | Latched* |
| L | L | L | L | $D_{0x}$ |
| L | L | H | L | $D_{0x} + D_{1x}$ |
| L | L | L | H | L |
| L | L | H | H | $D_{1x}$ |

*Stores data present before $\overline{E}$ went HIGH
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

### Truth Table

| Inputs | | | | | | | Outputs | |
|---|---|---|---|---|---|---|---|---|
| MR | $\overline{E}_1$ | $\overline{E}_2$ | $S_1$ | $\overline{S}_0$ | $D_{1x}$ | $D_{0x}$ | $\overline{Q}_x$ | $Q_x$ |
| H | X | X | X | X | X | X | H | L |
| L | L | L | H | H | H | X | L | H |
| L | L | L | H | H | L | X | H | L |
| L | L | L | L | L | X | H | L | H |
| L | L | L | L | L | X | L | H | L |
| L | L | L | L | H | X | X | H | L |
| L | L | L | H | L | H | X | L | H |
| L | L | L | H | L | X | H | L | H |
| L | L | L | H | L | L | L | H | L |
| L | H | X | X | X | X | X | Latched* | |
| L | X | H | X | X | X | X | Latched* | |

## Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Maximum Junction Temperature ($T_J$) | +150°C |
| Case Temperature under Bias ($T_C$) | 0°C to +85°C |
| $V_{EE}$ Pin Potential to Ground Pin | −7.0V to +0.5V |
| Input Voltage (DC) | $V_{EE}$ to +0.5V |
| Output Current (DC Output HIGH) | −50 mA |
| Operating Range (Note 2) | −5.0V to −4.2V |

## DC Electrical Characteristics

$V_{EE}$ = −4.5V, $V_{CC}$ = $V_{CCA}$ = GND, $T_C$ = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | −1025 | −955 | −880 | mV | $V_{IN}$ = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$ | Loading with 50Ω to −2.0V |
| $V_{OL}$ | Output LOW Voltage | −1810 | −1705 | −1620 | | | |
| $V_{OHC}$ | Output HIGH Voltage | −1035 | | | mV | $V_{IN}$ = $V_{IH(Min)}$ or $V_{IL\ (Max)}$ | Loading with 50Ω to −2.0V |
| $V_{OLC}$ | Output LOW Voltage | | | −1610 | | | |
| $V_{IH}$ | Input HIGH Voltage | −1165 | | −880 | mV | Guaranteed HIGH Signal for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | −1810 | | −1475 | mV | Guaranteed LOW Signal for All Inputs | |
| $I_{IL}$ | Input LOW Current | 0.50 | | | μA | $V_{IN}$ = $V_{IL\ (Min)}$ | |

## DC Electrical Characteristics

$V_{EE}$ = −4.2V, $V_{CC}$ = $V_{CCA}$ = GND, $T_C$ = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | −1020 | | −870 | mV | $V_{IN}$ = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$ | Loading with 50Ω to −2.0V |
| $V_{OL}$ | Output LOW Voltage | −1810 | | −1605 | | | |
| $V_{OHC}$ | Output HIGH Voltage | −1030 | | | mV | $V_{IN}$ = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$ | Loading with 50Ω to −2.0V |
| $V_{OLC}$ | Output LOW Voltage | | | −1595 | | | |
| $V_{IH}$ | Input HIGH Voltage | −1150 | | −870 | mV | Guaranteed HIGH Signal for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | −1810 | | −1475 | mV | Guaranteed LOW Signal for All Inputs | |
| $I_{IL}$ | Input LOW Current | 0.50 | | | μA | $V_{IN}$ = $V_{IL\ (Min)}$ | |

## DC Electrical Characteristics

$V_{EE}$ = −4.8V, $V_{CC}$ = $V_{CCA}$ = GND, $T_C$ = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | −1035 | | −880 | mV | $V_{IN}$ = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$ | Loading with 50Ω to −2.0V |
| $V_{OL}$ | Output LOW Voltage | −1830 | | −1620 | | | |
| $V_{OHC}$ | Output HIGH Voltage | −1045 | | | mV | $V_{IN}$ = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$ | Loading with 50Ω to −2.0V |
| $V_{OLC}$ | Output LOW Voltage | | | −1610 | | | |
| $V_{IH}$ | Input HIGH Voltage | −1165 | | −880 | mV | Guaranteed HIGH Signal for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | −1830 | | −1490 | mV | Guaranteed LOW Signal for All Inputs | |
| $I_{IL}$ | Input LOW Current | 0.50 | | | μA | $V_{IN}$ = $V_{IL\ (Min)}$ | |

**Note 1:** Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Parametric values specified at −4.2V to −4.8V.

**Note 3:** The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

**Note 4:** Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

## DC Electrical Characteristics

$V_{EE}$ = −4.2V to −4.8V unless otherwise specified, $V_{CC}$ = $V_{CCA}$ = GND, $T_C$ = 0°C to +85°C

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_{IH}$ | Input HIGH Current | | | | | |
| | $\overline{S}_0$, $S_1$ | | | 220 | μA | $V_{IN}$ = $V_{IH\ (Max)}$ |
| | $\overline{E}_1$, $\overline{E}_2$ | | | 350 | | |
| | $D_{na}$–$D_{nd}$ | | | 340 | | |
| | MR | | | 430 | | |
| $I_{EE}$ | Power Supply Current | −133 | −95 | −66 | mA | Inputs Open |



## Ceramic Dual-In-Line Package AC Electrical Characteristic

$V_{EE}$ = −4.2V to −4.8V, $V_{CC}$ = $V_{CCA}$ = GND

| Symbol | Parameter | $T_C$ = 0°C | | $T_C$ = +25°C | | $T_C$ = +85°C | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $D_{na}$–$D_{nd}$ to Output (Transparent Mode) | 0.50 | 1.90 | 0.60 | 1.85 | 0.50 | 1.90 | ns | *Figures 1* and *2* |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $\overline{S}_0$ $S_1$ to Output (Transparent Mode) | 1.50 | 3.50 | 1.50 | 3.40 | 1.50 | 3.50 | ns | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $\overline{E}_1$, $\overline{E}_2$ to Output | 0.90 | 2.50 | 1.00 | 2.40 | 1.00 | 2.50 | ns | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay MR to Output | 0.90 | 3.00 | 0.90 | 2.90 | 0.90 | 3.00 | ns | *Figures 1* and *3* |
| $t_{TLH}$ $t_{THL}$ | Transition Time 20% to 80%, 80% to 20% | 0.60 | 2.30 | 0.60 | 2.20 | 0.45 | 2.30 | ns | *Figures 1* and *2* |
| $t_S$ | Setup Time | | | | | | | | |
| | $D_{na}$–$D_{nd}$ | 0.90 | | 0.90 | | 0.90 | | ns | *Figure 4* |
| | $\overline{S}_0$, $S_1$ | 2.40 | | 2.40 | | 2.70 | | | |
| | MR (Release Time) | 1.50 | | 1.50 | | 1.50 | | | *Figure 3* |
| $t_H$ | Hold Time | | | | | | | | |
| | $D_{na}$–$D_{nd}$ | 0.40 | | 0.40 | | 0.40 | | ns | *Figure 4* |
| | $\overline{S}_0$, $S_1$ | −0.70 | | −0.70 | | −0.70 | | | |
| $t_{pw}$ (L) | Pulse Width LOW $\overline{E}_1$, $\overline{E}_2$ | 2.00 | | 2.00 | | 2.00 | | ns | *Figure 2* |
| $t_{pw}$ (H) | Pulse Width HIGH MR | 2.00 | | 2.00 | | 2.00 | | ns | *Figure 3* |

## Cerpak AC Electrical Characteristics

$V_{EE}$ = −4.2V to −4.8V, $V_{CC}$ = $V_{CCA}$ = GND

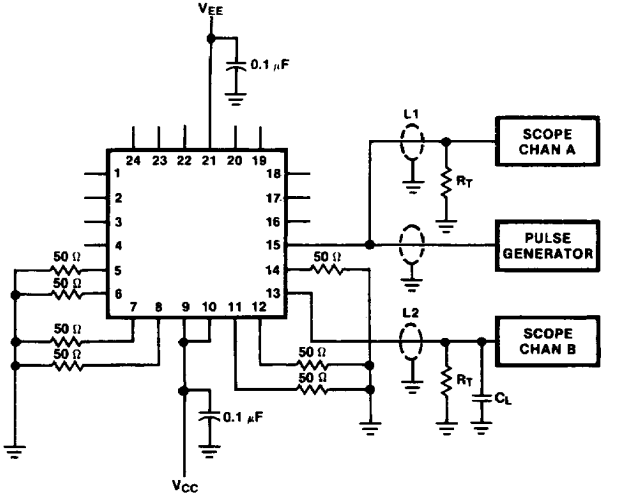
| Symbol | Parameter | $T_C$ = 0°C | | $T_C$ = +25°C | | $T_C$ = +85°C | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $D_{na}$–$D_{nd}$ to Output (Transparent Mode) | 0.50 | 1.70 | 0.60 | 1.65 | 0.50 | 1.70 | ns | *Figures 1* and *2* |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $\overline{S}_1$, $S_1$ to Output (Transparent Mode) | 1.50 | 3.30 | 1.50 | 3.20 | 1.50 | 3.30 | ns | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $\overline{E}_1$, $\overline{E}_2$ to Output | 0.90 | 2.30 | 1.00 | 2.20 | 1.00 | 2.30 | ns | |

## Cerpak AC Electrical Characteristics

$V_{EE}$ = −4.2V to −4.8V, $V_{CC}$ = $V_{CCA}$ = GND (Continued)

| Symbol | Parameter | $T_C$ = 0°C | | $T_C$ = +25°C | | $T_C$ = +85°C | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>MR to Output | 0.90 | 2.80 | 0.90 | 2.70 | 0.90 | 2.80 | ns | *Figures 1* and *3* |
| $t_{TLH}$<br>$t_{THL}$ | Transition Time<br>20% to 80%, 80% to 20% | 0.60 | 2.20 | 0.60 | 2.10 | 0.45 | 2.20 | ns | *Figures 1* and *2* |
| $t_S$ | Setup Time<br>$D_{na}$–$D_{nd}$<br>$\overline{S}_0$, $S_1$<br>MR (Release Time) | 0.80<br>2.30<br>1.40 | | 0.80<br>2.30<br>1.40 | | 0.80<br>2.60<br>1.40 | | ns | *Figure 4*<br>*Figure 3* |
| $t_H$ | Hold Time<br>$D_{na}$–$D_{nd}$<br>$\overline{S}_0$, $S_1$ | 0.30<br>−0.80 | | 0.30<br>−0.80 | | 0.30<br>−0.80 | | ns | *Figure 4* |
| $t_{pw}$ (L) | Pulse Width LOW $\overline{E}_1$, $\overline{E}_2$ | 2.00 | | 2.00 | | 2.00 | | ns | *Figure 2* |
| $t_{pw}$ (H) | Pulse Width HIGH MR | 2.00 | | 2.00 | | 2.00 | | ns | *Figure 3* |

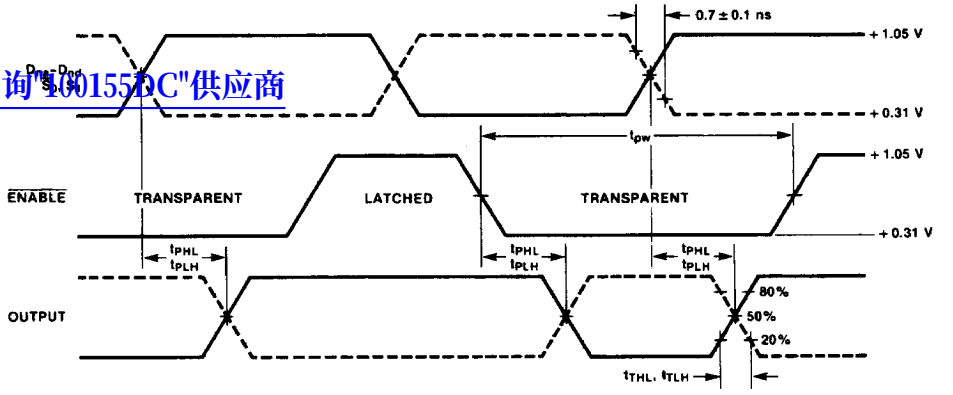





TL/F/9860–6

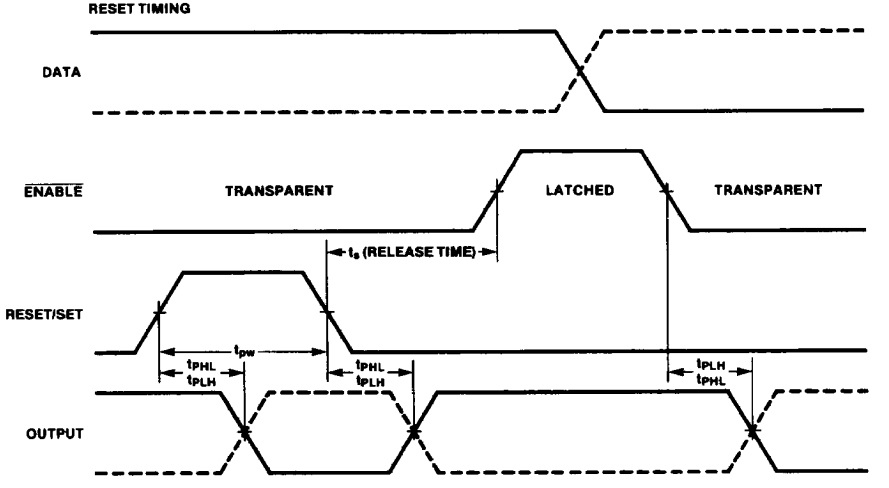
**FIGURE 1. AC Test Circuit**

**Notes:**
$V_{CC}$, $V_{CCA}$ = +2V, $V_{EE}$ = −2.5V
L1 and L2 = equal length 50Ω impedance lines
$R_T$ = 50Ω terminator internal to scope
Decoupling 0.1 µF from GND to $V_{CC}$ and $V_{EE}$
All unused outputs are loaded with 50Ω to GND
$C_L$ = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol



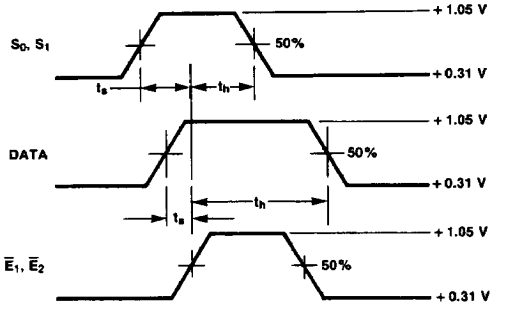

TL/F/9860–7

**FIGURE 2. Enable Timing**




TL/F/9860–8

**FIGURE 3. Reset Timing**




TL/F/9860–9

**FIGURE 4. Data Setup and Hold Times**

**Notes:**

$t_s$ is the minimum time before the transition of the enable that information must be present at the data input.

$t_h$ is the minimum time after the transition of the enable that information must remain unchanged at the data input.