

General Description

The MIC5013 is an 8-pin MOSFET driver with over-current shutdown and a fault flag. It is designed to drive the gate of an N-channel power MOSFET above the supply rail high-side power switch applications. The MIC5013 is compatible with standard or current-sensing power MOSFETs in both high- and low-side driver topologies.

The MIC5013 charges a 1nF load in 60μs typical and protects the MOSFET from over-current conditions. The current sense trip point is fully programmable and a dynamic threshold allows high in-rush current loads to be started. A fault pin indicates when the MIC5013 has turned off the FET due to excessive current.

Other members of the Micrel driver family include the MIC5011 minimum parts count driver and MIC5012 dual driver.

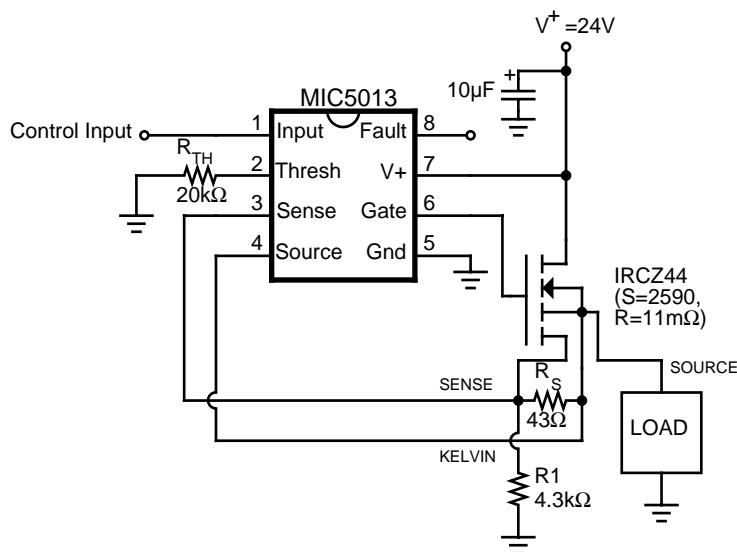
Features

- 7V to 32V operation
- Less than 1μA standby current in the “OFF” state
- Available in small outline SOIC packages
- Internal charge pump to drive the gate of an N-channel power FET above supply
- Internal zener clamp for gate protection
- 60μs typical turn-on time to 50% gate overdrive
- Programmable over-current sensing
- Dynamic current threshold for high in-rush loads
- Fault output pin indicates current faults
- Implements high- or low-side switches

Applications

- Lamp drivers
- Relay and solenoid drivers
- Heater switching
- Power bus switching
- Motion control

Typical Application



$$R_S = \frac{SR(V_{TRIP} + 100mV)}{R I_L - (V_{TRIP} + 100mV)}$$

$$R1 = \frac{V^+ SRR_S}{100mV (SR + R_S)}$$

$$R_{TH} = \frac{2200}{V_{TRIP}} - 1000$$

For this example:

$$I_L = 30A \text{ (trip current)}$$

$$V_{TRIP} = 100mV$$

Figure 1. High-Side Driver with Current-Sensing MOSFET

Note: The MIC5013 is ESD sensitive.

Protected under one or more of the following Micrel patents:
patent #4,951,101; patent #4,914,546

Absolute Maximum Ratings (Note 1, 2)

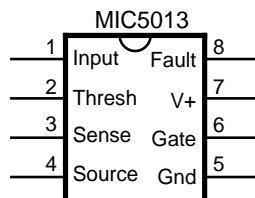
Input Voltage, Pin 1	-10 to V ⁺
Threshold Voltage, Pin 2	-0.5 to +5V
Sense Voltage, Pin 3	-10V to V ⁺
Source Voltage, Pin 4	-10V to V ⁺
Current into Pin 4	50mA
Gate Voltage, Pin 6	-1V to 50V
Supply Voltage (V ⁺), Pin 7	-0.5V to 36V
Fault Output Current, Pin 8	-1mA to +1mA
Junction Temperature	150°C

Operating Ratings (Notes 1, 2)

Power Dissipation	1.25W
θ_{JA} (Plastic DIP)	100°C/W
θ_{JA} (SOIC)	170°C/W
Ambient Temperature: B version	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Lead Temperature	260°C
(Soldering, 10 seconds)	
Supply Voltage (V ⁺), Pin 7	7V to 32V high side 7V to 15V low side

Pin Description (Refer to Figures 1 and 2)

Pin Number	Pin Name	Pin Function
1	Input	Resets current sense latch and turns on power MOSFET when taken above threshold (3.5V typical). Pin 1 requires <math><1\mu\text{A}</math> to switch.
2	Threshold	Sets current sense trip voltage according to: $V_{\text{TRIP}} = \frac{2200}{R_{\text{TH}} + 1000}$ where R_{TH} to ground is 3.3k Ω to 20k Ω . Adding capacitor C_{TH} increases the trip voltage at turn-on to 2V. Use $C_{\text{TH}} = 10\mu\text{F}$ for a 10ms turn-on time constant.
3	Sense	The sense pin causes the current sense to trip when V_{SENSE} is V_{TRIP} above V_{SOURCE} . Pin 3 is used in conjunction with a current shunt in the source of a 3 lead FET or a resistor R_S in the sense lead of a current sensing FET.
4	Source	Reference for the current sense voltage on pin 3 and return for the gate clamp zener. Connect to the load side of current shunt or kelvin lead of current sensing FET. Pins 3 and 4 can safely swing to -10V when turning off inductive loads.
5	Ground	
6	Gate	Drives and clamps the gate of the power FET. Pin 6 will be clamped to approximately -0.7V by an internal diode when turning off inductive loads.
7	V ⁺	Supply pin; must be decoupled to isolate from large transients caused by the power FET drain. 10 μF is recommended close to pins 7 and 5.
8	Fault	Outputs status of protection circuit when pin 1 is high. Fault low indicates normal operation; fault high indicates current sense tripped.

Pin Configuration

Electrical Characteristics (Note 3) Test circuit. $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V^+ = 15\text{V}$, all switches open, unless otherwise specified.

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Parameter	Conditions		Min	Typical	Max	Units	
Supply Current, I_7	$V^+ = 32\text{V}$	$V_{\text{IN}} = 0\text{V}$, S4 closed		0.1	10	μA	
		$V_{\text{IN}} = V_S = 32\text{V}$		8	20	mA	
Logic Input Voltage, V_{IN}	$V^+ = 4.75\text{V}$	Adjust V_{IN} for V_{GATE} low			2	V	
		Adjust V_{IN} for V_{GATE} high	4.5			V	
	$V^+ = 15\text{V}$	Adjust V_{IN} for V_{GATE} high	5.0			V	
Logic Input Current, I_1	$V^+ = 32\text{V}$	$V_{\text{IN}} = 0\text{V}$	-1			μA	
		$V_{\text{IN}} = 32\text{V}$			1	μA	
Input Capacitance	Pin 1			5		pF	
Gate Drive, V_{GATE}	S1, S2 closed, $V_S = V^+$, $V_{\text{IN}} = 5\text{V}$	$V^+ = 7\text{V}$, $I_6 = 0$	13	15		V	
		$V^+ = 15\text{V}$, $I_6 = 100\ \mu\text{A}$	24	27		V	
Zener Clamp, $V_{\text{GATE}} - V_{\text{SOURCE}}$	S2 closed, $V_{\text{IN}} = 5\text{V}$	$V^+ = 15\text{V}$, $V_S = 15\text{V}$	11	12.5	15	V	
		$V^+ = 32\text{V}$, $V_S = 32\text{V}$	11	13	16	V	
Gate Turn-on Time, t_{ON} (Note 4)	V_{IN} switched from 0 to 5V; measure time for V_{GATE} to reach 20V			60	200	μs	
Gate Turn-off Time, t_{OFF}	V_{IN} switched from 5 to 0V; measure time for V_{GATE} to reach 1V			4	10	μs	
Threshold Bias Voltage, V_2	$I_2 = 200\ \mu\text{A}$		1.7	2	2.2	V	
Current Sense Trip Voltage, $V_{\text{SENSE}} - V_{\text{SOURCE}}$	S2 closed, $V_{\text{IN}} = 5\text{V}$, Increase I_3	$V^+ = 7\text{V}$, $I_2 = 100\ \mu\text{A}$	S4 closed	75	105	135	mV
		$V^+ = 15\text{V}$, $I_2 = 200\ \mu\text{A}$	$V_S = 4.9\text{V}$, S4 open	70	100	130	mV
			S4 closed	150	210	270	mV
			$V_S = 11.8\text{V}$, S4 open	140	200	260	mV
			$V^+ = 32\text{V}$, $I_2 = 500\ \mu\text{A}$	$V_S = 0\text{V}$, S4 open	360	520	680
		$V_S = 25.5\text{V}$, S4 open	350	500	650	mV	
Peak Current Trip Voltage, $V_{\text{SENSE}} - V_{\text{SOURCE}}$	S3, S4 closed, $V^+ = 15\text{V}$, $V_{\text{IN}} = 5\text{V}$		1.6	2.1		V	
Fault Output Voltage, V_8	$V_{\text{IN}} = 0\text{V}$, $I_8 = -100\ \mu\text{A}$			0.4	1	V	
	$V_{\text{IN}} = 5\text{V}$, $I_8 = 100\ \mu\text{A}$, current sense tripped		14	14.6		V	

Note 1 **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified **Operating Ratings**.

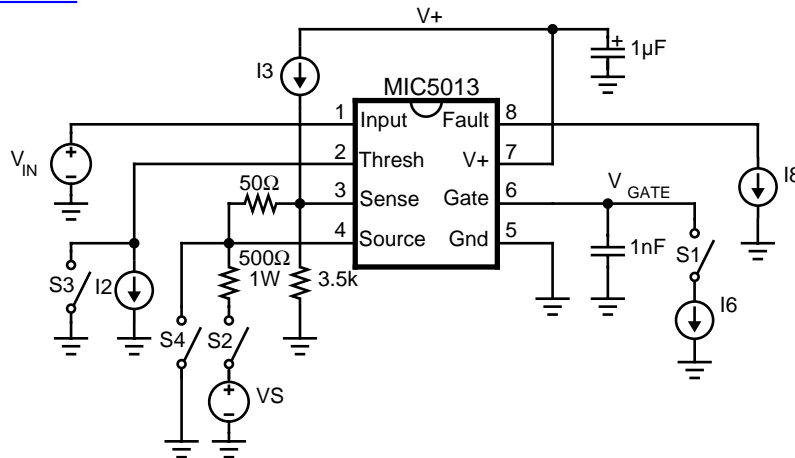
Note 2 The MIC5010 is ESD sensitive.

Note 3 Minimum and maximum **Electrical Characteristics** are 100% tested at $T_A = 25^\circ\text{C}$ and $T_A = 85^\circ\text{C}$, and 100% guaranteed over the entire range. Typicals are characterized at 25°C and represent the most likely parametric norm.

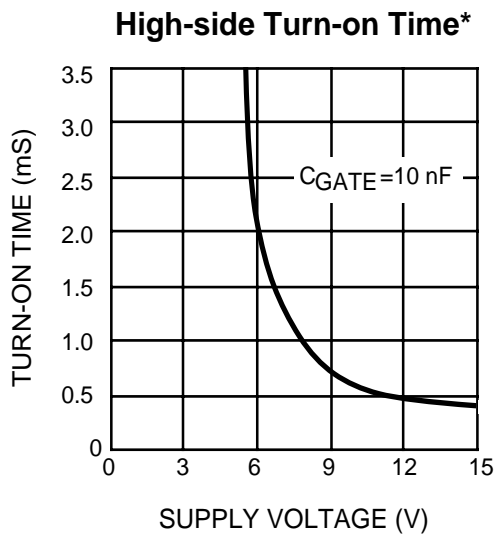
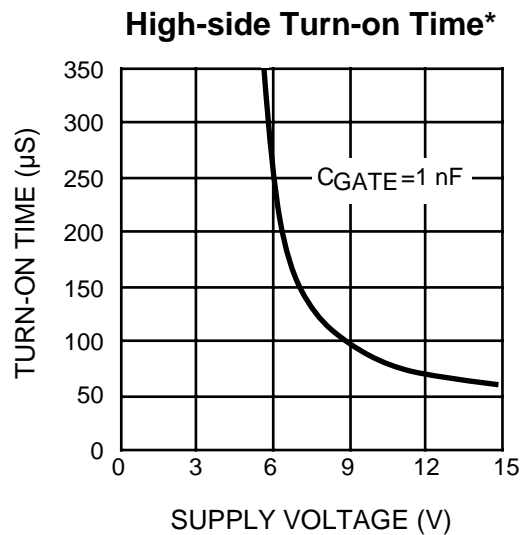
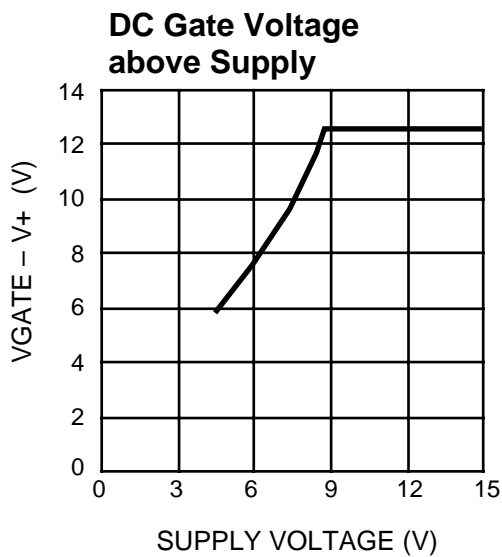
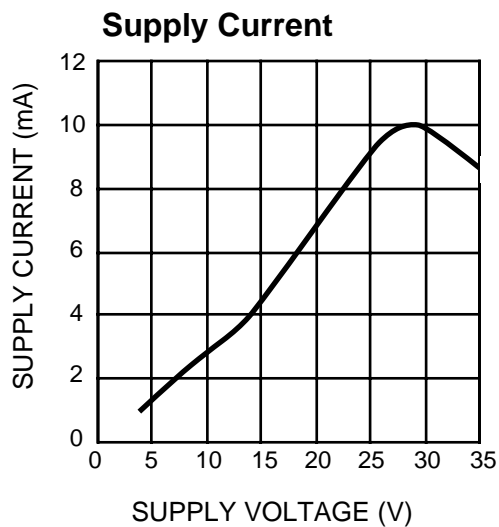
Note 4 Test conditions reflect worst case high-side driver performance. Low-side and bootstrapped topologies are significantly faster—see **Applications Information**.

Test Circuit

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Typical Characteristics

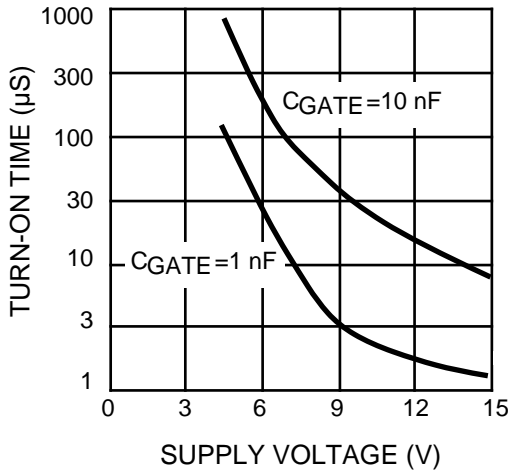


* Time for gate to reach V+ + 5V in test circuit with VS = V+ - 5V (prevents gate clamp from interfering with measurement).

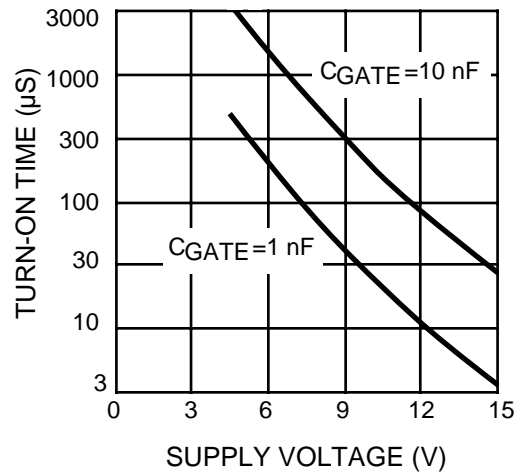
Typical Characteristics (Continued)

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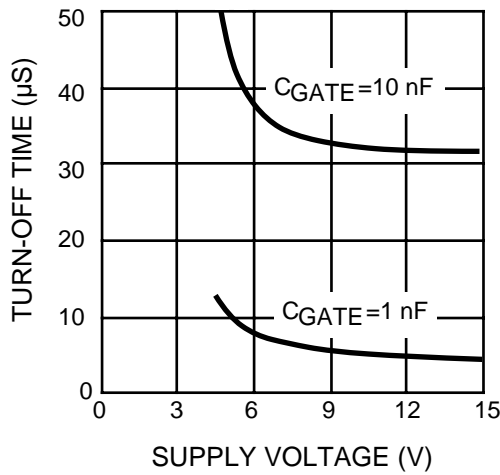
Low-side Turn-on Time for Gate = 5V



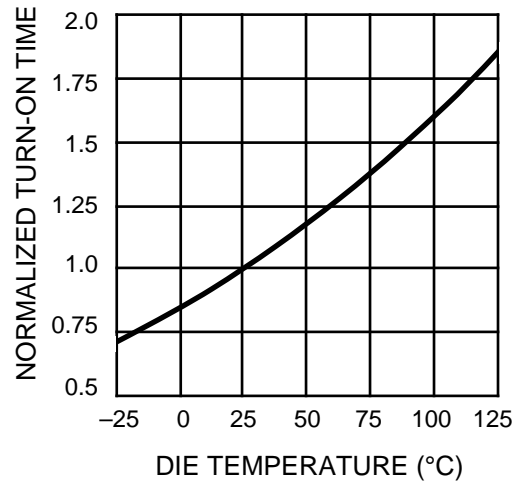
Low-side Turn-on Time for Gate = 10V



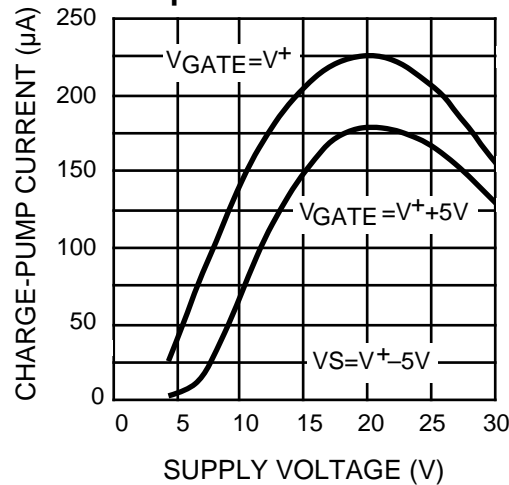
Turn-off Time



Turn-on Time

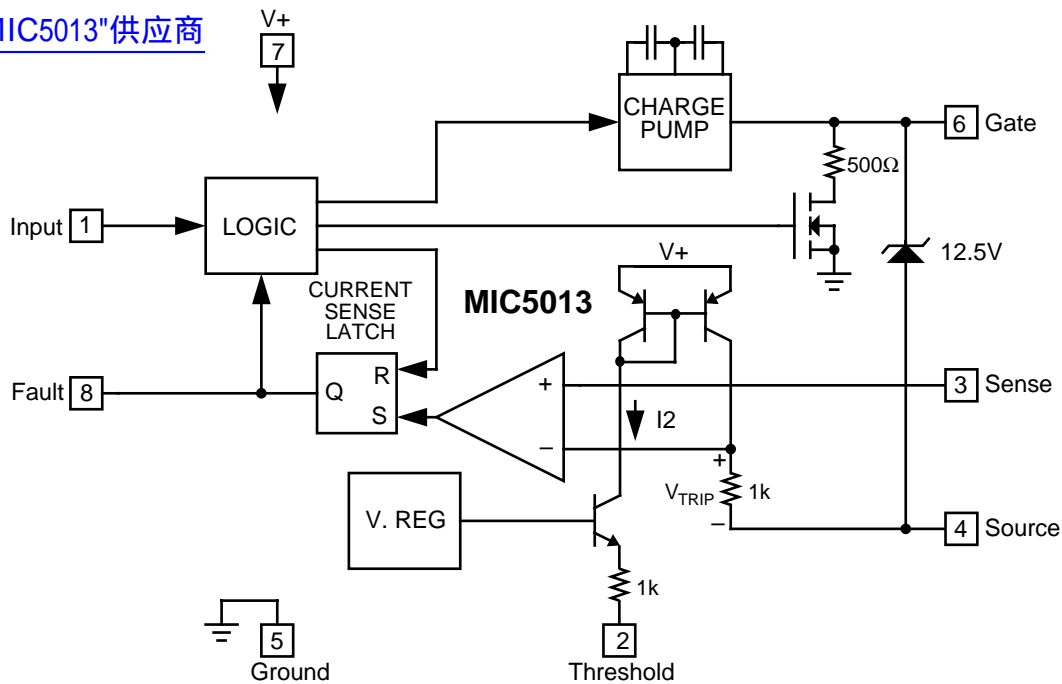


Charge Pump Output Current



Block Diagram

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Applications Information

Functional Description (refer to block diagram)

The various MIC5013 functions are controlled via a logic block connected to the input pin 1. When the input is low, all functions are turned off for low standby current and the gate of the power MOSFET is also held low through 500Ω to an N-channel switch. When the input is taken above the turn-on threshold (3.5V typical), the N-channel switch turns off and the charge pump is turned on to charge the gate of the power FET. A bandgap type voltage regulator is also turned on which biases the current sense circuitry.

The charge pump incorporates a 100kHz oscillator and on-chip pump capacitors capable of charging 1nF to 5V above supply in 60μs typical. The charge pump is capable of pumping the gate up to over twice the supply voltage. For this reason, a zener clamp (12.5V typical) is provided between the gate pin 6 and source pin 4 to prevent exceeding the V_{GS} rating of the MOSFET at high supplies.

The current sense operates by comparing the sense voltage at pin 3 to an offset version of the source voltage at pin 4. Current I_2 flowing in threshold pin 2 is mirrored and returned to the source via a 1kΩ resistor to set the offset, or trip voltage. When $(V_{SENSE} - V_{SOURCE})$ exceeds V_{TRIP} , the current sense trips and sets the current sense latch to turn off the power FET. An integrating comparator is used to reduce sensitivity to spikes on pin 3. The latch is reset to turn the FET back on by "recycling" the input pin 1 low and then high again.

A resistor R_{TH} from pin 2 to ground sets I_2 , and hence V_{TRIP} . An additional capacitor C_{TH} from pin 2 to ground creates a higher trip voltage at turn-on, which is necessary to prevent high in-rush current loads such as lamps or capacitors from false-tripping the current sense.

When the current sense has tripped, the fault pin 8 will be high as long as the input pin 1 remains high. However, when the input is low the fault pin will also be low.

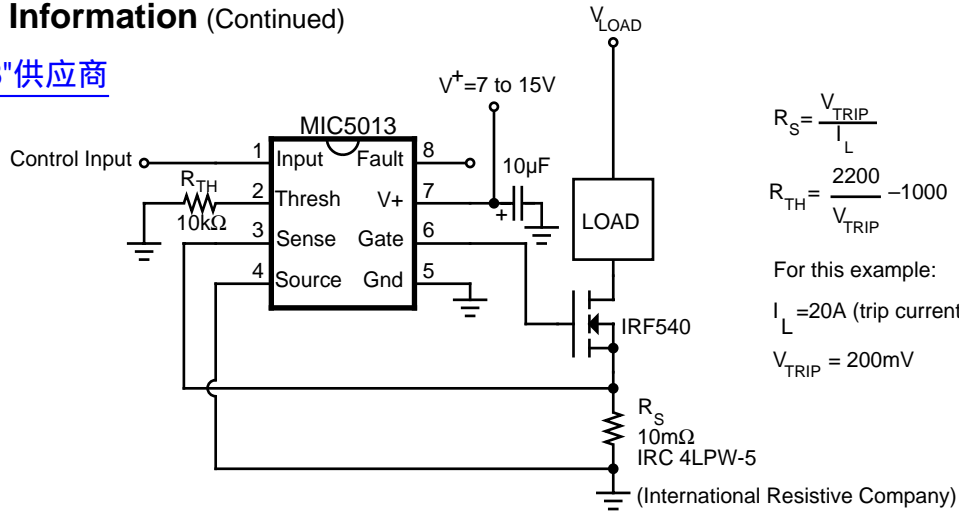
Construction Hints

High current pulse circuits demand equipment and assembly techniques that are more stringent than normal low current lab practices. The following are the sources of pitfalls most often encountered during prototyping: Supplies: many bench power supplies have poor transient response. Circuits that are being pulse tested, or those that operate by pulse-width modulation will produce strange results when used with a supply that has poor ripple rejection, or a peaked transient response. Monitor the power supply voltage that appears at the drain of a high-side driver (or the supply side of the load in a low-side driver) with an oscilloscope. It is not uncommon to find bench power supplies in the 1kW class that overshoot or undershoot by as much as 50% when pulse loaded. Not only will the load current and voltage measurements be affected, but it is possible to over-stress various components—especially electrolytic capacitors—with possibly catastrophic results. A 10μF supply bypass capacitor at the chip is recommended.

Residual Resistances: Resistances in circuit connections may also cause confusing results. For example, a circuit may employ a 50mΩ power MOSFET for low drop, but careless construction techniques could easily add 50 to 100mΩ resistance. Do not use a socket for the MOSFET. If the MOSFET is a TO-220 type package, make high-current drain connections to the tab. Wiring losses have a profound effect on high-current circuits. A floating millivoltmeter can identify connections that are contributing excess drop under load.

Applications Information (Continued)

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$$R_S = \frac{V_{TRIP}}{I_L}$$

$$R_{TH} = \frac{2200}{V_{TRIP}} - 1000$$

For this example:

$$I_L = 20A \text{ (trip current)}$$

$$V_{TRIP} = 200mV$$

(International Resistive Company)

Figure 2. Low-Side Driver with Current Shunt

Circuit Topologies

The MIC5013 is suited for use in high- or low-side driver applications with over-current protection for both current-sensing and standard MOSFETs. In addition, the MIC5013 works well in applications where, for faster switching times, the supply is bootstrapped from the MOSFET source output. Low voltage, high-side drivers (such as shown in the Test Circuit) are the slowest; their speed is reflected in the gate turn-on time specifications. The fastest drivers are the low-side and bootstrapped high-side types. Load current switching times are often much faster than the time to full gate enhancement, depending on the circuit type, the MOSFET, and the load. Turn-off times are essentially the same for all circuits (less than 10μs to V_{GS} = 1V). The choice of one topology over another is based on a combination of considerations including speed, voltage, and desired system characteristics. Each topology is described in this section. Note that I_L, as used in the design equations, is the load current that just trips the over-current comparator.

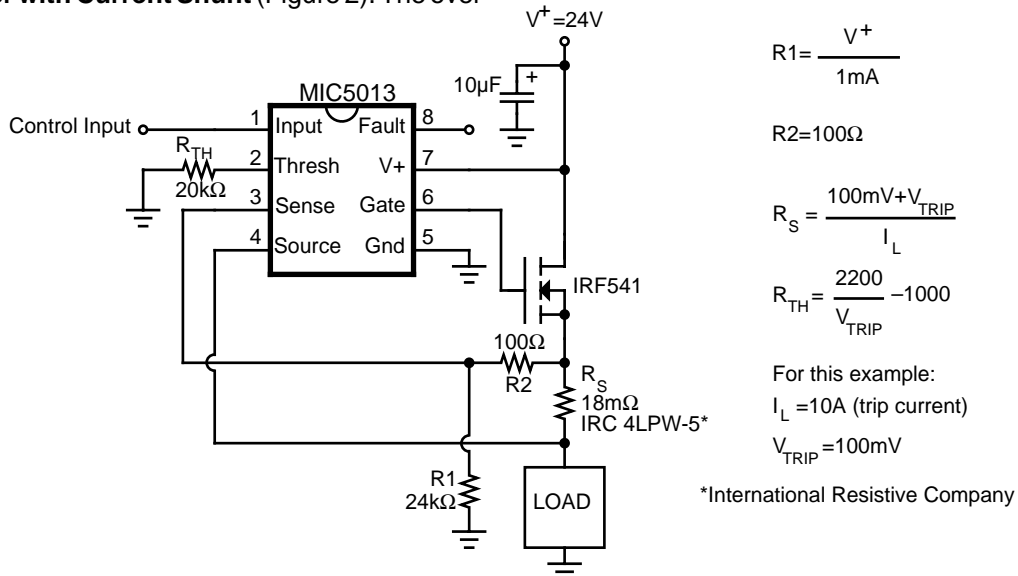
current comparator monitors R_S and trips if I_L × R_S exceeds V_{TRIP}. R is selected to produce the desired trip voltage.

As a guideline, keep V_{TRIP} within the limits of 100mV and 500mV (R_{TH} = 3.3kΩ to 20kΩ). Thresholds at the high end offer the best noise immunity, but also compromise switch drop (especially in low voltage applications) and power dissipation.

The trip current is set higher than the maximum expected load current—typically twice that value. Trip point accuracy is a function of resistor tolerances, comparator offset (only a few millivolts), and threshold bias voltage (V₂). The values shown in Figure 2 are designed for a trip current of 20 amperes. It is important to ground pin 4 at the current shunt R_S, to eliminate the effects of ground resistance.

A key advantage of the low-side topology is that the load supply is limited only by the MOSFET BVDSS rating. Clamping may be required to protect the MOSFET drain terminal from inductive switching transients. The MIC5013

Low-Side Driver with Current Shunt (Figure 2). The over-



$$R1 = \frac{V^+}{1mA}$$

$$R2 = 100\Omega$$

$$R_S = \frac{100mV + V_{TRIP}}{I_L}$$

$$R_{TH} = \frac{2200}{V_{TRIP}} - 1000$$

For this example:

$$I_L = 10A \text{ (trip current)}$$

$$V_{TRIP} = 100mV$$

*International Resistive Company

Figure 3. High-Side Driver with Current Shunt

Applications Information (Continued)

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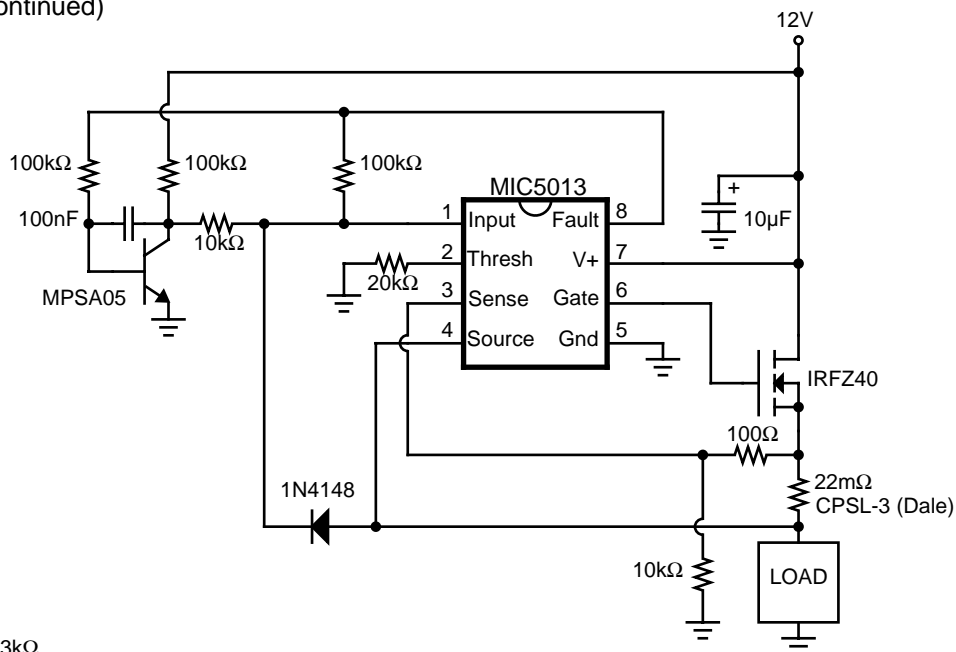


Figure 7. 10-Ampere Electronic Circuit Breaker

lated (100Hz to 20kHz), or where it is energized for only a short period of time ($\leq 25\text{ms}$). If the load is left energized for a long period of time ($> 25\text{ms}$), the bootstrap capacitor will discharge and the MIC5013 supply pin will fall to $V+ = V_{DD} - 1.4$. Under this condition pins 3 and 4 will be held above $V+$ and may false trigger the over-current circuit. A larger capacitor will lengthen the maximum “on” time; $1000\mu\text{F}$ will hold the circuit up for 2.5 seconds, but requires more charge time when the circuit is turned off. The optional Schottky barrier diode improves turn-on time on supplies of less than 10V.

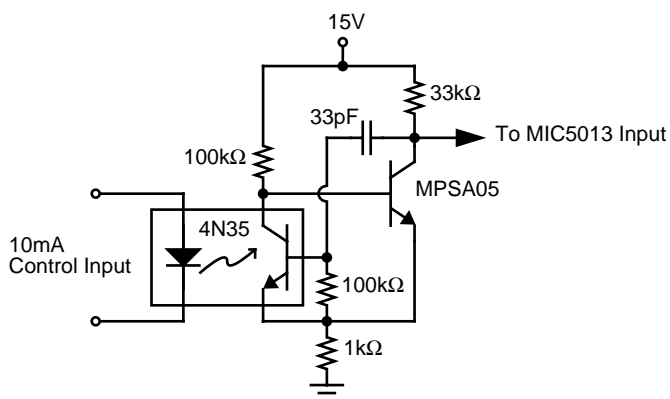


Figure 8. Improved Opto-Isolator Performance

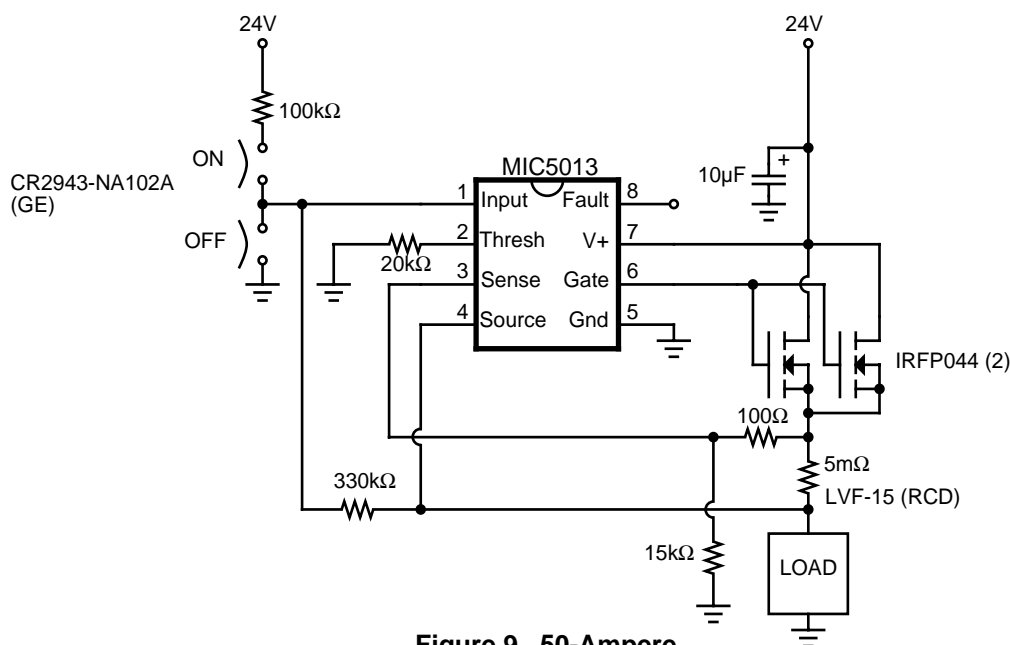


Figure 9. 50-Ampere Industrial Switch

Applications Information (Continued)

The top-side driver is based on the bootstrapped circuit of Figure 6, and cannot be switched on indefinitely. The bootstrap capacitor (1µF) relies on being pulled to ground by the bottom-side output to recharge. This limits the maximum duty cycle to slightly less than 100%.

Two of these circuits can be connected together to form an H-bridge. If the H-bridge is used for locked antiphase control, no special considerations are necessary. In the case of sign/magnitude control, the “sign” leg of the H-bridge should be held low (PWM input held low) while the other leg is driven by the magnitude signal.

If current feedback is required for torque control, it is available in chopped form at the bottom-side driver's 22 mΩ current-sensing resistor.

Time-Delay Relay (Figure 12). The MIC5013 forms the basis of a simple time-delay relay. As shown, the delay commences when power is applied, but the 100 kΩ/1N4148 could be independently driven from an external source such

as a switch or another high-side driver to give a delay relative to some other event in the system.

Hysteresis has been added to guarantee clean switching at turn-on. Note that an over-current condition latches the relay in a safe, OFF condition. Operation is restored by either cycling power or by momentarily shorting pin 1 to ground.

Motor Driver with Stall Shutdown (Figure 13). Tachometer feedback can be used to shut down a motor driver circuit when a stall condition occurs. The control switch is a 3-way type; the “START” position is momentary and forces the driver ON. When released, the switch returns to the “RUN” position, and the tachometer’s output is used to hold the MIC5013 input ON. If the motor slows down, the tach output is reduced, and the MIC5013 switches OFF. Resistor “R” sets the shutdown threshold. If the output current exceeds 30A, the MIC5013 shuts down and remains in that condition until the momentary “RESET” button is pushed. Control is then returned to the START/RUN/STOP switch.

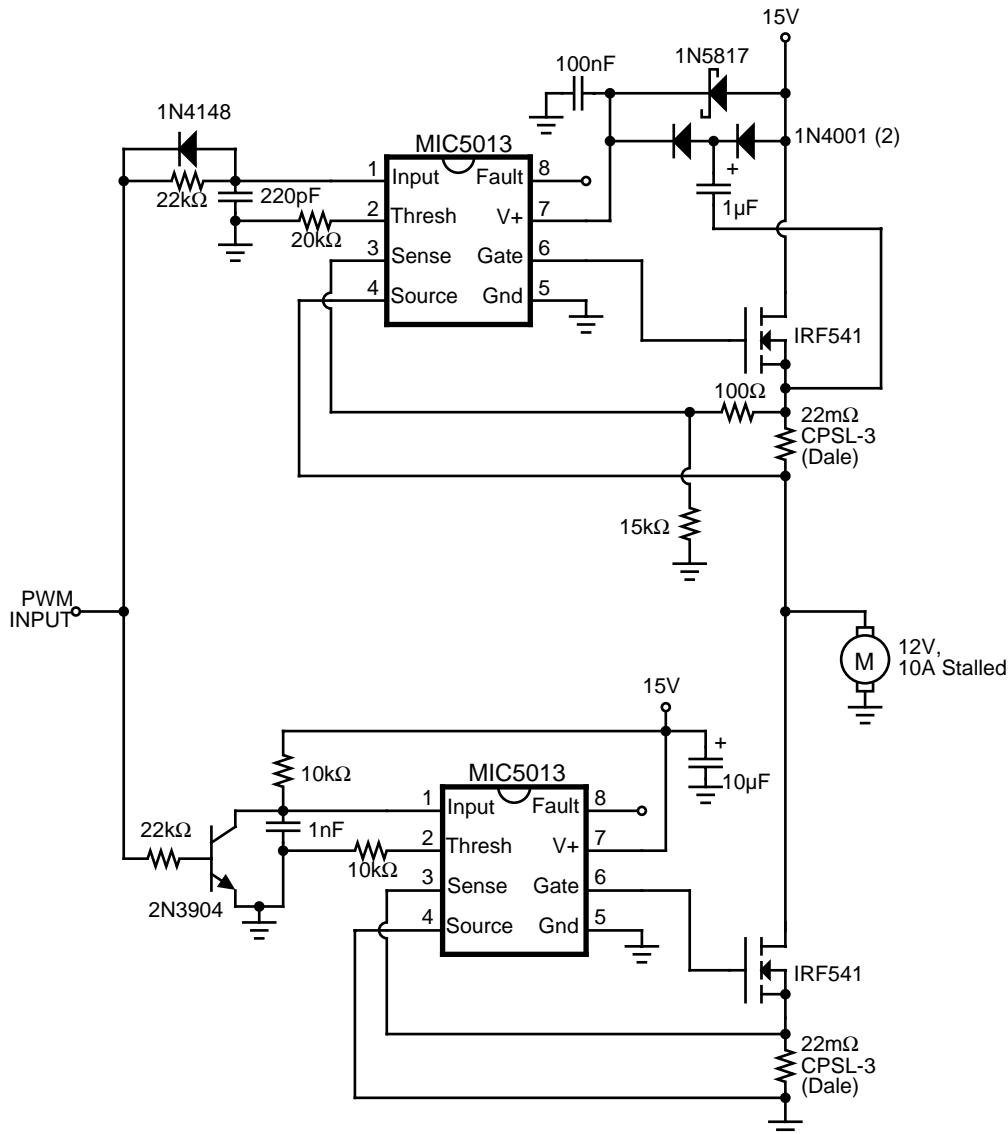


Figure 11. Half-Bridge Motor Driver

Applications Information (Continued)

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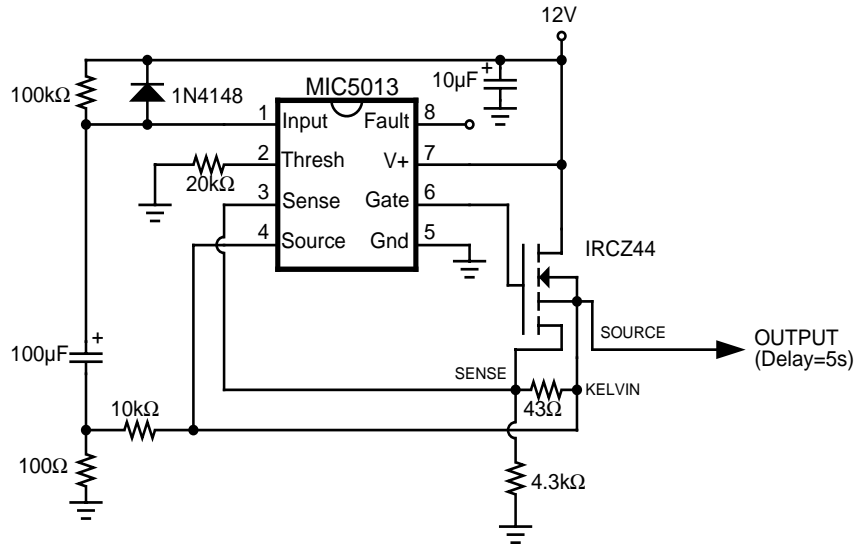


Figure 12. Time-Delay Relay with 30A Over-Current Protection

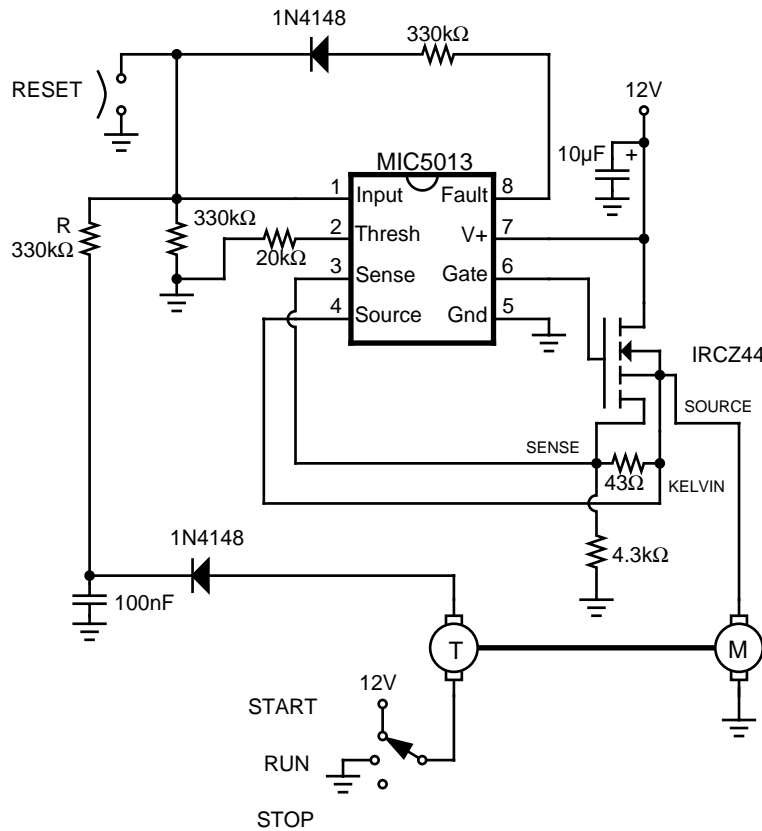


Figure 13. Motor Stall Shutdown

Applications Information (Continued)

Gate Control Circuit

When applying the MIC5010, it is helpful to understand the operation of the gate control circuitry (see Figure 14). The gate circuitry can be divided into two sections: 1) charge pump (oscillator, Q1-Q5, and the capacitors) and 2) gate turn-off switch (Q6).

When the MIC5010 is in the OFF state, the oscillator is turned off, thereby disabling the charge pump. Q5 is also turned off, and Q6 is turned on. Q6 holds the gate pin (G) at ground potential which effectively turns the external MOSFET off.

Q6 is turned off when the MIC5013 is commanded on. Q5 pulls the gate up to supply (through 2 diodes). Next, the charge pump begins supplying current to the gate. The gate accepts charge until the gate-source voltage reaches 12.5V and is clamped by the zener diode.

A 2-output, three-phase clock switches Q1-Q4, providing a quasi-tripling action. During the initial phase Q4 and Q2 are ON. C1 is discharged, and C2 is charged to supply through

Q5. For the second phase Q4 turns off and Q3 turns on, pushing pin C2 above supply (charge is dumped into the gate). Q3 also charges C1. On the third phase Q2 turns off and Q1 turns on, pushing the common point of the two capacitors above supply. Some of the charge in C1 makes its way to the gate. The sequence is repeated by turning Q2 and Q4 back on, and Q1 and Q3 off.

In a low-side application operating on a 12 to 15V supply, the MOSFET is fully enhanced by the action of Q5 alone. On supplies of more than approximately 14V, current flows directly from Q5 through the zener diode to ground. To prevent excessive current flow, the MIC5010 supply should be limited to 15V in low-side applications.

The action of Q5 makes the MIC5013 operate quickly in low-side applications. In high-side applications Q5 precharges the MOSFET gate to supply, leaving the charge pump to carry the gate up to full enhancement 10V above supply. Bootstrapped high-side drivers are as fast as low-side drivers since the chip supply is boosted well above the drain at turn-on.

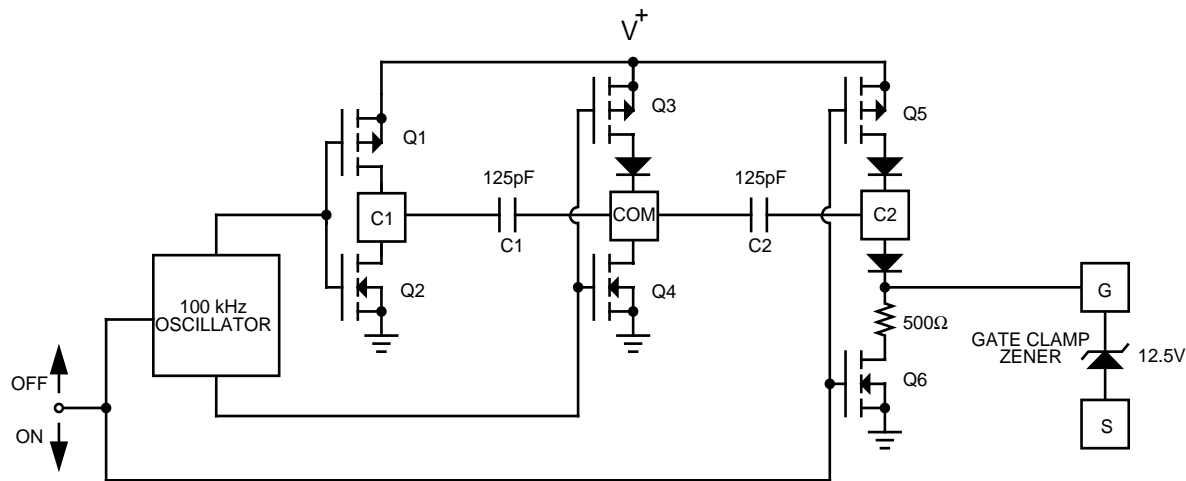
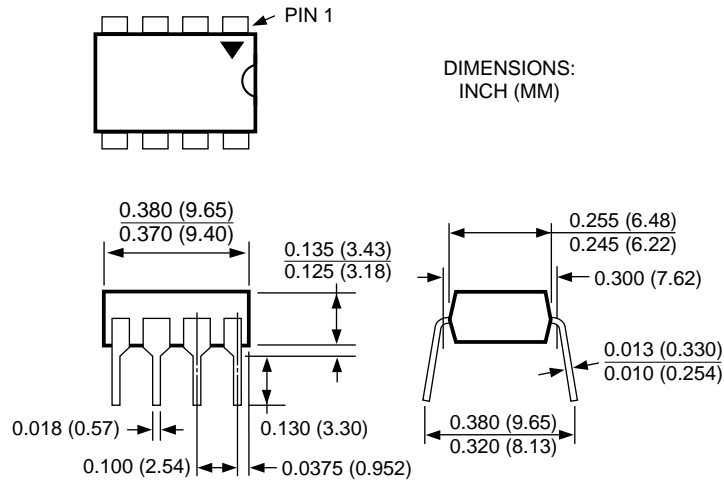


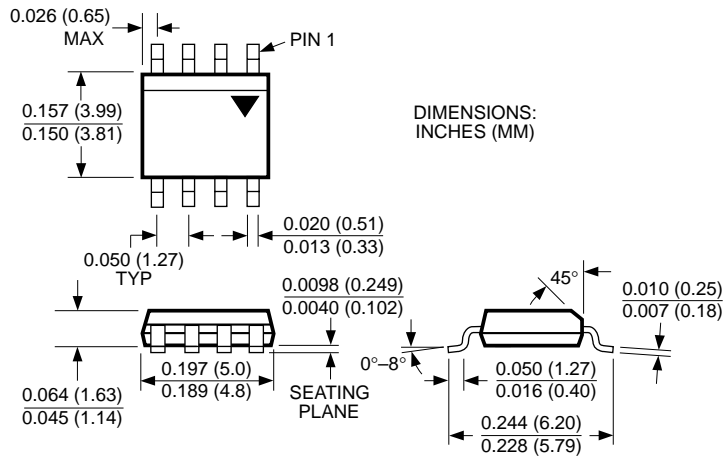
Figure 14. Gate Control Circuit Detail

Package Information

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8-Pin Plastic DIP (N)



8-Pin SOP (M)

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