

[查询"21041"供应商](#)

Digital Semiconductor 21041 PCI Ethernet LAN Controller

Data Sheet

Order Number: EC-QAWWB-TE

Revision/Update Information: This document supersedes the
*DECchip 21041 PCI Ethernet LAN
Controller Data Sheet (EC-QAWWA-TE).*

Digital Equipment Corporation
Maynard, Massachusetts



[查询"21041"供应商](#)

Important Notice

As of May 17, 1998, Digital Equipment Corporation's StrongARM, PCI Bridge, and Networking component businesses, along with the chip fabrication facility in Hudson, Massachusetts, were acquired by Intel Corporation and transferred to Intel Massachusetts, Inc. As a result of this transaction, certain references to web sites, telephone numbers, and fax numbers have changed in the documentation. This information will be updated in the next version of this manual. Copies of documents that have an ordering number and are referenced in this document, or other Intel literature may be obtained by calling **1-800-332-2717** or by visiting Intel's website for developers at:

<http://developer.intel.com>

The Intel Massachusetts Customer Technology Center continues to service your StrongARM Product, Bridge Product, and Network Product technical inquiries. Please use the following information lines for support:

For documentation and general information:

Intel Massachusetts Information Line

United States:	1-800-332-2717
Outside United States:	1-303-675-2148
Electronic mail address:	techdoc@intel.com

For technical support:

Intel Massachusetts Customer Technology Center

Phone (U.S. and international):	1-978-568-7474
Fax:	1-978-568-6698
Electronic mail address:	techsup@intel.com

February 1996

While Digital believes the information included in this publication is correct as of the date of publication, it is subject to change without notice.

Digital Equipment Corporation makes no representations that the use of its products in the manner described in this publication will not infringe on existing or future patent rights, nor do the descriptions contained in this publication imply the granting of licenses to make, use, or sell equipment or software in accordance with the description.

© Digital Equipment Corporation 1996. All rights reserved.
Printed in U.S.A.

DEC, DECchip, Digital, Digital Semiconductor, and the DIGITAL logo are trademarks of Digital Equipment Corporation.

Digital Semiconductor is a Digital Equipment Corporation business.

IEEE is a registered trademark of The Institute for Electrical and Electronics Engineers, Inc.
MicroWire is a registered trademark of BankAmerica Corporation.

All other trademarks and registered trademarks are the property of their respective owners.

Contents

1	Digital Semiconductor 21041 Overview	1
1.1	General Description	1
1.2	Microarchitecture	2
1.3	Features	4
2	Pinout	6
2.1	Pinout and Pin Descriptions	6
2.2	Quick Pin Reference	8
2.3	Pin Reference Tables	19
2.4	Signal Grouping by Function	20
3	Electrical and Environmental Specifications	22
3.1	Voltage Limit Ratings	22
3.2	Temperature Limit Ratings	23
3.3	Supply Current and Power Dissipation	24
3.4	PCI Bus Electrical Specifications	24
3.4.1	PCI I/O Voltage Specifications	24
3.4.2	PCI Reset	27
3.4.3	PCI Clock Specifications	28
3.4.4	Other PCI Signals	29
3.5	AUI and Twisted-Pair dc Specifications	31
3.6	Serial Interface Attachment Specifications	32
3.6.1	Serial Clock dc Specifications	32
3.6.2	Serial Clock Timing	33
3.6.3	Internal SIA Mode AUI Timing—Transmit	34
3.6.4	Internal SIA Mode AUI Timing—Receive	35
3.6.5	Internal SIA Mode AUI Timing—Collision	35
3.6.6	Internal SIA Mode 10BASE-T Interface Timing—Transmit	37
3.6.7	Internal SIA Mode 10BASE-T Interface Timing—Receive	39
3.6.8	Internal SIA Mode 10BASE-T Interface Timing—Idle Link Pulse	40

3.7	Joint Test Action Group—Test Access Port	41
3.7.1	JTAG dc Specifications	41
3.7.2	JTAG Boundary-Scan Timing	41
3.8	Boot ROM, Serial ROM, and LED Port Specification	43
3.9	LED Timing	44
3.10	Boot ROM Port Timing	45
3.10.1	Boot ROM Read Timing	45
3.10.2	Boot ROM Write Timing	47
3.11	Ethernet ID Port Serial ROM Timing	49
3.12	External Register Timing	50
4	Mechanical Specifications	52

Figures

1	21041 Microarchitecture	3
2	21041 Pinout Diagram (Top View)	7
3	PCI Reset Timing Diagram	27
4	PCI Clock Timing Diagram	28
5	Timing Diagram for Other PCI Signals	29
6	Serial Clock (XTAL) Timing Diagram	33
7	Internal SIA Mode AUI Timing Diagram—Transmit	34
8	Internal SIA Mode AUI Timing Diagram—Receive	35
9	Internal SIA Mode AUI Timing Diagram—Collision	35
10	Internal SIA Mode 10BASE-T Interface Timing Diagram—Transmit	37
11	Internal SIA Mode 10BASE-T Interface Timing Diagram—Receive	39
12	Internal SIA Mode 10BASE-T Interface Timing Diagram—Idle Link Pulse	40
13	JTAG Boundary-Scan Timing Diagram	42
14	LED Signal Stretching Function Timing Diagram	44
15	Boot ROM Read Timing Diagram	45
16	Boot ROM Write Timing Diagram	47
17	Ethernet ID Port Timing Diagram	49
18	External Register Read Timing Diagram	50
19	External Register Write Timing Diagram	50
20	Mechanical Layout of the 21041	53

Tables

1	Index to Pinout Tables	6
2	21041 Pin Cross Reference by Logic Signal	8
3	21041 Pin Cross Reference by Power Signal	10
4	Quick Pin Reference	11
5	Input Pin Reference	19
6	Output Pin Reference	20
7	Input/Output Pin Reference	20
8	Signal Functions	21
9	Voltage Limit Ratings	22
10	Temperature Limit Ratings	23
11	Supply Current and Power Dissipation	24
12	I/O Voltage Specifications for 5.0-Volt Levels	25
13	I/O Voltage Specifications for 3.3-Volt Levels	26
14	PCI Reset Timing Specifications	27
15	PCI Clock Timing Specifications	28
16	Other PCI Signal Timing Specifications	30
17	AUI and Twisted-Pair dc Specifications	31
18	Serial Clock (XTAL) dc Specifications	32
19	Serial Clock (XTAL) Timing Specifications	33
20	Internal SIA Mode AUI Timing Specifications—Transmit . . .	34
21	Internal SIA Mode AUI Timing Specifications—Receive and Collision	36
22	Internal SIA Mode 10BASE-T Interface Timing Specifications—Transmit	38
23	Internal SIA Mode 10BASE-T Interface Timing Specifications—Receive	39
24	Internal SIA Mode 10BASE-T Interface Timing Specifications—Idle Link Pulse	40
25	JTAG dc Specifications	41
26	JTAG Interface Signal Timing Specifications	42
27	Boot ROM, Serial ROM, and LED Port dc Specifications	43
28	LED Signal Stretching Function Timing Specifications	44
29	Boot ROM Read Timing Specifications	46
30	Boot ROM Write Timing Specifications	48
31	Ethernet ID Port Timing Specifications	49
32	External Register Timing Specifications	51

[查询"21041"供应商](#)

33	120-Pin PQFP Package Dimensions	52
----	---	----

1 Digital Semiconductor 21041 Overview

The Digital Semiconductor 21041 PCI Ethernet LAN Controller (21041) provides a direct interface connection to the peripheral component interconnect (PCI) bus and adapts easily to most other standard buses. The 21041 provides a direct Ethernet connection to the twisted-pair (TP) interface and attachment unit interface (AUI).

The 21041 operates in two modes: mode 0 and mode 1. In mode 0 operation, the 21041 is software compatible with the 21040 and functions as a 21040. In mode 1 operation, the 21041 incorporates enhanced features that are described in this document. For a description of mode 0 operation, refer to the *DECchip 21040 Ethernet LAN Controller for PCI Data Sheet* and the *DECchip 21040 Ethernet LAN Controller for PCI Hardware Reference Manual*.

1.1 General Description

The 21041 interfaces with the PCI using onchip control and status registers (CSRs), and a shared system memory area that is set up mainly during initialization. This minimizes the CPU involvement in the 21041 operation during normal reception and transmission. The 21041 is compliant with the *PCI Local Bus Specification, Revision 2.0* and the *PCI Local Bus Specification, Revision 2.1*. Bus traffic is also minimized by filtering out received runt frames and by automatically retransmitting collided frames without needing to repeat a fetch from system memory.

The 21041 provides a direct interface to a 64KB, 128KB, or 256KB boot ROM. It supports both PCI 3.3-volt and 5.0-volt signaling environments and a power-down mode for energy conservation.

On the network side, the 21041 provides an AUI and a TP interface, enabling a low chip count connection to the two most popular Ethernet interfaces. The 21041 can sustain transmission or reception of minimal-sized, back-to-back packets at full line speed with an interpacket gap (IPG) of 9.6 microseconds. It is also capable of functioning in a full-duplex environment, and it supports IEEE 802.3 autonegotiation algorithm of full-duplex and half-duplex network environments.

1.2 Microarchitecture

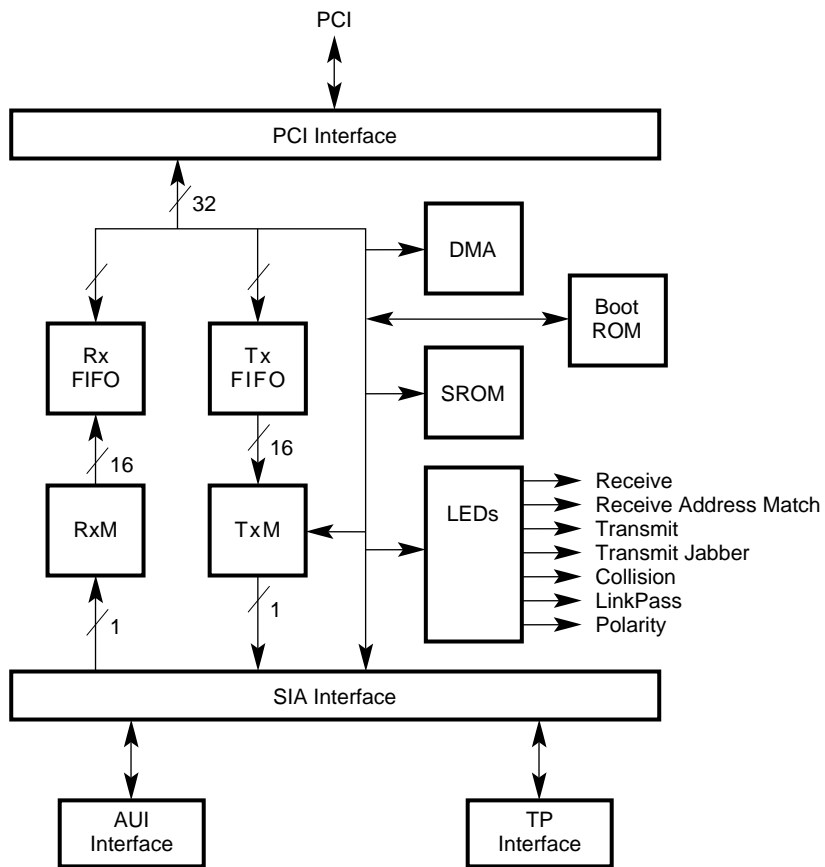
The following list describes the 21041 microarchitecture components, and Figure 1 shows the microarchitecture.

- PCI interface—Includes all interface functions to the PCI bus; handles all interconnect control signals; executes PCI direct memory access (DMA) and I/O transactions.
- DMA—Contains dual receive and transmit controller; supports programmable burst sizes of up to 32 longwords; handles data transfers between system memory and onchip memory.
- FIFOs—Contains dual 256-byte FIFOs for receive and transmit; supports automatic receive packet deletion (for example, runt packets or after a collision) and packet retransmission after a collision on transmit.
- TxM—Handles all CSMA/CD¹ MAC²-level transmit operations and transfers data from transmit FIFO to the serial interface attachment (SIA) for transmission.
- RxM—Handles all CSMA/CD receive operations and transfers the data from the SIA to the receive FIFO.
- SIA—Performs physical layer operations; implements the AUI and 10BASE-T functions, including the Manchester encoder and decoder functions.
- Boot ROM—Includes the required interface to the boot ROM for read and write operations. Accesses to bytes or to longwords (32-bit) are supported.
- SRAM—Provides all interface logic to allow accesses to the external serial ROM.
- LEDs—Contains the logic to detect seven network events and to drive them outside the device for LED display. Also supports two general-purpose LEDs.

¹ Carrier-sense multiple access with collision detection

² Media access control

Figure 1 21041 Microarchitecture



LJ-03988.AI

1.3 Features

The 21041 has the following features:

Note

Asterisks (*) indicate 21041 features that are not available on the 21040.

- Offers a single-chip Ethernet controller for PCI local bus
 - Provides a direct interface connection to PCI bus
 - Implements pinout order as recommended by the *PCI Local Bus Specification* to allow board layout within trace-length restriction*
 - Contains onchip integrated attachment unit interface (AUI) port and a 10BASE-T transceiver
 - Compliant with PCI local bus specification
 - Support for subvendor ID
- Implements the same architecture as 21040 to allow using unified drivers*
- Supports full-duplex operation and IEEE 802.3 autonegotiation algorithm of full-duplex and half-duplex environments*
- Provides upgradable boot ROM interface (FLASH or EEPROM) of 64KB, 128KB, or 256KB*
- Contains serial ROM interface (suitable also for MicroWire EEPROM) for Ethernet ID address and, optionally, other system parameters*
 - Implements automatic loading of subsystem vendor ID and subsystem ID from serial ROM to distinguish between different adapters based on the 21041 chip*
- Provides clock speed up to 33 megahertz, with no wait states on PCI master operation
- Enables powerful onchip DMA with programmable burst sizes of up to 32 longwords providing for low CPU utilization
- Implements unique, patent-pending intelligent arbitration between DMA channels preventing underflow or overflow and is optimized for full-duplex operation
- Incorporates a 16-bit, general-purpose timer*

- Contains two large (256-byte) independent receive and transmit FIFOs
- Supports either big or little endian byte ordering for buffers and descriptors
- Implements JTAG-compatible test access port with boundary-scan pins
- Provides full support of IEEE 802.3, ANSI 8802-3, and Ethernet standards
- Offers a unique, patented solution to Ethernet capture-effect problem
- Contains a variety of flexible address filtering modes
 - 16 perfect addresses
 - 512 hash-filtered, multicast addresses and one perfect address
 - 512 hash-filtered, physical addresses and multicast addresses
 - Inverse perfect filtering
- Supports seven LEDs: Receive, Receive Address Match, Transmit, Transmit Jabber, Collision, LinkPass, and Polarity.* It also supports two general-purpose LEDs.*
- Enables automatic detection and correction of 10BASE-T receive polarity
- Enables full autosensing between 10BASE-T, 10BASE2, and 10BASE5 ports*
- Provides external and internal loopback capability
- Provides a software-controllable, power-saving mode*
- Contains 3.3-volt complementary metal-oxide semiconductor (CMOS) device which interfaces to 5.0-volt or 3.3-volt logic
- Supports both PCI 5.0-volt and 3.3-volt signaling environments*

2 Pinout

The tables in this section provide a description of the pins and their respective signal definitions. Table 1 lists the tables in this section.

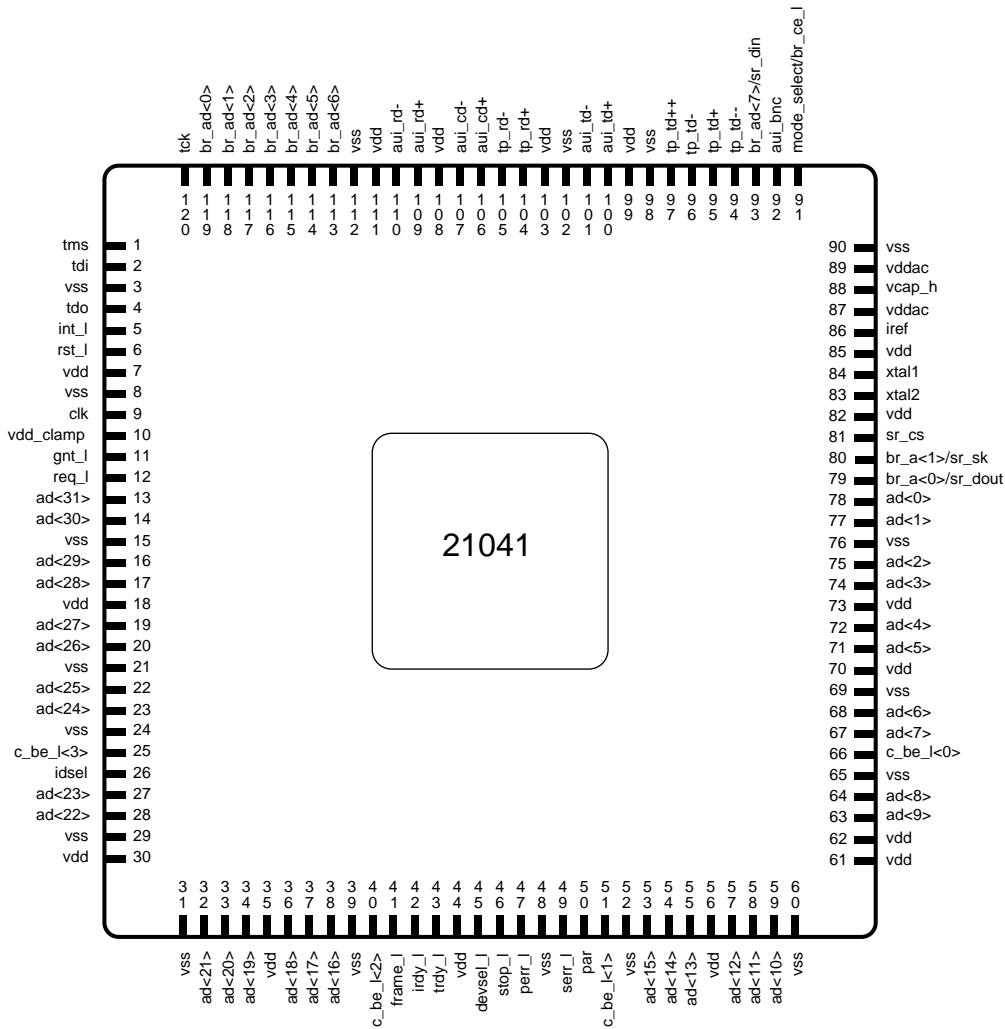
Table 1 Index to Pinout Tables

For this information . . .	Refer to . . .
Pin cross reference by logic signal	Table 2
Pin cross reference by power signal	Table 3
Quick pin reference	Table 4
Input pin reference	Table 5
Output pin reference	Table 6
Input/output pin reference	Table 7
Signal functions	Table 8

2.1 Pinout and Pin Descriptions

The 21041 is housed in the 120-pin plastic quad flat pack (PQFP). The 21041 uses all pins. Figure 2 shows the 21041 pinout.

Figure 2 21041 Pinout Diagram (Top View)



LJ-03989.AI

2.2 Quick Pin Reference

Table 2 provides a pin cross reference listed by logic signal name. Table 3 provides a pin cross reference listed by power signal name. Table 4 is a quick pin reference that defines the logic signals.

Table 2 21041 Pin Cross Reference by Logic Signal

Signal	Location	Signal	Location
ad<0>	78	ad<24>	23
ad<1>	77	ad<25>	22
ad<2>	75	ad<26>	20
ad<3>	74	ad<27>	19
ad<4>	72	ad<28>	17
ad<5>	71	ad<29>	16
ad<6>	68	ad<30>	14
ad<7>	67	ad<31>	13
ad<8>	64	au_i_bnc	92
ad<9>	63	au_i_cd-	107
ad<10>	59	au_i_cd+	106
ad<11>	58	au_i_rd-	110
ad<12>	57	au_i_rd+	109
ad<13>	55	au_i_td-	101
ad<14>	54	au_i_td+	100
ad<15>	53	br_a<0>/sr_dout	79
ad<16>	38	br_a<1>/sr_sk	80
ad<17>	37	br_ad<0>	119
ad<18>	36	br_ad<1>	118
ad<19>	34	br_ad<2>	117
ad<20>	33	br_ad<3>	116
ad<21>	32	br_ad<4>	115
ad<22>	28	br_ad<5>	114
ad<23>	27	br_ad<6>	113

(continued on next page)

Table 2 (Cont.) 21041 Pin Cross Reference by Logic Signal

Signal	Location	Signal	Location
br_ad<7>/sr_din	93	serr_l	49
c_be_l<0>	66	sr_cs	81
c_be_l<1>	51	stop_l	46
c_be_l<2>	40	tck	120
c_be_l<3>	25	tdi	2
clk	9	tdo	4
devsel_l	45	tms	1
frame_l	41	tp_rd-	105
gnt_l	11	tp_rd+	104
idsel	26	tp_td-	96
int_l	5	tp_td- -	94
irdy_l	42	tp_td+	95
iref	86	tp_td+ +	97
mode_select /br_ce_l	91	trdy_l	43
par	50	vcap_h	88
perr_l	47	xtal1	84
req_l	12	xtal2	83
rst_l	6		

Table 3 21041 Pin Cross Reference by Power Signal

Signal	Location	Signal	Location
vdd (3.3 V)	7, 18, 30, 35	vss (GND)	3, 8, 15, 21
	44, 56, 61, 62		24, 29, 31, 39
	70, 73, 82, 85		48, 52, 60, 65
	99, 103, 108, 111		69, 76, 90, 98
			102, 112
vdd_clamp	10		
vddac (3.3 V)	87, 89		

Table 4 lists a functional description of each of the 21041 signals. These signals are listed alphabetically. The functional grouping of each pin is listed in Section 2.4.

The following terms describe the 21041 pinout.

- **Address phase**
The address and appropriate bus command are driven during this cycle.
- **Data phase**
Data and the appropriate byte enable code are driven during this cycle.
- **_l**
All pin names with the **_l** suffix are only asserted low.

Note

The following list describes the abbreviations used in the tables in this section.

- I = Input
 - O = Output
 - I/O = Input/output
 - O/D = Open drain
-

Table 4 Quick Pin Reference

Signal	Type	Pin Number	Description
ad<31:00>	I/O	See Figure 2.	32-bit multiplexed PCI address and data lines. Address and data bits are multiplexed on the same pins. During the first clock cycle of a transaction, ad<31:00> contain a physical byte address (32 bits). During subsequent clock cycles, ad<31:00> contain data. A 21041 bus transaction consists of an address phase followed by one or more data phases. The 21041 supports both read and write bursts. Little and big endian byte ordering can be used.
au_i_bnc	I/O	92	Attachment unit interface and BNC select line. When asserted high, the 10BASE5 (AUI) mode is selected. When asserted low, the 10BASE2 (BNC) mode is selected. This output pin is used mainly to enable the external BNC transceiver in 10BASE2 mode. This pin is an input pin in mode 0.
au_i_cd-	I	107	Attachment unit interface receive collision differential negative data.
au_i_cd+	I	106	Attachment unit interface receive collision differential positive data.
au_i_rd-	I	110	Attachment unit interface receive differential negative data.
au_i_rd+	I	109	Attachment unit interface receive differential positive data.
au_i_td-	O	101	Attachment unit interface transmit differential negative data.
au_i_td+	O	100	Attachment unit interface transmit differential positive data.

(continued on next page)

Table 4 (Cont.) Quick Pin Reference

Signal	Type	Pin Number	Description
br_a<0>/ sr_dout	I/O	79	<p>Boot ROM address line bit 0. In a 256KB configuration, this pin also carries in two consecutive address cycles, boot ROM address bits 16 and 17.</p> <p>When the 21041 operates with the serial ROM, serial ROM data out (sr_dout) shifts the Ethernet identification address from the serial ROM device into the 21041.</p> <p>During operation with the external register, this pin is used for read and write control.</p>
br_a<1>/ sr_sk	O	80	<p>Boot ROM address line bit 1. This pin also latches the boot ROM address and control lines by the two external latches.</p> <p>When the 21041 operates with the serial ROM, sr_sk provides the serial ROM clock.</p>
br_ad<6:0>	I/O	See Figure 2.	<p>Boot ROM address and data multiplexed lines bits 6 through 0. In two consecutive address cycles, these lines contain the boot ROM address bits 6 through 2, oe_1, and we_1 in the first cycle; and these lines contain boot ROM address bits 14 through 8 in the second cycle. During the data cycles, bits 6 through 0 contain data.</p> <p>The boot ROM address bits 6 through 0 can be connected directly to seven network event LEDs: Transmit, Collision, Receive Address Matching, Receive, TP Polarity, Transmit Jabber, and LinkPass respectively.</p> <p>During operation with the external register, these lines are used to carry data bits 6 through 0 to and from the external register.</p>

(continued on next page)

Table 4 (Cont.) Quick Pin Reference

Signal	Type	Pin Number	Description
br_ad<7>/ sr_din	I/O	93	<p>Boot ROM address and data multiplexed line bit 7. In two consecutive address cycles, this pin carries boot ROM address bits 7 and 15. During the data phase, it contains data.</p> <p>When the 21041 operates with the serial ROM, serial ROM data in (sr_din) serially shifts the Ethernet identification address from the 21041 into the serial ROM device.</p> <p>During operation with the external register, this pin is used to carry data bit 7 to and from the external register.</p> <p>When mode 0 (21040) is selected, this pin must be tied to vss.</p>
c_be_l<3:0>	I/O	See Figure 2.	<p>Bits 0 through 3 of the bus command and byte enable lines. Bus command and byte enable are multiplexed on the same PCI pins.</p> <p>During the address phase of the transaction, c_be_l<3:0> provide the bus command.</p> <p>During the data phase, c_be_l<3:0> provide the byte enable. The byte enable determines which byte lines carry valid data. For example, c_be_l<0> applies to byte 0, and c_be_l<3> applies to byte 3.</p> <p>In all master and I/O operations, c_be_l<3:0> contain a value equal to a longword hexadecimal value of 0. In configuration operations, c_be_l<3:0> can contain any value; 21041 supports byte, word, and longword operations.</p>
clk	I	9	<p>The clock provides the timing for the 21041-related bus transactions. All the other bus signals are sampled on the rising edge of clk. The clock range is between 16 megahertz and 33 megahertz.</p>

(continued on next page)

Table 4 (Cont.) Quick Pin Reference

Signal	Type	Pin Number	Description
devsel_1	I/O	45	The 21041 asserts device select when it is the target of the current bus access. When the 21041 is the initiator of the current bus access, it expects the target to assert devsel_1 within 5 bus cycles, confirming the access. To accomplish this, the 21041 asserts this signal in a medium speed (within two bus cycles). If the target does not assert devsel_1 within the required bus cycles, then the 21041 aborts the cycle.
frame_1	I/O	41	Frame is driven by the 21041 (bus initiator) to indicate the beginning and duration of an access. When frame_1 asserts, it indicates the beginning of a bus transaction. While frame_1 is asserted, data transfers continue. When frame_1 is deasserted, it indicates that the next data phase is the final data phase transaction.
gnt_1	I	11	Bus grant asserts to indicate to the 21041 that access to the bus is granted.
idsel	I	26	Initialization device select asserts to act as a chip select during configuration read or write transactions.
int_1	O/D	5	<p>Interrupt request asserts when one of the appropriate bits of CSR5 sets and causes an interrupt, provided that the corresponding mask bit in CSR7 is not asserted. The int_1 deasserts by writing a 1 into the appropriate CSR5 bit.</p> <p>If more than one interrupt bit is asserted in CSR5, then the host clears only the interrupt bit that was acknowledged, int_1 deasserts for one cycle and then asserts again. This process continues until all interrupts are acknowledged.</p> <p>When deasserted, this pin should be pulled up by an external resistor.</p>

(continued on next page)

Table 4 (Cont.) Quick Pin Reference

Signal	Type	Pin Number	Description
irdy_1	I/O	42	<p>Initiator ready indicates the bus initiator's ability to complete the current data phase of the transaction.</p> <p>A data phase is completed on any clock when both irdy_1 and target ready (trdy_1) are asserted. Wait cycles are inserted until both irdy_1 and trdy_1 are asserted together.</p> <p>When the 21041 is the bus initiator, irdy_1 is asserted during write operations to indicate that valid data is present on ad<31:00>. During read operations, the 21041 asserts irdy_1 to indicate that it is ready to accept data.</p>
iref	I	86	<p>Current reference input for the analog phase-locked loop (PLL) logic.</p>
mode_select/ br_ce_1	I/O	91	<p>Selects either mode 0 (21040) or mode 1 (21041) operation. When this pin is tied to VSS, mode 0 operation is selected. When this pin is not connected (internally pulled up), mode 1 operation is selected. When a hardware or software reset is detected, the 21041 senses this input and sets the mode of operation accordingly.</p> <p>When mode 1 operation is selected, this pin changes its functionality, and it is actually the boot ROM or the external register chip enable (br_ce_1) output pin.</p>
par	I/O	50	<p>Parity is calculated by the 21041 as an even parity bit for the ad<31:00> and c_be_1<3:0> lines.</p> <p>During address and data phases, par is calculated on all the ad and c_be_1 lines whether or not any of these lines carry meaningful information.</p>

(continued on next page)

Table 4 (Cont.) Quick Pin Reference

Signal	Type	Pin Number	Description
perr_l	I/O	47	<p>Parity error asserts when a data parity error is detected.</p> <p>When the 21041 is the bus initiator and a parity error is detected, the 21041 asserts both CSR5 bit 13 (system error) and CFCS bit 9 (serr_l enable) and completes the current data burst transaction, then stops its operation. After the host clears the system error, the 21041 continues its operation.</p> <p>When the 21041 is the bus target and a parity error is detected, the 21041 asserts perr_l.</p>
req_l	O	12	<p>Bus request is asserted by the 21041 to indicate to the bus arbiter that it wants to use the bus.</p>
rst_l	I	6	<p>Resets the 21041 to its initial state. This signal must be asserted for at least 10 active PCI clock cycles. When in the reset state, all PCI port output pins are put into tristate and all open drain (O/D) signals are floated.</p>
serr_l	O/D	49	<p>If an address parity error is detected and CFCS bit 31 (detected parity error) is enabled, then 21041 asserts both serr_l (system error) and CFCS bit 30 (signal system error).</p> <p>When an address parity error is detected, system error asserts two clocks after the failing address.</p> <p>When deasserted, this pin should be pulled up by an external resistor.</p>
sr_cs	O	81	<p>Serial ROM chip select asserts when the 21041 accesses the serial ROM.</p>
stop_l	I/O	46	<p>Stop indicator indicates that the current target is requesting the bus initiator to stop the current transaction.</p> <p>The 21041 responds to the assertion of stop_l when it is the bus initiator, either to disconnect, retry, or abort.</p>

(continued on next page)

Table 4 (Cont.) Quick Pin Reference

Signal	Type	Pin Number	Description
tck	I	120	JTAG clock shifts state information and test data into and out of the 21041 during JTAG test operations.
tdi	I	2	JTAG data in is used to serially shift test data and instructions into the 21041 during JTAG test operations.
tdo	O	4	JTAG data out pin is used to serially shift test data and instructions out of the 21041 during JTAG test operations.
tms	I	1	JTAG test mode select controls the state operation of JTAG testing in the 21041.
tp_rd-	I	105	Twisted-pair negative differential receive data.
tp_rd+	I	104	Twisted-pair positive differential receive data.
tp_td- tp_td- -	O	See Figure 2.	Twisted-pair negative differential transmit data. The positive and negative differential transmit data outputs are resistively combined outside the 21041 with equalization to compensate for intersymbol interference on the twisted-pair medium.
tp_td+ tp_td+ +	O	See Figure 2.	Twisted-pair positive differential transmit data. The positive and negative differential transmit data outputs are resistively combined outside the 21041 with equalization to compensate for intersymbol interference on the twisted-pair medium.

(continued on next page)

Table 4 (Cont.) Quick Pin Reference

Signal	Type	Pin Number	Description
trdy_1	I/O	43	<p>Target ready indicates the target agent's ability to complete the current data phase of the transaction.</p> <p>A data phase is completed on any clock when both trdy_1 and initiator ready (irdy_1) are asserted. Wait cycles are inserted until both irdy_1 and trdy_1 are asserted together.</p> <p>When the 21041 is the bus initiator, trdy_1 is asserted by the bus target on the read operation indicating that valid data is present on ad<31:00>. During a write cycle, it indicates that the target is prepared to accept data.</p>
vcap_h	I	88	Capacitor input for analog PLL logic.
vdd	I	See Figure 2.	3.3-volt supply input voltage.
vddac	I	See Figure 2.	3.3-volt supply input for analog PLL logic.
vdd_clamp	I	10	Supplies +5.0 volts or +3.3 volts reference for the clamp logic.
vss	—	See Figure 2.	Ground pin.
xtal1	I	84	Crystal oscillator input.
xtal2	O	83	Crystal feedback output pin used for crystal connections only. If this pin is unused, then do not connect it.

2.3 Pin Reference Tables

There are three pin reference tables:

- Table 5 lists the input pins.
- Table 6 lists the output pins.
- Table 7 lists the input/output pins.

Table 5 Input Pin Reference

Signal	Signal
au_i_cd-	tck
au_i_cd+	tdi
au_i_rd-	tms
au_i_rd+	tp_{rd}-
clk	tp_{rd}+
gnt_l	vcap_h
idsel	vdd
iref	vddac
rst_l	vdd_clamp
	xtal1

Table 6 Output Pin Reference

Signal	Signal
au_i_td-	tdo
au_i_td+	tp_td-
br_a<1>/sr_sk	tp_td- -
int_l	tp_td+
req_l	tp_td+ +
sr_cs	xtal2

Table 7 Input/Output Pin Reference

Signal	Signal
ad<31:00>	irdy_l
au_i_bnc	mode_select/br_ce_l
br_a<0>/sr_dout	par
br_ad<6:0>	perr_l
br_ad<7>/sr_din	serr_l
c_be_l<3:0>	stop_l
devsel_l	trdy_l
frame_l	

2.4 Signal Grouping by Function

Table 8 lists the signals according to their interface function.

Table 8 Signal Functions

Interface	Function	Signal
PCI	Address and data	ad<31:00>
	Arbitration	gnt_l, req_l
	Bus command and byte enable	c_be_l<3:0>
	Control	frame_l, irdy_l, stop_l, trdy_l
	Device select	devsel_l, idsel
	Error reporting	perr_l, serr_l
	Interrupt	int_l
	Parity	par
	System	clk, rst_l
Network connection	Analog PLL logic	iref, vcap_h
	AUI collision data	au_i_cd-, au_i_cd+
	AUI transmit and receive data	au_i_rd-, au_i_rd+, au_i_td-, au_i_td+
	10BASE5/10BASE2 select	au_i_bnc
	Crystal oscillator	xtal1, xtal2
	Twisted-pair transmit and receive data	tp_rd-, tp_rd+, tp_td-, tp_td- -, tp_td+, tp_td+ +
Power and diagnostic	3.3-volt and 5.0-volt supply input	vdd, vddac, vdd_clamp
	Ground	vss
Test access port	JTAG test operations	tck, tdi, tdo, tms
Ethernet ID ROM and boot ROM	Address serial ROM and boot ROM interface	br_ad<7>/sr_din, br_ad<6:0>, sr_cs, br_a<1>/sr_sk, br_a<0>/sr_dout
Chip mode	Select mode 1, 0	mode_select/br_ce_l

3 Electrical and Environmental Specifications

This section contains the electrical and environmental specifications of the 21041. The test conditions for the specified values are as follows unless otherwise indicated:

- Temperature (Ta): 70°C
- Power supply voltage (**vdd**): 3.3 V
- Power supply voltage (**vddac**): 3.3 V
- Reference voltage (**vdd_clamp**): 3.3 V or 5.0 V, depending on the PCI signaling environment
- Ground **vss**: 0 V

3.1 Voltage Limit Ratings

Table 9 lists the voltage limit ratings.

Table 9 Voltage Limit Ratings

Parameter	Minimum	Maximum
Power supply voltage	+3.0 V	+3.6 V
vdd_clamp (5.0 V)	+4.75 V	+5.25 V
vdd_clamp ¹ (3.3 V)	+3.0 V	+3.6 V
ESD protection voltage	—	2000 V

¹In the 3.3-V signaling environment, **vdd_clamp** must not be greater than **vdd** +0.3 V.

Caution

Stresses greater than the maximum or less than the minimum ratings can cause permanent damage to the 21041. Exposure to the maximum or minimum ratings for extended periods of time lessen the reliability of the 21041.

3.2 Temperature Limit Ratings

Table 10 lists the temperature limit ratings.

Table 10 Temperature Limit Ratings

Parameter	Minimum	Maximum
Storage temperature	-55°C	+125°C
Operating temperature	0°C	70°C

Caution

Stresses greater than the maximum or less than the minimum ratings can cause permanent damage to the 21041. Exposure to the maximum or minimum ratings for extended periods of time lessen the reliability of the 21041.

3.3 Supply Current and Power Dissipation

The values in Table 11 are estimates based on a PCI clock frequency of 33 megahertz and a network clock frequency of 10 megahertz.

Table 11 Supply Current and Power Dissipation

Symbol	Conditions	Typical	Maximum	Units
IDD	VDD=3.6 V, Ta=70°C	120	145	mA
Normal power mode	VDD=3.6 V, Ta=70°C	0.43	0.52	W
Snooze power mode ¹	VDD=3.6 V, Ta=70°C	0.23	0.31	W
Sleep power mode ¹	VDD=3.6 V, Ta=70°C	0.20	0.25	W

¹Refer to the *Digital Semiconductor 21041 Ethernet LAN Controller for PCI Hardware Reference Manual* for a description of sleep mode and snooze mode.

3.4 PCI Bus Electrical Specifications

This section contains information about electrical characteristics for the 21041 input and output pins of the PCI.

3.4.1 PCI I/O Voltage Specifications

The 21041 meets the I/O voltage specifications listed in Table 12 and Table 13.

Table 12 I/O Voltage Specifications for 5.0-Volt Levels

Symbol	Parameter	Condition	Minimum	Maximum
Vih	Input high voltage	—	2.0 V	vdd_clamp + 0.5 V
Vil	Input low voltage	—	-0.5 V	0.8 V
Ii ¹	Input leakage current	0.5 V <Vin<2.7 V	—	±20 µA
Voh	Output high voltage	Iout=- 2mA	2.4 V	—
Vol ²	Output low voltage	Iout=3 mA, 6 mA	—	0.55 V
Cin ³	Input Pin Capacitance	—	—	10 pF
Cclk ³	CLK Pin Capacitance	—	5 pF	12 pF
Cidsel ³	IDSEL Pin Capacitance	—	—	8 pF

¹Input leakage currents include high-impedance output leakage for all bidirectional buffers with tristate outputs.

²Signals without pullup resistors must have 3 milliamps low output current. Signals requiring pullup resistors (including **frame_l**, **trdy_l**, **irdy_l**, **devsel_l**, **stop_l**, **serr_l**, and **perr_l**) must have 6 milliamps.

³Parameter design guarantee.

Table 13 I/O Voltage Specifications for 3.3-Volt Levels

Symbol	Parameter	Condition	Minimum	Maximum
Vih	Input high voltage	—	$0.475 \cdot \mathbf{vdd_clamp}$	$\mathbf{vdd_clamp} + 0.5 \text{ V}$
Vil	Input low voltage	—	-0.5 V	$0.325 \cdot \mathbf{vdd_clamp}$
Ii ¹	Input leakage current	$0.0 \text{ V} < V_{in} < \mathbf{vdd_clamp}$	—	$\pm 10 \text{ }\mu\text{A}$
Voh	Output high voltage	$I_{out} = -500 \text{ }\mu\text{A}$	$0.9 \cdot \mathbf{vdd_clamp}$	—
Vol	Output low voltage	$I_{out} = 1500 \text{ }\mu\text{A}$	—	$0.1 \cdot \mathbf{vdd_clamp}$
Cin ²	Input pin capacitance	—	—	10 pF
Cclk ²	CLK pin capacitance	—	5 pF	12 pF
Cidsel ²	IDSEL pin capacitance	—	—	8 pF

¹Input leakage currents include high-impedance output leakage for all bidirectional buffers with tristate outputs.

²Parameter design guarantee.

3.4.2 PCI Reset

PCI reset (**pci_rst**) is an asynchronous signal that must be active for at least 10 PCI clock (**pci_clk**) cycles. Figure 3 shows the PCI reset timing characteristics, and Table 14 lists the PCI reset signal limits.

Figure 3 PCI Reset Timing Diagram

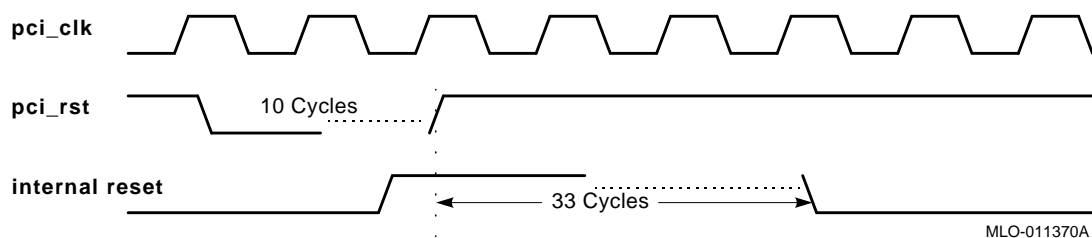


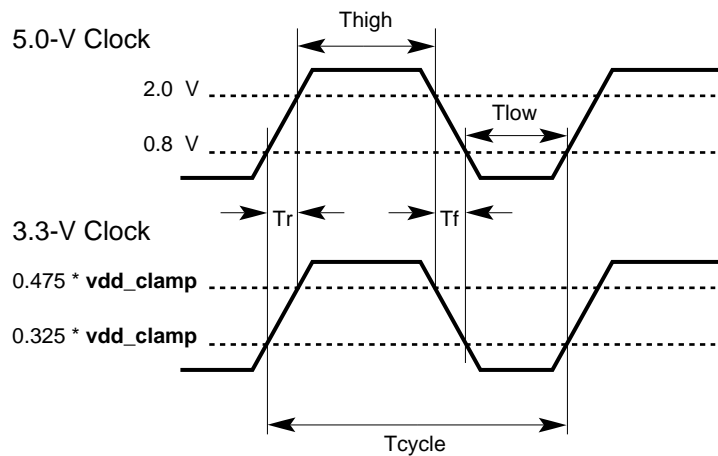
Table 14 PCI Reset Timing Specifications

Symbol	Parameter	Minimum	Maximum	Notes
Trst	pci_rst pulse width	10*Tcycle	—	pci_clk active

3.4.3 PCI Clock Specifications

The standard clock frequency range for the PCI is between 16 megahertz and 33 megahertz. Figure 4 shows the PCI clock timing characteristics and required measurement points for both 5.0-volt and 3.3-volt signaling environments. Table 15 lists the frequency-derived clock specifications.

Figure 4 PCI Clock Timing Diagram



LJ03910A.A15

Table 15 PCI Clock Timing Specifications

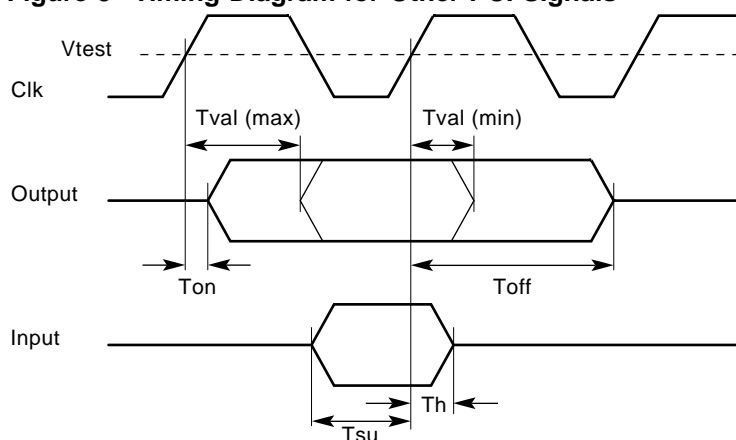
Symbol	Parameter	Minimum	Maximum
Tcycle	Cycle time	30 ns	62.5 ns
Thigh	pci_clk high time	11 ns	—
Tlow	pci_clk low time	11 ns	—
Tr/Tf	pci_clk slew rate ¹	1 V/ns	4 V/ns

¹Rise and fall times are specified in terms of the edge rate measured in V/ns. Parameter design guarantee.

3.4.4 Other PCI Signals

Figure 5 shows the timing diagram characteristics, and Table 16 lists the other PCI signal specifications.

Figure 5 Timing Diagram for Other PCI Signals



LJ04719B.A15

V_{test} is 1.5 volts in the 5-volt signaling environment and is $0.4 * v_{dd_clamp}$ in the 3.3-volt signaling environment.

Table 16 Other PCI Signal Timing Specifications

Symbol	Parameter	Minimum	Maximum
Tval ¹	clk-to-signal valid delay	2 ns	11 ns
Ton ²	Float-to-active delay from clk	2 ns	—
Toff ²	Active-to-float delay from clk	—	28 ns
Tsu	Input signal valid setup time before clk	7 ns	—
Th	Input signal hold time from clk	0 ns	—

¹Load for this measurement is specified in the PCI local bus specification, revisions 2.0 and 2.1.

²Parameter design guarantee.

3.5 AUI and Twisted-Pair dc Specifications

Table 17 lists the dc specifications for the AUI and twisted-pair parts of the SIA.

Table 17 AUI and Twisted-Pair dc Specifications

Symbol	Definition	Conditions	Minimum	Maximum	Units
AUI Pins					
V_{od}^1	Transmit differential output voltage (au_i_td±)	78Ω termination	±550	±1200	mV
V_{odi}^1	Transmit differential output idle voltage (au_i_td±)	78Ω termination	-40	+40	mV
I_{odi}^1	Transmit differential output idle current (au_i_td±)	78Ω termination	-1	+1	mA
V_{asq+}^1	Differential positive squelch threshold (au_i_rd±)	—	175	275	mV
V_{asq-}^1	Differential negative squelch threshold (au_i_rd± and au_i_cd±)	—	-275	-175	mV
V_{odu}^1	Transmit differential output undershoot voltage on return to zero (au_i_td±)	78Ω termination	—	-100	mV
Twisted-Pair Interface Pins					
V_{toh}	Output high voltage (tp_i_td± and tp_i_td±±)	$I_{oh} = -25$ mA	+ 2.5	V_{dd}	V
V_{tol}	Output low voltage (tp_i_td± and tp_i_td±±)	$I_{ol} = 25$ mA	V_{ss}	+ 0.5	V
V_{tsq+}^1	Differential positive squelch threshold (tp_i_rd±)	—	300	520	mV
V_{tsq-}^1	Differential negative squelch threshold (tp_i_rd±)	—	-520	-300	mV
V_{tdif}^1	Differential input voltage range (tp_i_rd±)	—	-3.1	3.1	V
¹ Parameter design guarantee.					

3.6 Serial Interface Attachment Specifications

This section describes the dc specifications and timing limits of the SIA unit.

3.6.1 Serial Clock dc Specifications

Table 18 lists the dc specifications for the two serial clock pins: **xtal1** and **xtal2**.

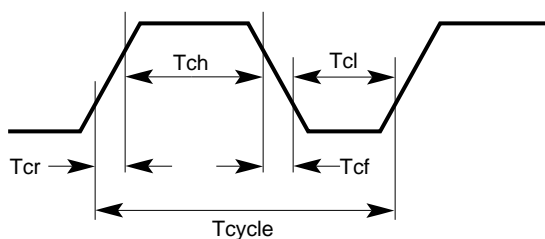
Table 18 Serial Clock (XTAL) dc Specifications

Symbol	Definition	Conditions	Minimum	Maximum	Units
V_{oh}	Output high voltage	$I_{oh} = -4 \text{ mA}$	2.4	—	V
V_{ol}	Output low voltage	$I_{ol} = 4 \text{ mA}$	—	0.4	V
V_{ih}	Input high voltage	—	2.0	—	V
V_{il}	Input low voltage	—	—	0.8	V
I_i	Input leakage current	$0.0 < V_{in} < v_{dd}$	—	± 10	μA

3.6.2 Serial Clock Timing

Figure 6 shows the serial clock (TTL or CMOS) timing characteristics, and Table 19 lists the serial clock timing specifications.

Figure 6 Serial Clock (XTAL) Timing Diagram



LJ-04101.AI

Table 19 Serial Clock (XTAL) Timing Specifications

Symbol	Parameter	Minimum	Maximum
Tcr ¹	Rise time	—	4 ns
Tcf ¹	Fall time	—	4 ns
Tcycle ¹	Cycle time	49.995 ns	50.005 ns
Tch	Clock high time	0.4*Tcycle	0.6*Tcycle
Tcl	Clock low time	0.4*Tcycle	0.6*Tcycle

¹Parameter design guarantee.

3.6.3 Internal SIA Mode AUI Timing—Transmit

Figure 7 shows the internal SIA transmit timing characteristics for the AUI, and Table 20 lists the internal SIA transmit timing limits for the AUI.

Figure 7 Internal SIA Mode AUI Timing Diagram—Transmit

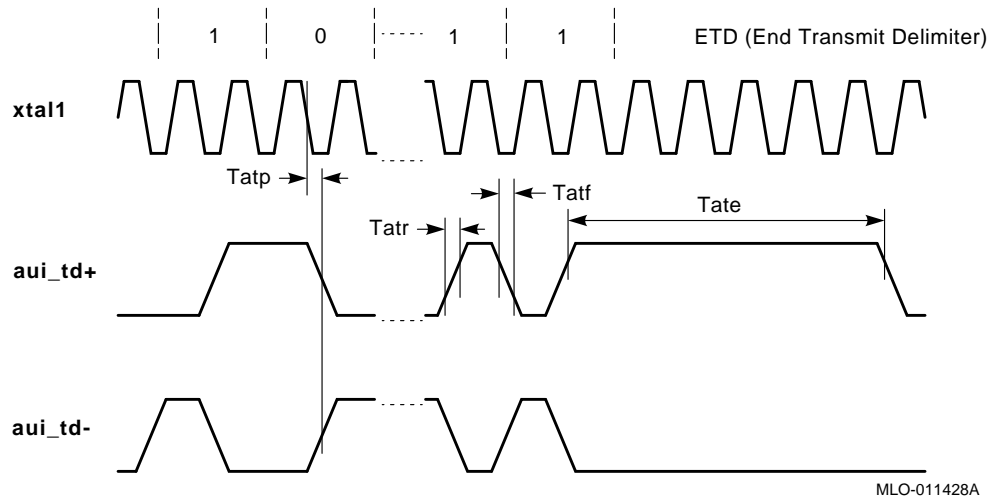


Table 20 Internal SIA Mode AUI Timing Specifications—Transmit

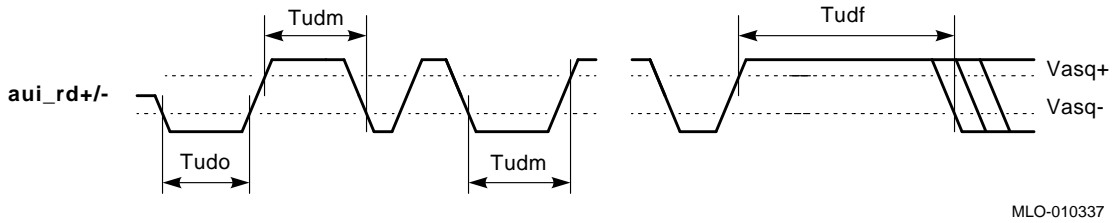
Symbol	Definition	Minimum	Maximum	Units
Tatp	aui_td+ , aui_td- propagation delay from xtal1 fall	—	30	ns
Tatr ¹	aui_td+ , aui_td- rise time	2	8	ns
Tatf ¹	aui_td+ , aui_td- fall time	2	8	ns
Tatm ¹	aui_td+ , aui_td- rise and fall time mismatch (not shown)	—	1	ns
Tate ¹	aui_td± end transmit delimiter length	345	405	ns

¹Parameter design guarantee.

3.6.4 Internal SIA Mode AUI Timing—Receive

Figure 8 shows the internal SIA receive timing characteristics for the AUI, and Table 21 lists the internal SIA receive timing limits for the AUI.

Figure 8 Internal SIA Mode AUI Timing Diagram—Receive



3.6.5 Internal SIA Mode AUI Timing—Collision

Figure 9 shows the internal SIA collision timing characteristics for the AUI, and Table 21 lists the internal SIA collision timing limits for the AUI.

Figure 9 Internal SIA Mode AUI Timing Diagram—Collision

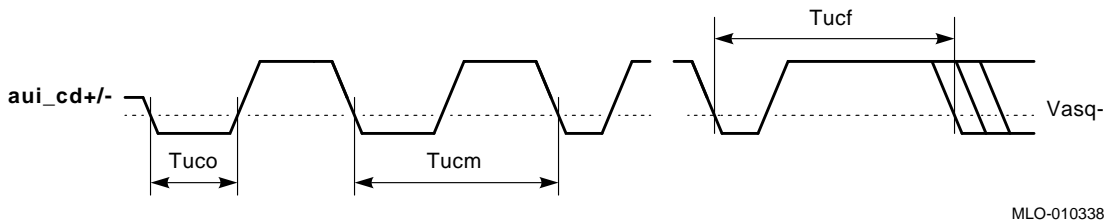


Table 21 Internal SIA Mode AUI Timing Specifications—Receive and Collision

Symbol	Definition	Minimum	Maximum	Units
Tudo ¹	au_i_rd_± start of frame pulse width	15	20	ns
Tudm ¹	au_i_rd_± delay between opposite squelch crossings not recognized as end of packet	—	140	ns
Tudf ¹	au_i_rd_± delay from last squelch crossing recognized as end of packet	150	—	ns
Tuco ¹	au_i_cd_± start of collision pulse width	20	25	ns
Tucm ¹	au_i_cd_± delay between squelch crossings not recognized as end of collision	—	140	ns
Tucf ¹	au_i_cd_± delay from last squelch crossing recognized as end of collision	150	—	ns

¹Parameter design guarantee.

3.6.6 Internal SIA Mode 10BASE-T Interface Timing—Transmit

Figure 10 shows the internal SIA transmit timing characteristics for the 10BASE-T interface, and Table 22 lists the internal SIA transmit limits.

Figure 10 Internal SIA Mode 10BASE-T Interface Timing Diagram—Transmit

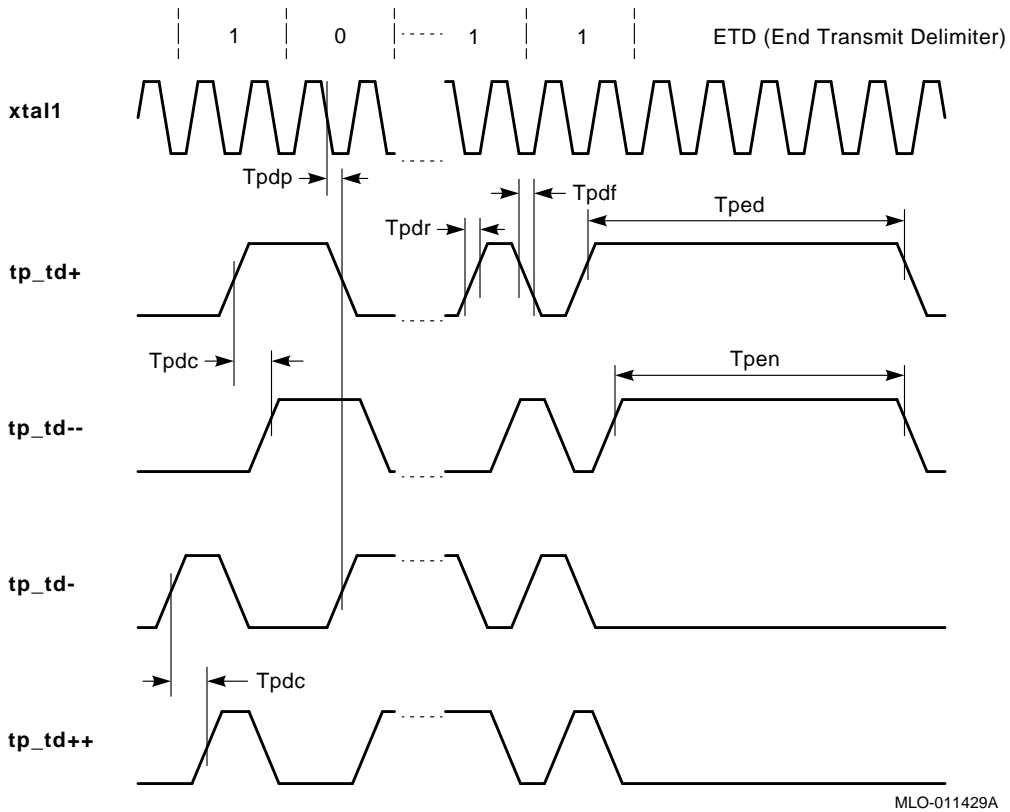


Table 22 Internal SIA Mode 10BASE-T Interface Timing Specifications—Transmit

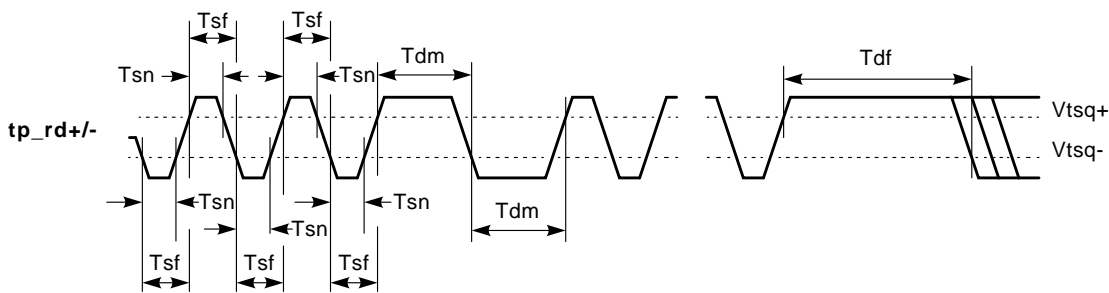
Symbol	Definition	Minimum	Maximum	Units
Tpdp	tp_td+ , tp_td- propagation delay from xtal1 fall	—	30	ns
Tpdr ¹	tp_td+ , tp_td++ , tp_td- , tp_td- – rise time	2	8	ns
Tpdf ¹	tp_td+ , tp_td++ , tp_td- , tp_td- – fall time	2	8	ns
Tpdm ¹	tp_td+ , tp_td++ , tp_td- , tp_td- – rise and fall time mismatch (not shown)	—	1	ns
Tpdc ¹	tp_td+ to tp_td- – and tp_td- to tp_td++ delay	46	54	ns
Tped ¹	tp_td± end transmit delimiter length	295	355	ns
Tpen ¹	tp_td++/- – end transmit delimiter length	245	305	ns

¹Parameter design guarantee.

3.6.7 Internal SIA Mode 10BASE-T Interface Timing—Receive

Figure 11 shows the internal SIA receive timing characteristics for the 10BASE-T interface, and Table 23 lists the internal SIA receive limits for the 10BASE-T interface.

Figure 11 Internal SIA Mode 10BASE-T Interface Timing Diagram—Receive



MLO-010340

Table 23 Internal SIA Mode 10BASE-T Interface Timing Specifications—Receive

Symbol	Definition	Minimum	Maximum	Units
Tsn ¹	tp_{rd±} start of frame pulse width during smart squelch operation	15	20	ns
Tsf ¹	tp_{rd±} maximum delay between opposite squelch crossings to not turn smart squelch off	140	150	ns
Tdm ¹	tp_{rd±} delay between opposite squelch crossings not recognized as end of packet	—	140	ns
Tdf ¹	tp_{rd±} delay from last squelch crossing recognized as end of packet	150	—	ns

¹Parameter design guarantee.

3.6.8 Internal SIA Mode 10BASE-T Interface Timing—Idle Link Pulse

Figure 12 shows the internal SIA idle link pulse timing characteristics for the 10BASE-T interface, and Table 24 lists the internal SIA idle link pulse limits for the 10BASE-T interface.

Figure 12 Internal SIA Mode 10BASE-T Interface Timing Diagram—Idle Link Pulse

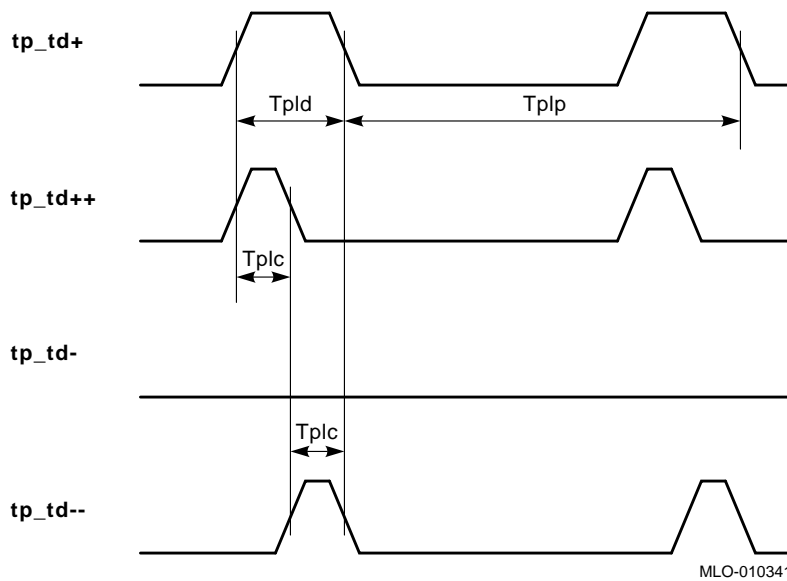


Table 24 Internal SIA Mode 10BASE-T Interface Timing Specifications—Idle Link Pulse

Symbol	Definition	Minimum	Maximum	Units
T_{pld}^1	tp_{td+} idle link pulse width	80	120	ns
T_{plc}^1	tp_{td++} and tp_{td-} - idle link pulse width	40	60	ns
T_{plp}^1	Idle link pulse period	8	24	ms

¹Parameter design guarantee.

3.7 Joint Test Action Group—Test Access Port

This section provides the joint test action group (JTAG) test access port specifications.

3.7.1 JTAG dc Specifications

Table 25 lists the dc specifications for the JTAG pins.

Table 25 JTAG dc Specifications

Symbol	Definition	Conditions	Minimum	Maximum	Units
V_{oh}	Output high voltage	$I_{oh} = -4 \text{ mA}$	2.4	—	V
V_{ol}	Output low voltage	$I_{ol} = 4 \text{ mA}$	—	0.4	V
V_{ih}	Input high voltage	—	2.0	—	V
V_{il}	Input low voltage	—	—	0.8	V
I_i	Input leakage current (tck)	$0.0 < V_{in} < \mathbf{vdd}$	—	± 20	μA
I_{ip}	Input leakage current on pins with internal pullups (tdi and tms)	$0.0 < V_{in} < \mathbf{vdd}$	—	$+20/-1500^1$	μA
I_{oz}	Tristate output leakage current (tdo)	$0.0 < V_{out} < \mathbf{vdd}$	—	± 20	μA

¹For **tdi** and **tms** pins that have internal pullups, the leakage current can get to 1.5 mA when $V_{in} = 0 \text{ V}$.

3.7.2 JTAG Boundary-Scan Timing

Figure 13 shows the JTAG boundary-scan timing, and Table 26 lists the interface signal timing relationships.

Figure 13 JTAG Boundary-Scan Timing Diagram

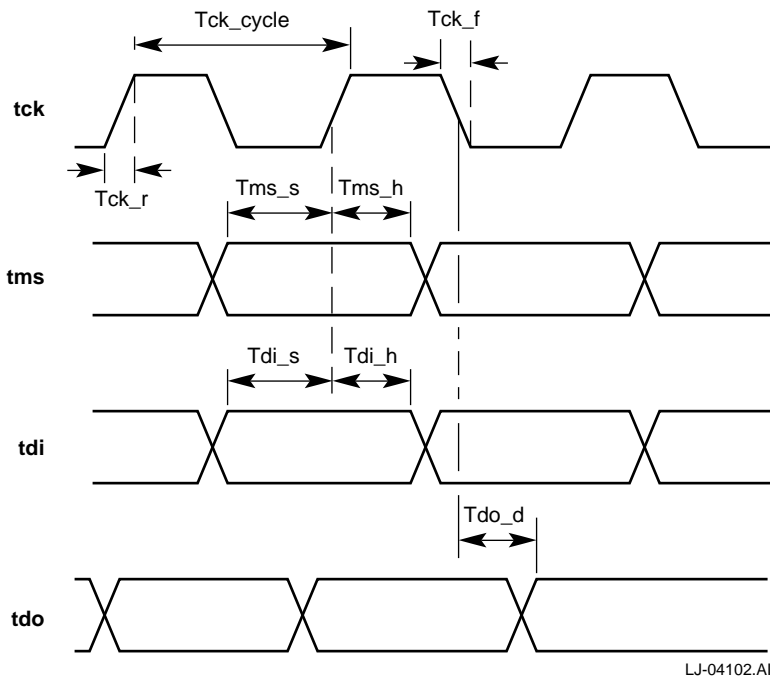


Table 26 JTAG Interface Signal Timing Specifications

Symbol	Parameter	Minimum	Maximum	Units
Tms_s	tms setup time	20	—	ns
Tms_h	tms hold time	5	—	ns
Tdi_s	tdi setup time	20	—	ns
Tdi_h	tdi hold time	5	—	ns
Tdo_d	tdo delay time	—	20	ns
Tck_r ¹	tck rise time	—	3	ns
Tck_f ¹	tck fall time	—	3	ns
Tck_cycle	tck cycle time	90	—	ns

¹Parameter design guarantee.

3.8 Boot ROM, Serial ROM, and LED Port Specification

Table 27 lists the dc specifications for the boot ROM, serial ROM, and the LED multiplexed port. These specifications apply in any mode in which the port is used.

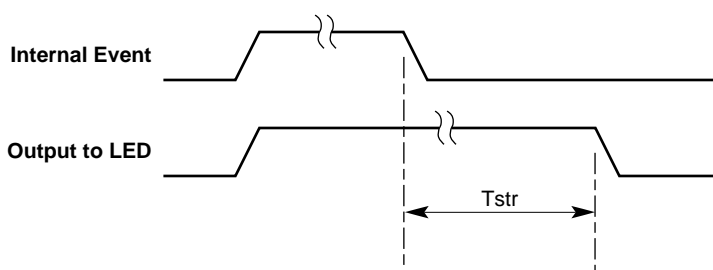
Table 27 Boot ROM, Serial ROM, and LED Port dc Specifications

Symbol	Definition	Conditions	Minimum	Maximum	Units
V _{oh}	Output high voltage	I _{oh} = -4 mA	2.4	—	V
V _{ol}	Output low voltage	I _{ol} = 4 mA	—	0.4	V
V _{ih}	Input high voltage	—	2.0	—	V
V _{il}	Input low voltage	—	—	0.8	V
I _{oz}	Maximum tristate output leakage current	V _{out} = V _{dd} or V _{ss}	-10	10	μA
I _{ip}	Input leakage current on pins with internal pullups (br_a<0>/sr_dout)	0.0 < V _{in} < vdd	—	+20/-1500	μA

3.9 LED Timing

Figure 14 shows the stretching function for a sample internal signal that is reflected by an LED. It also shows how this function affects the time that the LED is on. Table 28 lists the stretching function timing specification.

Figure 14 LED Signal Stretching Function Timing Diagram



LJ-04172.AI

Table 28 LED Signal Stretching Function Timing Specifications

Symbol	Definition	Minimum	Maximum	Units
Tstr ¹	Stretch time from internal event fall time	52	78	ms

¹Parameter design guarantee.

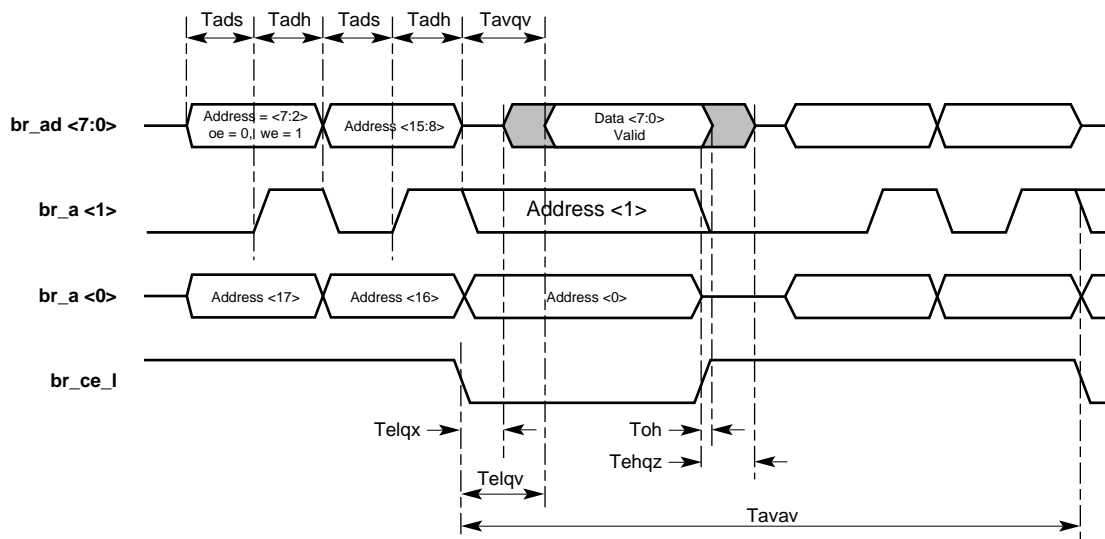
3.10 Boot ROM Port Timing

This section describes the boot ROM port timing.

3.10.1 Boot ROM Read Timing

Figure 15 shows the boot ROM read timing characteristics, and Table 29 lists the boot ROM read timing limits.

Figure 15 Boot ROM Read Timing Diagram



LJ-04104.AI

Table 29 Boot ROM Read Timing Specifications

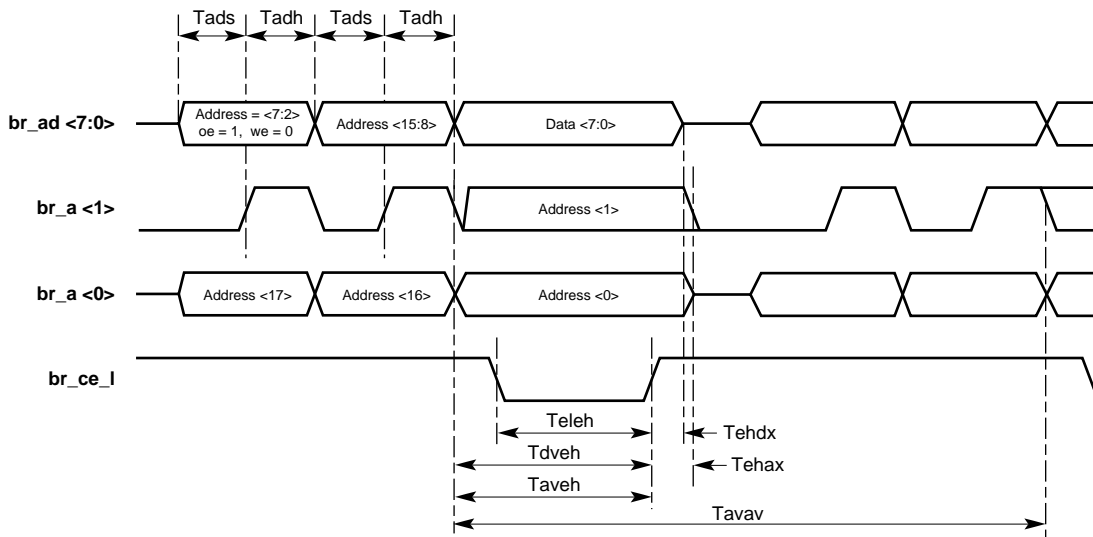
Symbol	Parameter	Minimum	Maximum	Units
Tavav ¹	Read cycle time	120	—	ns
Tavqv ¹	Address to output delay	—	120	ns
Telqv ¹	br_ce_1 to output delay	—	120	ns
Telqx ¹	br_ce_1 to output low impedance	0	—	ns
Tehqz ¹	br_ce_1 going high to output high impedance	—	55	ns
Toh ¹	Output hold from br_ce_1 change	0	—	ns
Tads ¹	Address setup to latch enable high	30	—	ns
Tadh ¹	Address hold from latch enable high	30	—	ns

¹Parameter design guarantee.

3.10.2 Boot ROM Write Timing

Figure 16 shows the boot ROM write timing characteristics, and Table 30 lists the boot ROM write timing limits.

Figure 16 Boot ROM Write Timing Diagram



LJ-04103.AI

Table 30 Boot ROM Write Timing Specifications

Symbol	Parameter	Minimum	Maximum	Units
Tavav ¹	Write cycle time	120	—	ns
Teleh ¹	br_ce_1 pulse width	70	—	ns
Taveh ¹	Address setup to br_ce_1 going high	50	—	ns
Tdveh ¹	Data setup to br_ce_1 going high	50	—	ns
Tehdx ¹	Data hold from br_ce_1 going high	10	—	ns
Tehax ¹	Address hold from br_ce_1 high	15	—	ns
Tads ¹	Address setup to latch enable high	30	—	ns
Tadh ¹	Address hold from latch enable high	30	—	ns

¹Parameter design guarantee.

3.11 Ethernet ID Port Serial ROM Timing

Figure 17 shows the Ethernet ID port serial ROM timing characteristics, and Table 31 lists the Ethernet ID port serial ROM timing limits.

Figure 17 Ethernet ID Port Timing Diagram

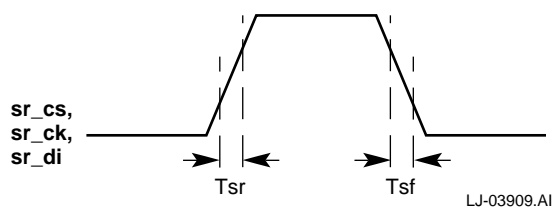


Table 31 Ethernet ID Port Timing Specifications

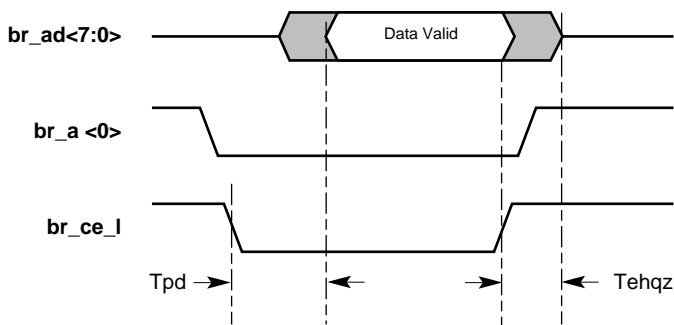
Symbol	Definition	Minimum	Maximum	Units
Tsr ¹	Rise time	—	10	ns
Tsf ¹	Fall time	—	10	ns

¹Parameter design guarantee.

3.12 External Register Timing

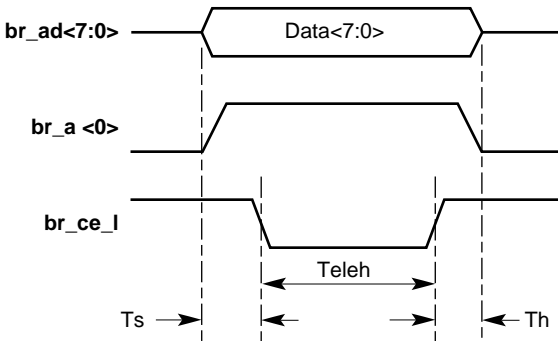
Figure 18 shows the external register read timing characteristics, and Figure 19 shows its write timing characteristics. Table 32 lists the external register timing specifications for both read and write operations.

Figure 18 External Register Read Timing Diagram



LJ-04169.AI

Figure 19 External Register Write Timing Diagram



LJ-04170.AI

Table 32 External Register Timing Specifications

Symbol	Parameter	Minimum	Maximum	Units
Teleh ¹	br_ce_l pulse width	120	—	ns
Read Timing				
Tpd ¹	br_ce_l low to br_ad <7:0> valid	—	20	ns
Tehqz ¹	br_ce_l high to br_ad <7:0> high impedance	—	20	ns
Write Timing				
Ts ¹	Data setup time prior to br_ce_l	30	—	ns
Th ¹	Data hold after br_ce_l high	30	—	ns

¹Parameter design guarantee.

4 Mechanical Specifications

The 21041 is contained in a 120-pin plastic quad flat pack (PQFP). Table 33 lists the mechanical specifications, and Figure 20 shows the mechanical layout of the 21041.

Table 33 120-Pin PQFP Package Dimensions

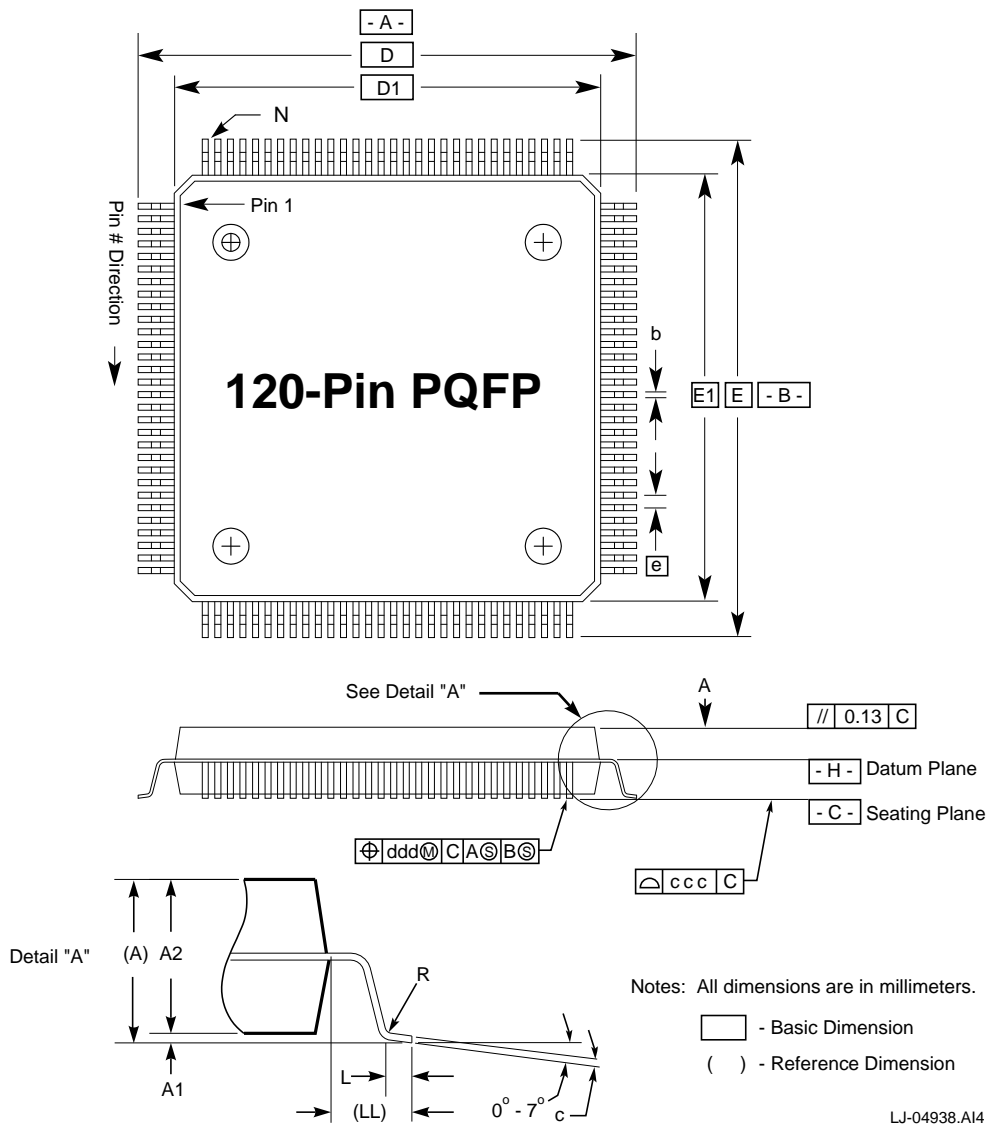
Symbol	Dimension	Value (mm)
LL	Lead length	1.60 reference ¹
e	Lead pitch	0.80 BSC ²
L	Foot length	0.65 minimum to 1.03 maximum
A	Package overall height	4.10 maximum
A1	Package standoff height	0.25 minimum
A2	Package thickness	3.17 minimum to 3.67 maximum
b	Lead width	0.30 minimum to 0.45 maximum
c	Lead thickness	0.11 minimum to 0.23 maximum
ccc	Coplanarity	0.10
ddd	Lead skew	0.20
D	Package overall width	31.20 BSC ²
D1	Package width	28.00 BSC ²
E	Package overall length	31.20 BSC ²
E1	Package length	28.00 BSC ²
R	Ankle radius	0.13 minimum to 0.30 maximum

¹The value for this measurement is for reference only.

²The default tolerances for basic (BSC) dimensions are:

0 mm to 5 mm	±0.1 mm
5 mm to 30 mm	±0.2 mm
30 mm to 100 mm	±0.3 mm

Figure 20 Mechanical Layout of the 21041



[查询"21041"供应商](#)

Technical Support and Ordering Information

Obtaining Technical Support

If you need technical support or help deciding which literature best meets your needs, call the Digital Semiconductor Information Line:

United States and Canada **1-800-332-2717**
Outside North America **+1-508-628-4760**

Ordering Digital Semiconductor Products

To order the Digital Semiconductor 21041 PCI Ethernet LAN Controller and evaluation board, contact your local distributor.

The following table lists some of the semiconductor products you can order from Digital. To obtain a Digital Semiconductor Product Catalog, contact the Digital Semiconductor Information Line.

Product	Order Number
Digital Semiconductor 21041 PCI Ethernet LAN Controller	21041-AB
Digital Semiconductor 21041 Evaluation Board Kit	21A41-01
Digital Semiconductor 21140A PCI Fast Ethernet LAN Controller	21140-AC
Digital Semiconductor 21140A 10/100BASE-TX Evaluation Board Kit	21A40-TX
Digital Semiconductor 21142 PCI 10/100-Mb/s Ethernet LAN Controller	21142-PA (PQFP package) 21142-TA (TQFP package)

Ordering Digital Semiconductor Literature

The following table lists some of the available Digital Semiconductor literature. For a complete list, contact the Digital Semiconductor Information Line.

Title	Order Number
Digital Semiconductor 21041 PCI Ethernet LAN Controller Product Brief	EC-QAWVB-TE
Digital Semiconductor 21041 PCI Ethernet LAN Controller Hardware Reference Manual	EC-QAWXB-TE
Using the Digital Semiconductor 21041 with Boot ROM, Serial ROM, and External Register: An Application Note	EC-QJLGB-TE

Ordering Third-Party Literature

You can order the following third-party literature directly from the vendor:

Title	Vendor
PCI Local Bus Specification, Revisions 2.0 and 2.1	PCI Special Interest Group 1-800-433-5177 (U.S.) 1-503-797-4207 (International) 1-503-234-6762 (FAX)
Institute of Electrical and Electronics Engineers (IEEE) 802.3	The Institute of Electrical and Electronics Engineers, Inc. 1-800-701-4333 (U.S.) 1-908-981-0060 (International) 1-908-981-9667 (FAX)