DC MOTOR DRIVER IC

Check for Samples: DRV8842

FEATURES

- **Single H-Bridge Current-Control Motor Driver**
  - **Drives One DC Motor, One Coil of a Stepper Motor, or Other Actuators**
  - **Five-Bit Winding Current Control Allows Up to 32 Current Levels**
  - **Low MOSFET On-Resistance**
- **5-A Maximum Drive Current at 24 V, 25°C**
- **Built-In 3.3-V Reference Output**
- **Independent 1/2-Bridge Parallel Digital Control Interface**
- **8-V to 45-V Operating Supply Voltage Range**
- **Thermally Enhanced Surface Mount Package**

APPLICATIONS

- **Printers**
- **Scanners**
- **Office Automation Machines**
- **Gaming Machines**
- **Factory Automation**
- **Robotics**

DESCRIPTION

The DRV8842 provides an integrated motor driver solution for printers, scanners, and other automated equipment applications. The device has one H-bridge driver, and is intended to drive one DC motor, one coil of a stepper motor, or other loads. The output driver block consists of N-channel power MOSFET’s configured as an H-bridge. The DRV8842 can supply up to 5-A peak or 3.5-A RMS output current (with proper heatsinking at 24 V and 25°C).

Separate inputs to independently control each half of the H-bridge are provided.

Internal shutdown functions are provided for over current protection, short circuit protection, under voltage lockout and overtemperature.

TheDRV8842 is available in a 28-pin HTSSOP package with PowerPAD™ (Eco-friendly: RoHS & no Sb/Br).

PRODUCT PREVIEW

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PowerPAD™ (HTSSOP) - PWP	Reel of 2000	DRV8842PWPR	8842

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

DEVICE INFORMATION

Functional Block Diagram

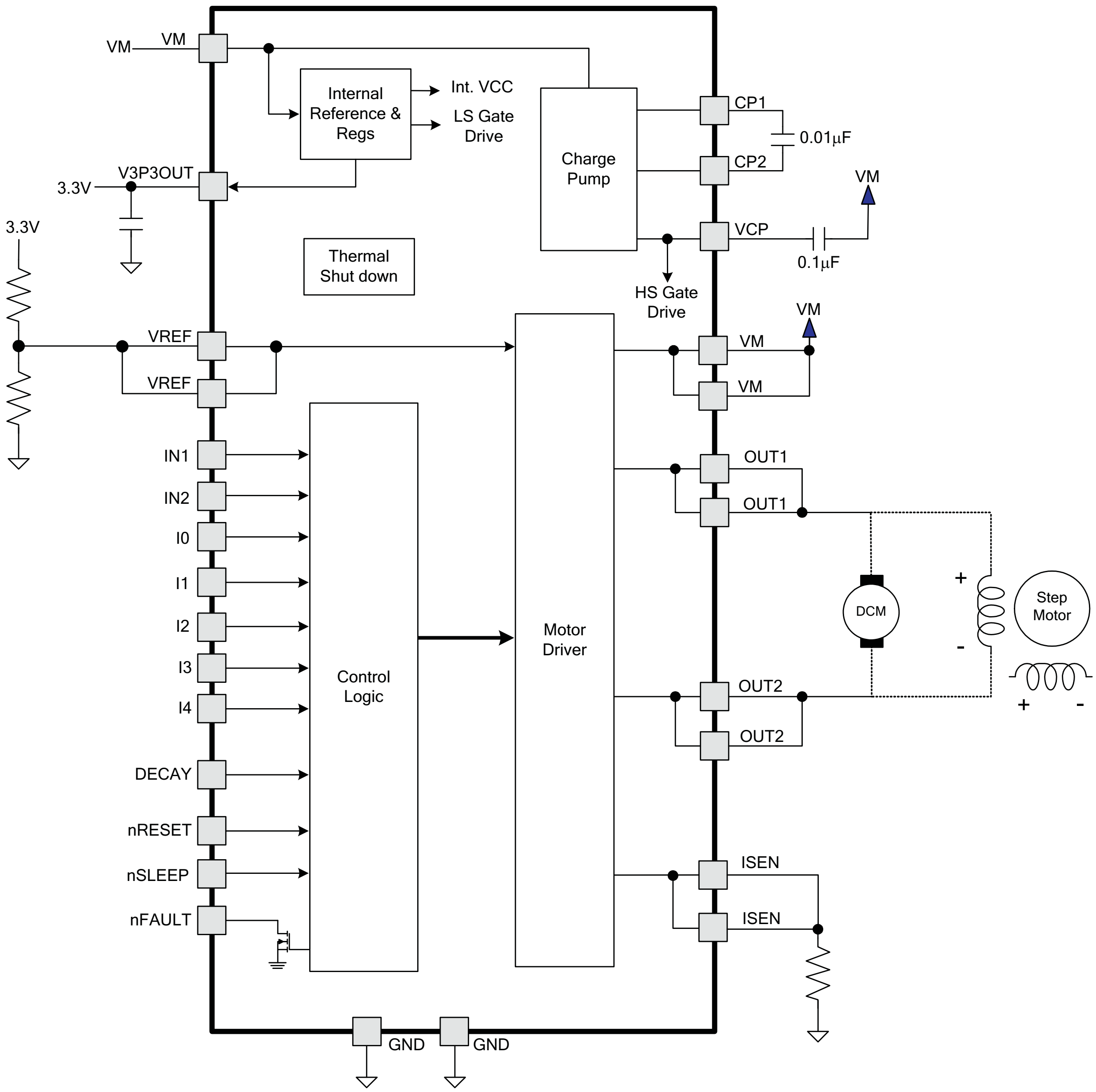
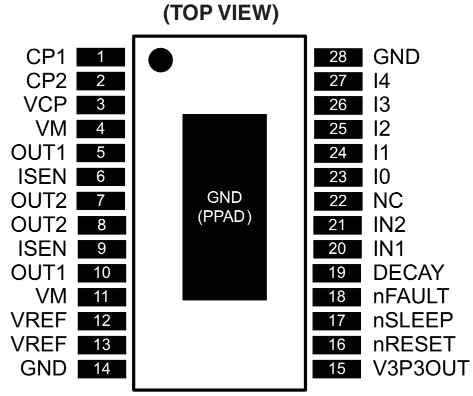


Table 1. TERMINAL FUNCTIONS

NAME	PIN	I/O [1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
POWER AND GROUND				
GND	14, 28	-	Device ground	
VM	4, 11	-	Bridge A power supply	Connect to motor supply (8 V - 45 V). Both pins must be connected to same supply.
V3P3OUT	15	O	3.3-V regulator output	Bypass to GND with a 0.47-µF, 6.3-V ceramic capacitor. Can be used to supply VREF.
CP1	1	IO	Charge pump flying capacitor	Connect a 0.01-µF 50-V capacitor between CP1 and CP2.
CP2	2	IO	Charge pump flying capacitor	
VCP	3	IO	High-side gate drive voltage	Connect a 0.1-µF 16-V ceramic capacitor to VM.
CONTROL				
IN1	20	I	Input 1	Logic input controls state of OUT1
IN2	21	I	Input 2	Logic input controls state of OUT2
I0	23	I	Current set inputs	Sets winding current as a percentage of full-scale
I1	24	I		
I2	25	I		
I3	26	I		
I4	27	I		
DECAY	19	I	Decay mode	Low = slow decay, open = mixed decay, high = fast decay
nRESET	16	I	Reset input	Active-low reset input initializes the logic and disables the H-bridge outputs
nSLEEP	17	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode
VREF	12,13	I	Current set reference input	Reference voltage for winding current set. Both pins must be connected together on the PCB.
STATUS				
nFAULT	18	OD	Fault	Logic low when in fault condition (overtemp, overcurrent)
OUTPUT				
ISEN	6, 9	IO	Bridge ground / Isense	Connect to current sense resistor. Both pins must be connected together on the PCB.
OUT1	5, 10	O	Bridge output 1	Connect to motor winding. Both pins must be connected together on the PCB.
OUT2	7, 8	O	Bridge output 2	Connect to motor winding. Both pins must be connected together on the PCB.

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

PWP PACKAGE (TOP VIEW)



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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1) (2)

		VALUE	UNIT
VM	Power supply voltage range	–0.3 to 47	V
	Digital pin voltage range	–0.5 to 7	V
VREF	Input voltage	–0.3 to 4	V
	ISENSEx pin voltage	–0.3 to 0.8	V
	Peak motor drive output current, t < 1 µS	Internally limited	A
	Continuous motor drive output current (3)	5	A
	Continuous total power dissipation	See Dissipation Ratings table	
T_J	Operating virtual junction temperature range	–40 to 150	°C
T_A	Operating ambient temperature range	–40 to 85	°C
T_{stg}	Storage temperature range	–60 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed.

DISSIPATION RATINGS (PRELIMINARY)

BOARD	PACKAGE	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	T_A < 25°C	T_A = 70°C	T_A = 85°C
Low-K (1)	PWP	67.5°C/W	14.8 mW/°C	1.85 W	1.18 W	0.96 W
Low-K (2)		39.5°C/W	25.3 mW/°C	3.16 W	2.02 W	1.64 W
High-K (3)		33.5°C/W	29.8 mW/°C	3.73 W	2.38 W	1.94 W
High-K (4)		28°C/W	35.7 mW/°C	4.46 W	2.85 W	2.32 W

(1) The JEDEC Low-K board used to derive this data was a 76-mm x 114-mm, 2-layer, 1.6-mm thick PCB with no backside copper.
(2) The JEDEC Low-K board used to derive this data was a 76-mm x 114-mm, 2-layer, 1.6-mm thick PCB with 25-cm^2 2-oz copper on back side.
(3) The JEDEC High-K board used to derive this data was a 76-mm x 114-mm, 4-layer, 1.6-mm thick PCB with no backside copper and solid 1-oz internal ground plane.
(4) The JEDEC High-K board used to derive this data was a 76-mm x 114-mm, 4-layer, 1.6-mm thick PCB with 25-cm^2 1-oz copper on back side and solid 1-oz internal ground plane.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage range (1)	8		45	V
V_{REF}	VREF input voltage (2)	1		3.5	V
I_{V3P3}	V3P3OUT load current			1	mA

(1) All V_M pins must be connected to the same supply voltage.
(2) Operational at VREF between 0 V and 1 V, but accuracy is degraded.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	VM operating supply current	V_M = 24 V, f_{PWM} < 50 kHz		5	8	mA
I_{VMQ}	VM sleep mode supply current	V_M = 24 V		10	20	µA
V_{UVLO}	VM undervoltage lockout voltage	V_M rising		9	10	V
V3P3OUT REGULATOR						
V_{3P3}	V3P3OUT voltage	IOUT = 0 to 1 mA	3.2	3.3	3.4	V
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage			0.6	0.7	V
V_{IH}	Input high voltage		2		5.25	V
V_{HYS}	Input hysteresis		0.3	0.45	0.6	V
I_{IL}	Input low current	VIN = 0	–20		20	µA
I_{IH}	Input high current	VIN = 3.3 V		33	100	µA
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	µA
DECAY INPUT						
V_{IL}	Input low threshold voltage	For slow decay (brake) mode	0		0.8	V
V_{IH}	Input high threshold voltage	For fast decay (coast) mode	2			V
I_{IN}	Input current	VIN = 0 V to 3.3 V	–25		25	µA
H-BRIDGE FETS						
$R_{DS(ON)}$	HS FET on resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		TBD		Ω
		V_M = 24 V, I_O = 1 A, T_J = 85°C		0.15	TBD	
$R_{DS(ON)}$	LS FET on resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		TBD		Ω
		V_M = 24 V, I_O = 1 A, T_J = 85°C		0.15	TBD	
I_{OFF}	Off-state leakage current		–40		40	µA
MOTOR DRIVER						
f_{PWM}	PWM frequency		45	50	55	kHz
t_{BLANK}	Current sense blanking time			3.75		µs
t_R	Rise time		50		300	ns
t_F	Fall time		50		300	ns
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		TBD		TBD	A
t_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C
CURRENT CONTROL						
I_{REF}	VREF input current	VREF = 3.3 V	–3		3	µA
V_{TRIP}	ISENSE trip voltage	VREF = 3.3 V, 100% current setting	635	660	685	mV
ΔI_{TRIP}	Current trip accuracy (relative to programmed value)	VREF = 3.3 V, 5% current setting	–25		25	%
		VREF = 3.3 V, 10% - 34% current setting	–15		15	
		VREF = 3.3 V, 38% - 67% current setting	–10		10	
		VREF = 3.3 V, 71% - 100% current setting	–5		5	
A_{ISENSE}	Current sense amplifier gain	Reference only		5		V/V

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FUNCTIONAL DESCRIPTION

PWM Motor Drivers

The DRV8842 contains one H-bridge motor driver with current-control PWM circuitry. A block diagram of the motor control circuitry is shown in Figure 1.

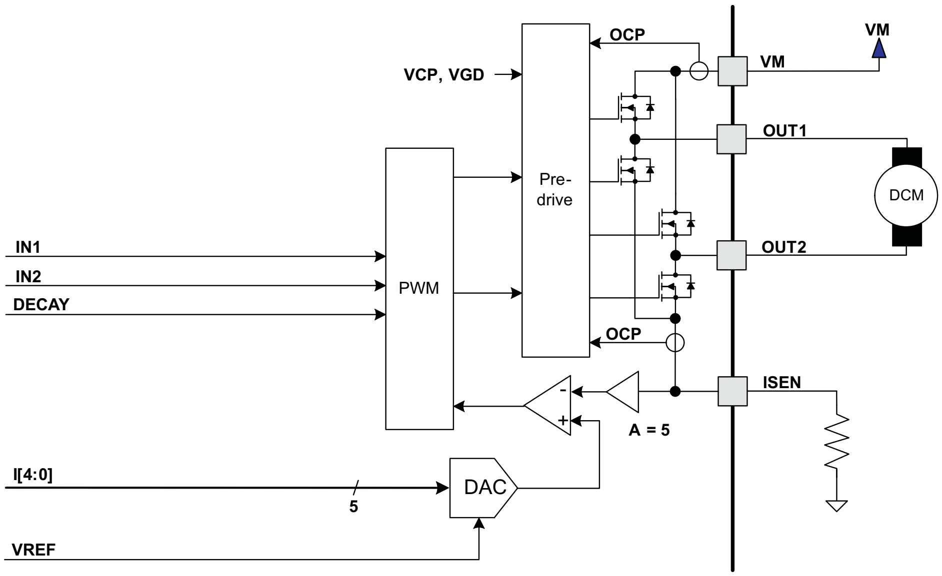

Figure 1. Motor Control Circuitry

Note that there are multiple VM, ISEN, OUT, and VREF pins. All like-named pins must be connected together on the PCB.

Bridge Control

The IN1 and IN2 input pins directly control the state of the OUT1 and OUT2 outputs. Either input can also be used for PWM control of the load. Table 2 shows the logic.

Table 2. H-Bridge Logic

xIN1	xIN2	xOUT1	xOUT2
0	0	L	L
0	1	L	H
1	0	H	L
1	1	H	H

Current Regulation

The maximum current through the load is regulated by a fixed-frequency PWM current regulation, or current chopping. When the H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. Once the current hits the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle.

For DC motors, current regulation is used to limit the start-up and stall current of the motor. Speed control is typically performed by providing an external PWM signal to the xIN1 or xIN2 input pins.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the ISEN pin, multiplied by a factor of 5, with a reference voltage. The reference voltage is input from the VREF pin, and is scaled by a 5-bit DAC that allows current settings of zero to 100% in an approximately sinusoidal sequence.

The full-scale (100%) chopping current is calculated in Equation 1.

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$$I_{CHOP} = \frac{V_{REFX}}{5 \bullet R_{ISENSE}} \qquad (1)$$

Example:

If a 0.25-Ω sense resistor is used and the VREFx pin is 2.5 V, the full-scale (100%) chopping current will be 2.5 V / (5 x 0.25 Ω) = 2 A.

Five input pins per (I0 through I4) are used to scale the current in the bridge as a percentage of the full-scale current set by the VREF input pin and sense resistance. The function of the pins is shown in Table 3.

Table 3. Pin Functions

I[4..0]	RELATIVE CURRENT (% FULL-SCALE CHOPPING CURRENT)
0x00h	0%
0x01h	5%
0x02h	10%
0x03h	15%
0x04h	20%
0x05h	24%
0x06h	29%
0x07h	34%
0x08h	38%
0x09h	43%
0x0Ah	47%
0x0Bh	51%
0x0Ch	56%
0x0Dh	60%
0x0Eh	63%
0x0Fh	67%
0x10h	71%
0x11h	74%
0x12h	77%
0x13h	80%
0x14h	83%
0x15h	86%
0x16h	88%
0x17h	90%
0x18h	92%
0x19h	94%
0x1Ah	96%
0x1Bh	97%
0x1Ch	98%
0x1Dh	99%
0x1Eh	100%
0x1Fh	100%

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Decay Mode

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 2 as case 1. The current flow direction shown indicates the state when the IN1 pin is high and the IN2 pin is low.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. As the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in Figure 2 as case 2.

In slow decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in Figure 2 as case 3.

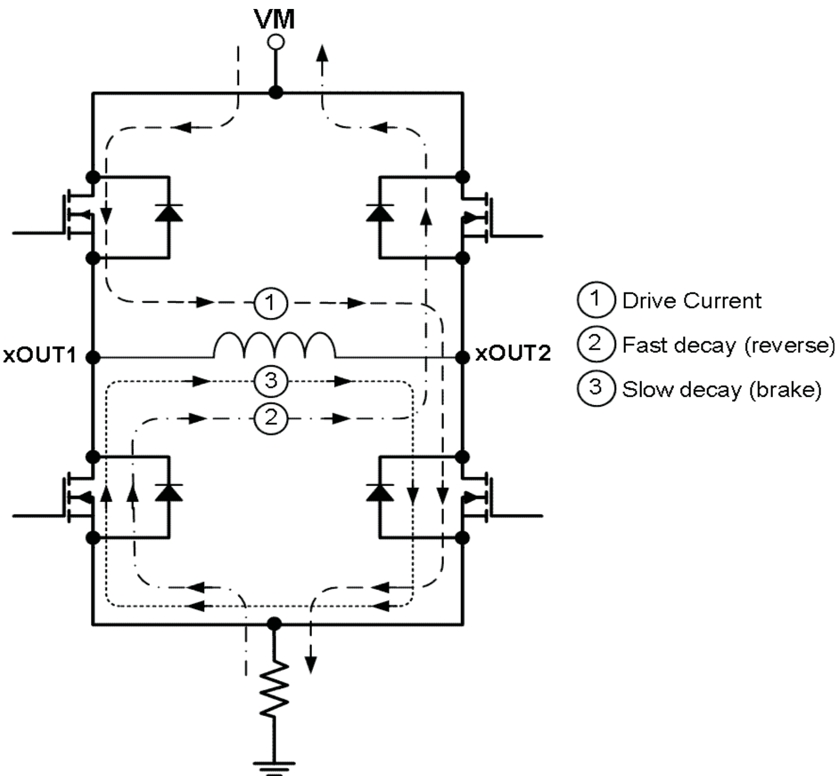

Figure 2. Decay Mode

The DRV8842 supports fast decay, slow decay and a mixed decay mode. Slow, fast, or mixed decay mode is selected by the state of the DECAY pin - logic low selects slow decay, open selects mixed decay operation, and logic high sets fast decay mode.

Mixed decay mode begins as fast decay, but at a fixed period of time (75% of the PWM cycle) switches to slow decay mode for the remainder of the fixed PWM period.

Blanking Time

After the current is enabled in an H-bridge, the voltage on the xISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 μs. Note that the blanking time also sets the minimum on time of the PWM.

nRESET and nSLEEP Operation

The nRESET pin, when driven active low, resets the internal logic. It also disables the H-bridge driver. All inputs are ignored while nRESET is active.

Driving nSLEEP low will put the device into a low power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped, the V3P3OUT regulator is disabled, and all internal clocks are stopped. In this state all inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time (approximately 1 ms) needs to pass before the motor driver becomes fully operational.

Protection Circuits

The DRV8842 is fully protected against undervoltage, overcurrent and overtemperature events.

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Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. The device will remain disabled until either nRESET pin is applied, or VM is removed and re-applied.

Overcurrent conditions on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Note that overcurrent protection does not use the current sense circuitry used for PWM current control, and is independent of the I_{SENSE} resistor value or VREF voltage.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume.

Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pins falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled and internal logic will be reset. Operation will resume when V_M rises above the UVLO threshold.

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THERMAL INFORMATION

Thermal Protection

The DRV8842 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Power Dissipation

Average power dissipation in the DRV8842 when running a DC motor can be roughly estimated by: Equation 2.

$$P = 2 \bullet R_{DS(ON)} \bullet (I_{OUT})^2 \quad (2)$$

where P is the power dissipation of one H-bridge, $R_{DS(ON)}$ is the resistance of each FET, and I_{OUT} is the RMS output current being applied to each winding. I_{OUT} is equal to the average current drawn by the DC motor. Note that at start-up and fault conditions this current is much higher than normal running current; these peak currents and their duration also need to be taken into consideration. The factor of 2 comes from the fact that at any instant two FETs are conducting winding current (one high-side and one low-side).

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report SLMA002, " PowerPAD™ Thermally Enhanced Package" and TI application brief SLMA004, " PowerPAD™ Made Easy", available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

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