查询"AD7821TE/883B"供应商

LC²MOS 8-Bit Sampling ADC

AD7821

1.1 Scope.

This specification covers the detail requirement for a monolithic CMOS 8-bit sampling analog-to-digital converter. It features a conversion time of 660 ns and accepts unipolar or bipolar inputs.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD7821T(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-20	20-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = +25°C)

V_{DD} to GND	−0.3 V, +7 V
V_{SS} to GND	+0.3 V, −7 V
V_{IN} to GND	V_{SS} −0.3 V, V_{DD} +0.3 V
V_{REF}(+) to GND	V_{SS} −0.3 V, V_{DD} +0.3 V
V_{REF}(−) to GND	V_{SS} −0.3 V, V_{DD} +0.3 V
V_{IN} to GND	V_{SS} −0.3 V, V_{DD} +0.3 V
Digital Inputs to DGND	−0.3 V, V_{DD} +0.3 V
Digital Outputs to DGND	−0.3 V, V_{DD} +0.3 V
Power Dissipation (to +75°C)	450 mW
Derates above +75°C	6 mW/°C
Operating Temperature Range	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-20 and E-20A
θ_{JA} = 120°C/W for Q-20 and E-20A

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AD7821—SPECIFICATIONS

Table 1.

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Test	Symbol	Device	Design Limit T_{MIN}–T_{MAX}	Sub Group 1	Sub Group 2, 3	Test Condition[1, 2]	Units
Resolution	RES	–1	8			This Is the Minimum Resolution for Which No Missing Codes Are Guaranteed.	Bits
Total Unadjusted Error[3]	TUE	–1	1	1	1		±LSB max
Signal to Noise Ratio	SNR	–1	45	45	45		dB
Total Harmonic Distortion	THD	–1	–50	–50	–50		dB
Peak Harmonic or Spurious Noise		–1	–30	–30	–30		dB
Intermodulation Distortion Second Order	IMD	–1	–30	–30	–30		dB
Third Order		–1	–50	–50	–50		dB
Analog Input Leakage Current	I_{IN}	–1	3	3	3		±μA max
Analog Input Capacitance	C_I	–1	55				pF typ
Reference Input Resistance	R_I	–1	1	1	1		kΩ min
			4	4	4		kΩ max
Digital Input High Level	V_{IH}	–1	2.4	2.4	2.4	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$	V min
			3.5	3.5	3.5	Mode (Pin 7)	
Digital Input Low Level	V_{IH}	–1	0.8	0.8	0.8	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$	V max
			1.5	1.5	1.5	Mode (Pin 7)	
Digital Input High Current	I_{IH}	–1	1.0	1.0	1.0	$\overline{CS}$, $\overline{RD}$	μA max
			3.0	3.0	3.0	$\overline{WR}$	
			200.0	200.0	200.0	Mode (Pin 7)	
Digital Input Low Current	I_{IL}	–1	1.0	1.0	1.0	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, Mode (Pin 7)	–μA max
Digital Input Capacitance	C_I	–1	8.0			$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, Mode (Pin 7)	pF max
Digital Output High Level	V_{OH}	–1	4.0	4.0	4.0	DB0–DB7, $\overline{OFL}$, $\overline{INT}$ I_{SOURCE} = 360 μA	V min
Digital Output Low Level	V_{OL}	–1	0.4	0.4	0.4	DB0–DB7, $\overline{OFL}$, $\overline{INT}$ I_{SINK} = 1.6 mA	V max
			0.4			RDY: I_{SINK} = 2.6 mA	
Floating State Leakage Current	I_{OUT}	–1	3.0	3.0	3.0	DB0–DB7	μA max
Digital Output Capacitance	C_{OUT}	–1	8.0			(Typically 5 pF)	pF max
Slew Rate Tracking		–1	1.6			Typically 2.36	V/μs
Supply Current from V_{DD}	I_{DD}	–1	25	25	25	$\overline{CS}$ = $\overline{RD}$ = 0 V	mA max
Supply Current from V_{SS}	I_{SS}	–1	100	100	100	$\overline{CS}$ = $\overline{RD}$ = 0 V	μA max
Power Supply Sensitivity		–1	1/4	1/4	1/4	V_{DD} = 5 V ± 5%	±LSB max
$\overline{CS}$ to $\overline{RD}$/$\overline{WR}$ Setup Time	t_{CS}	–1	0				ns min
$\overline{CS}$ to $\overline{RD}$/$\overline{WR}$ Hold Time	t_{CH}	–1	0				ns min
$\overline{CS}$ to RDY Delay. Pull-Up Resistor 2 kΩ[4]	t_{RDY}	–1	100			70 ns max at +25°C	ns max
Conversion Time ($\overline{RD}$ Mode)	t_{CRD}	–1	975			700 ns max at +25°C	ns max
Data Access Time ($\overline{RD}$ Mode)[5]	t_{ACCO}	–1	t_{CRD} +75			(t_{CRD} +50) ns max at +25°C	ns max

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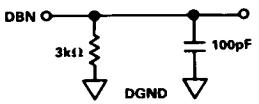
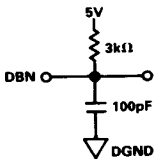
Test	Symbol	Device	Design Limit T_{MIN}–T_{MAX}	Sub Group 1	Sub Group 2, 3	Test Condition[1, 2]	Units
$\overline{RD}$ to INT Delay ($\overline{RD}$ Mode)[4]	t_{INTH}	−1	90			80 ns max at +25°C	ns max
Data Hold Time[6]	t_{DH}	−1	80			60 ns max at +25°C	ns max
			15			15 ns min at +25°C	ns min
Delay Time Between Conversions	t_P	−1	500			350 ns min at +25°C	ns min
Write Pulse Width	t_{WR}	−1	400				ns min
			10			250 ns min at +25°C	μs max
Delay Time Between $\overline{WR}$ and $\overline{RD}$ Pulses	t_{RD}	−1	450			250 ns min at +25°C	ns min
Data Access Time[5] ($\overline{WR}$/$\overline{RD}$ Mode, See Figure 4)	t_{ACC1}	−1	275			185 ns min at +25°C	ns max
$\overline{RD}$ to $\overline{INT}$ Delay	t_{RI}	−1	220			150 ns max at +25°C	ns max
$\overline{WR}$ to $\overline{INT}$ Delay[4]	t_{INTL}	−1	700			500 ns max at +25°C	ns max
Access Time[5] ($\overline{WR}$/$\overline{RD}$ Mode, See Figure 3)	t_{ACC2}	−1	130			90 ns max at +25°C	ns max
$\overline{WR}$ to $\overline{INT}$ Delay (Stand-Alone Operation)[4]	t_{IHWR}	−1	120			80 ns max at +25°C	ns max
Data Access Time after $\overline{INT}$ (Stand-Alone Operation)	t_{ID}	−1	70			45 ns max at +25°C	ns max

NOTES
[1]V_{DD} = +5 V; $V_{REF}(+)$ = +5 V; $V_{REF}(-)$ = GND = 0 V unless otherwise specified. Specifications apply for $\overline{RD}$ mode (Pin 7 = 0 V).
[2]All input control signals are specified with $t_r = t_f$ = 20 ns (10% to 90% of +5 V) and timed from a voltage level of +1.6 V.
[3]Includes gain error, offset error and linearity error.
[4]C_L = 50 pF.
[5]Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[6]Defined as the time required for the data lines to changed 0.5 V when loaded with the circuits of Figure 2.

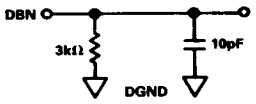


a. High-Z to V_{OH}

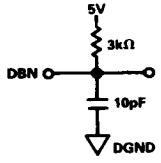


b. High-Z to V_{OL}

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High-Z



b. V_{OL} to High-Z

Figure 2. Load Circuits for Data Hold Time Test

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3.2.1 Functional Block Diagram and Terminal Assignments.

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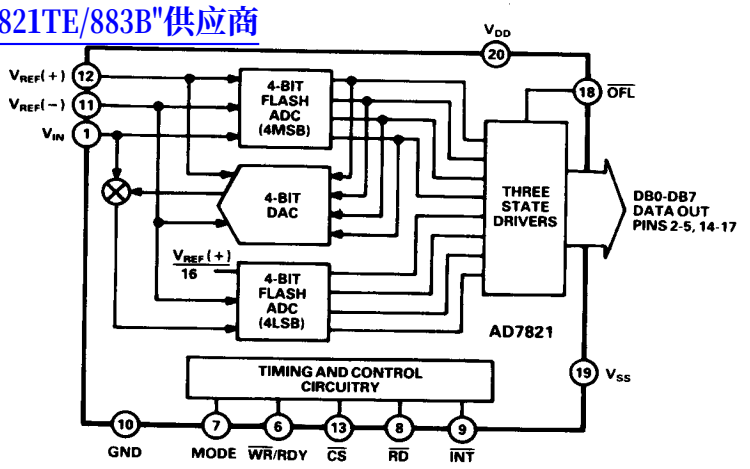
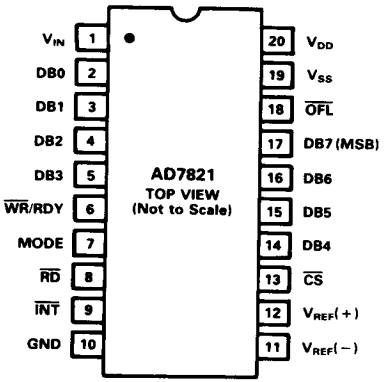
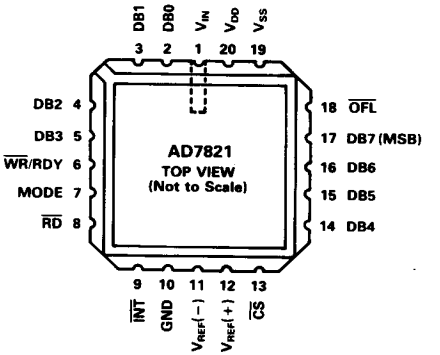


Q Package (DIP)



E Package (LCC)



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (81).

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4.2.1 Life Test/Burn-In Circuit.

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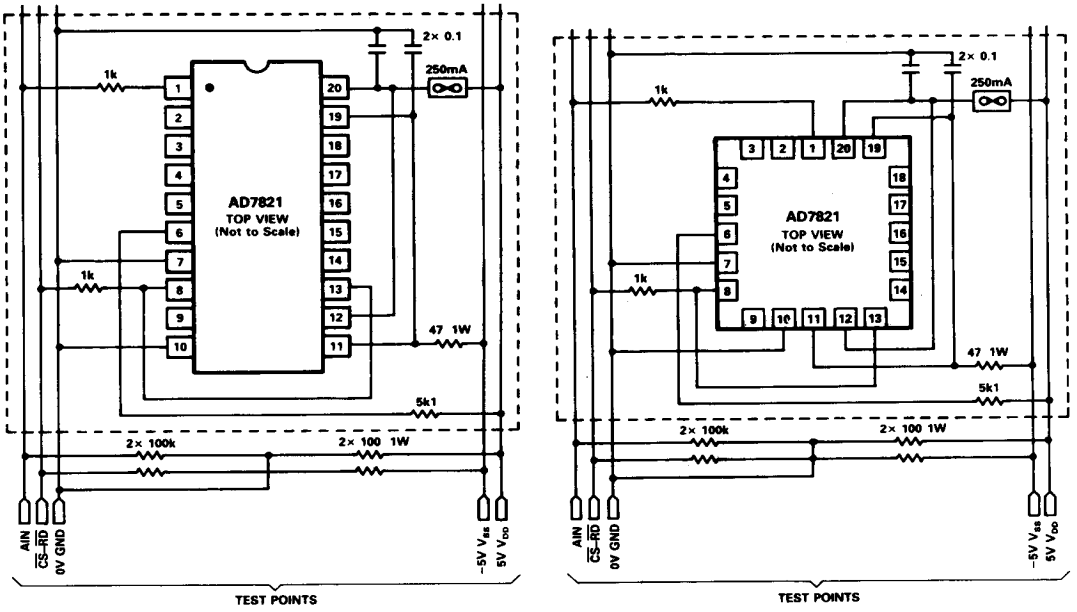
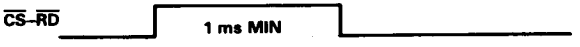
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD7821 Edge Connections



AIN = 0V

Static Burn-In Initialization

AIN = ±4.7V SINE @ 100Hz

Dynamic Burn-In Signals

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6.0 Digital Interface.

The AD7821 has two basic interface modes which are determined by the status of the MODE pin. When this pin is low, the converter is in the RD mode; with this pin high, the AD7821 is set up for the WR-RD mode.

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The RD mode is designed for microprocessors which can be driven into a WAIT state. A READ operation (i.e., $\overline{CS}$ and $\overline{RD}$ are taken low) starts a conversion and data is read when the conversion is complete. The WR-RD mode does not require microprocessor WAIT states. A WRITE operation (i.e., $\overline{CS}$ and $\overline{WR}$ are taken low) initiates a conversion, and a READ operation reads the result when the conversion is complete.

6.1 RD Mode (MODE = 0).

The timing diagram for the RD mode is shown in Figure 3. This mode is intended for use with microprocessors which have a WAIT state facility, whereby a READ instruction cycle can be extended to accommodate slow memory devices. A conversion is started by taking $\overline{CS}$ and $\overline{RD}$ low (READ operation). Both $\overline{CS}$ and $\overline{RD}$ are then kept low until output data appears.

In this mode, Pin 6 of the AD7821 is configured as a status output, RDY. This RDY output can be used to drive the processor READY or WAIT input. It is an open drain output (no internal pull-up device) which goes low after the falling edge of $\overline{CS}$ and goes high impedance at the end of conversion. An $\overline{INT}$ line is also provided which goes low when a conversion is complete. $\overline{INT}$ returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

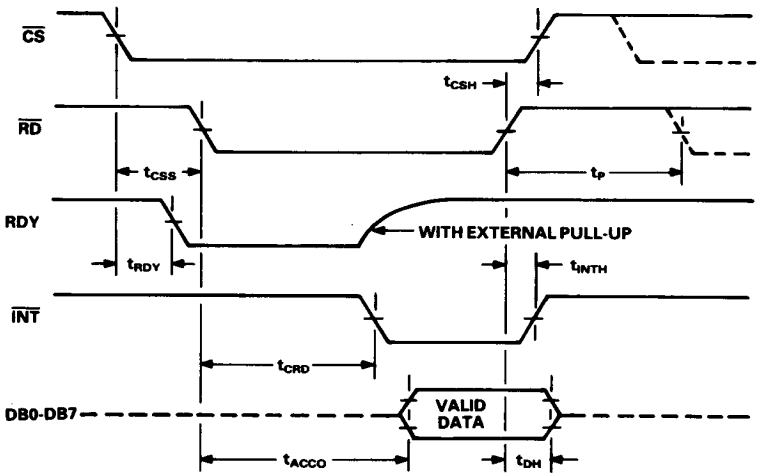

Figure 3. RD Mode

6.2 WR-RD Mode (MODE = 1).

In the WR-RD mode, Pin 6 is configured as a WRITE ($\overline{WR}$) input for the AD7821. With $\overline{CS}$ low, conversion is initiated on the falling edge of $\overline{WR}$. Two options exist for reading data from the converter.

In the first of these options the processor waits for the $\overline{INT}$ status line to go low before reading the data (see Figure 4). $\overline{INT}$ typically goes low within 380 ns after the rising edge of $\overline{WR}$. It indicates that conversion is complete and that the data result is in the output latch. With $\overline{CS}$ low, the data outputs (DB0–DB7) are activated when $\overline{RD}$ goes low. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$.

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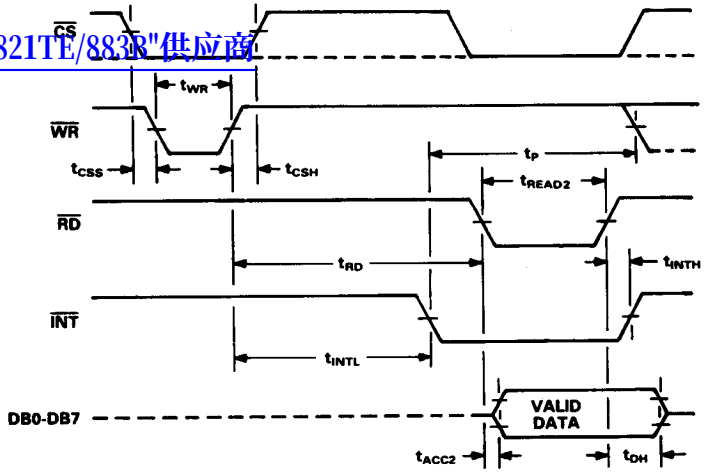

Figure 4. WR–RD Mode (t_{RD}>t_{INTL})

The alternative option can be used to shorten the conversion time. This is a method for bypassing the internal time-out circuit. The $\overline{INT}$ line is ignored and $\overline{RD}$ can be brought low 250 ns after the rising edge of $\overline{WR}$. In this case $\overline{RD}$ going low transfers the data result into the output latch and activates the data output (DB0–DB7). $\overline{INT}$ is driven low on the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$. The timing for this interface is shown in Figure 5.

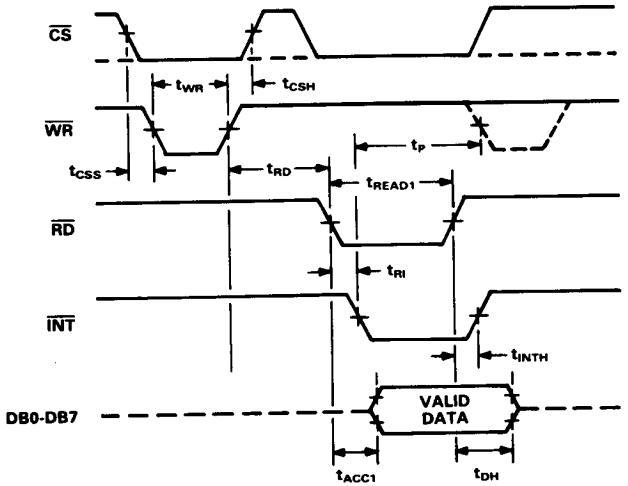

Figure 5. WR–RD Mode (t_{RD}<t_{INTL})

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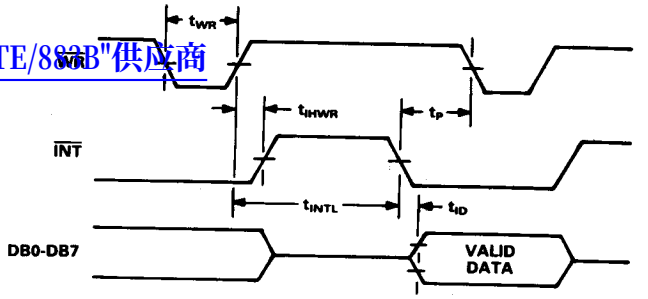

Figure 6. WR–RD Stand-Alone Operation, $\overline{CS}$ = $\overline{RD}$ = 0

The AD7821 can also be used in stand-alone operation in the WR-RD mode. $\overline{CS}$ and $\overline{RD}$ are tied low, and a conversion is initiated by bringing $\overline{WR}$ low. Output data is valid 530 ns (t_{INTL} + t_{ID}) after the rising edge of $\overline{WR}$. The timing diagram for this mode is shown in Figure 6.

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