REVISIONS			
	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24									

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Gary L. Gross

CHECKED BY
Jeff Bowling

APPROVED BY
Raymond Monnin

DRAWING APPROVAL DATE
98-09-11

REVISION LEVEL

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, MEMORY, CMOS, 32K x 9 PARALLEL SYNCHRONOUS FIFO, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-97631**

SHEET 1 OF 24

DSCC FORM 2233
APR 97

5962-E254-98

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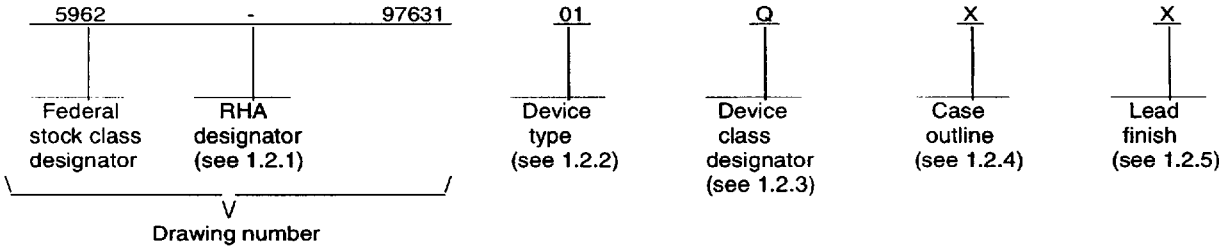
1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01		32K x 9 CMOS parallel synchronous FIFO	15 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CQCC1-N32	32	Rectangular leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103 and QML-38535 (see 6.6.2 herein).

1.3 Absolute maximum ratings. 2/

Terminal voltage with respect to ground	-0.5 V dc to +7.0 V dc
DC output current	20 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.25 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case X	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
Supply voltage (GND)	0 V
Input high voltage (V_{IH})	2.2 V dc minimum
Input low voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard for Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Blvd., Arlington, VA 22201).

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-PRF-38535.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Input leakage current	I_{LI}	$0.4\ V \le V_{IN} \le V_{CC}$	1,2,3	All	-10	+10	µA
Output leakage current	I_{LO}	$\overline{OE} \ge V_{IH}$, $0.4 \le V_{OUT} \le V_{CC}$	1,2,3	All	-10	+10	µA
Output high voltage	V_{OH}	I_{OH} = -2 mA, V_{CC} = min.	1,2,3	All	2.4		V
Output low voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = min.	1,2,3	All		0.4	V
Active power supply current	I_{CC1}	f = 20 MHz, outputs open	1,2,3	All		40	mA
Standby power supply current	I_{CC2}	1/	1,2,3	All		15	mA
Input capacitance	C_{IN}	V_{IN} = 0 V, f = 1.0 MHz, T_A = +25°C, see 4.4.1e	4	All		5	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V, f = 1.0 MHz, with output deselected ($\overline{OE}$ = high), T_A = +25°C, see 4.4.1e	4	All		7	pF
Functional tests		See 4.4.1c	7,8A,8B	All			
Clock cycle frequency	fs	C_L = 30 pF, input pulse levels = GND to 3.0 V, input rise/fall times = 3 ns, input/output timing reference levels = 1.5 V, see figures 3 and 4	9,10,11	All		66.7	MHz
Data access time	t_A		9,10,11	All	2	10	ns
Clock cycle time	t_{CLK}		9,10,11	All	15		ns
Clock high time	t_{CLKH}		9,10,11	All	6		ns
Clock low time	t_{CLKL}		9,10,11	All	6		ns
Data setup time	t_{DS}		9,10,11	All	4		ns
First read latency time	t_{FRL}		9,10,11	All		2/	
Data hold time	t_{DH}		9,10,11	All	1		ns
Enable setup time	t_{ENS}		9,10,11	All	4		ns
Enable hold time	t_{ENH}		9,10,11	All	1		ns
Reset pulse width 3/	t_{RS}		9,10,11	All	15		ns
Reset setup time	t_{RSS}		9,10,11	All	10		ns
Reset recovery time	t_{RSR}		9,10,11	All	10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Reset to flag and output time	t_{RSF}	C_L = 30 pF, input pulse levels = GND to 3.0 V, input rise/fall times = 3 ns, input/output timing reference levels = 1.5 V, see figures 3 and 4	9,10,11	All		15	ns
Output enable to output in low Z 4/	t_{OLZ}		9,10,11	All	0		ns
Output enable to output valid	t_{OE}		9,10,11	All	3	8	ns
Output enable to output in high Z 4/	t_{OHZ}		9,10,11	All	3	8	ns
Write clock to full flag	t_{WFF}		9,10,11	All		10	ns
Read clock to empty flag	t_{REF}		9,10,11	All		10	ns
Clock to programmable almost-full flag	t_{PAE}		9,10,11	All		10	ns
Clock to programmable almost-full flag	t_{PAF}		9,10,11	All		10	ns
Skew time between read clock and write clock for empty flag & full flag	t_{SKEW1}		9,10,11	All	6		ns
Skew time between read clock and write clock for Almost-Empty Flag & Almost-Full Flag	t_{SKEW2}		9,10,11	All	15		ns

1/ All inputs = V_{CC} - 0.2 V, except WCLK and RCLK (which are switching at f = 20 Mhz). All outputs are unloaded.
2/ When $t_{SKEW1} \ge$ the minimum limit, t_{FRL} (maximum) = $t_{CLK} + t_{SKEW1}$. When t_{SKEW1} < the minimum limit, t_{FRL} (max) = either $2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$. The latency timing applies only at the empty boundary ($\overline{EF}$ = LOW).
3/ Pulse widths less than the minimum values specified are not allowed.
4/ If not tested, shall be guaranteed to the limits specified in table I.

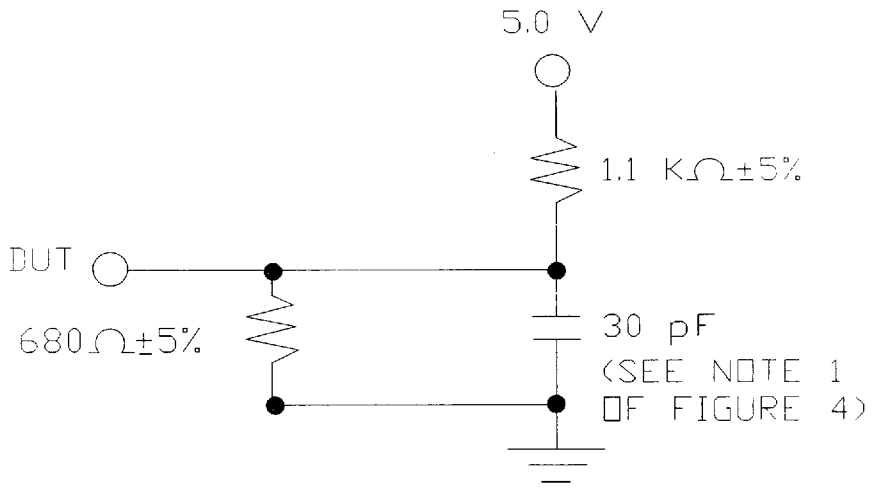
Device type	All
Case outline	X
Terminal number	Terminal symbol
1	D_5
2	D_4
3	D_3
4	D_2
5	D_1
6	D_0
7	$\overline{PAF}$
8	$\overline{PAE}$
9	GND
10	$\overline{REN1}$
11	RCLK
12	$\overline{REN2}$
13	$\overline{OE}$
14	$\overline{EF}$
15	$\overline{FF}$
16	Q_0
17	Q_1
18	Q_2
19	Q_3
20	Q_4
21	Q_5
22	Q_6
23	Q_7
24	Q_8
25	V_{CC}
26	WEN2/$\overline{LD}$
27	WCLK
28	$\overline{WEN1}$
29	$\overline{RS}$
30	D_8
31	D_7
32	D_6

FIGURE 1. Terminal connections.

No. of words in FIFO	$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
0	H	H	L	L
1 to n 1/	H	H	L	H
(n+1) to (32768-(m+1))	H	H	H	H
(32768-m) to 32767 2/	H	L	H	H
32768	L	L	H	H

1/ n = empty offset (n = 7 default value).
2/ m = full offset (m = 7 default value).

FIGURE 2. Truth table.



AC test conditions:
Input pulse levels: GND to 3.0 V
Input rise/fall times: ≤ 3 ns/V
Input timing reference levels: 1.5 V
Output reference levels: 1.5 V

FIGURE 3. Output load circuit.

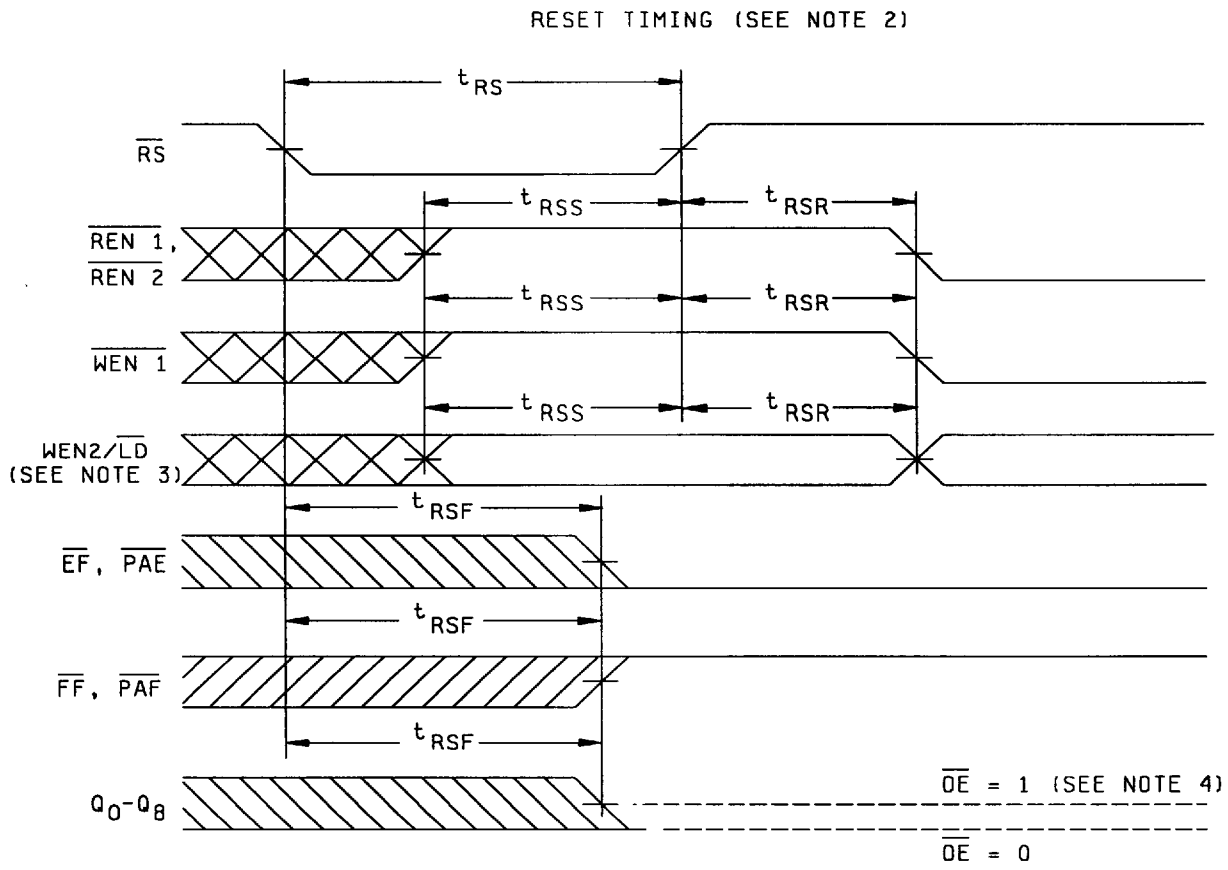


FIGURE 4. Timing waveforms.

WRITE CYCLE TIMING

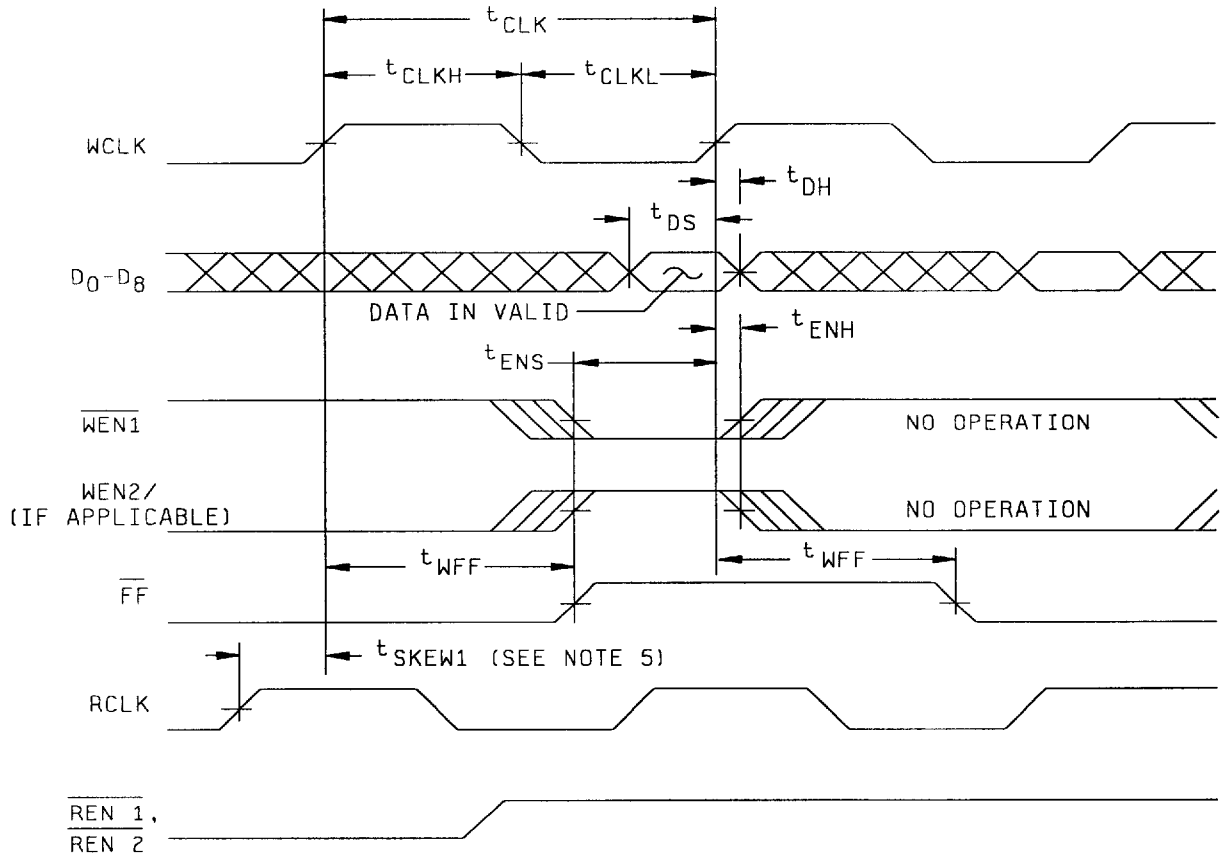


FIGURE 4. Timing waveforms - continued.

READ CYCLE TIMING

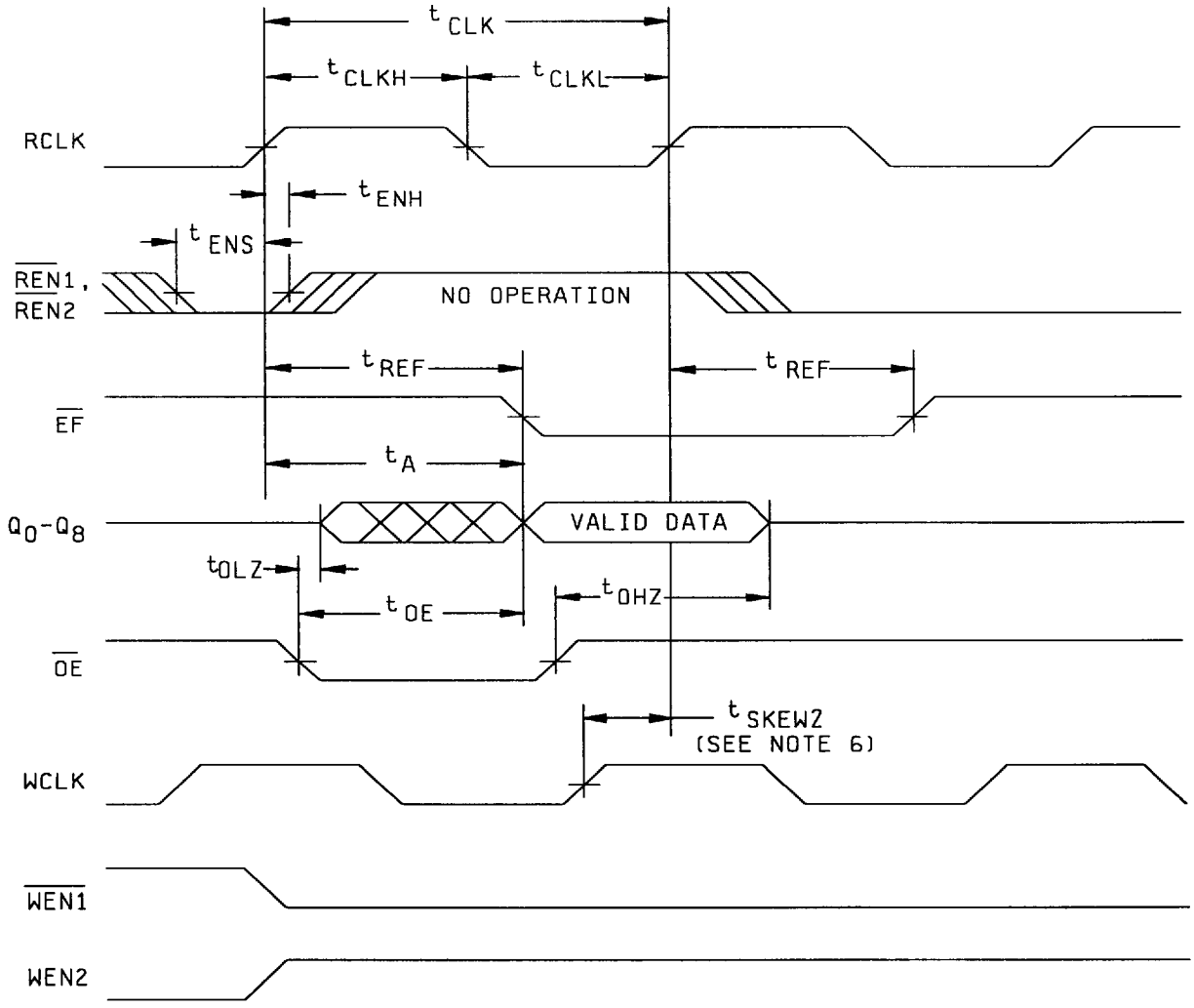


FIGURE 4. Timing waveforms - continued.

FIRST DATA WORD LATENCY AFTER RESET WITH READ AND WRITE

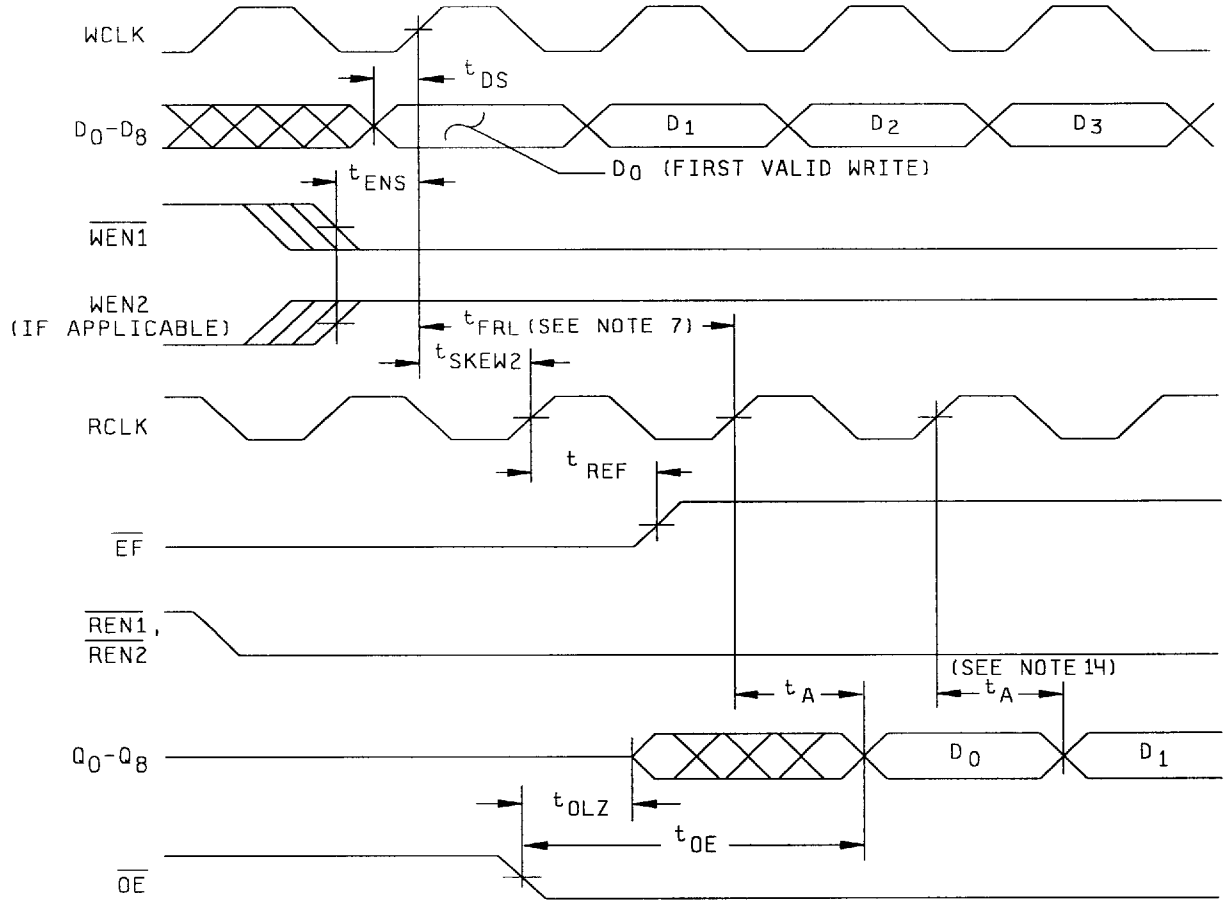
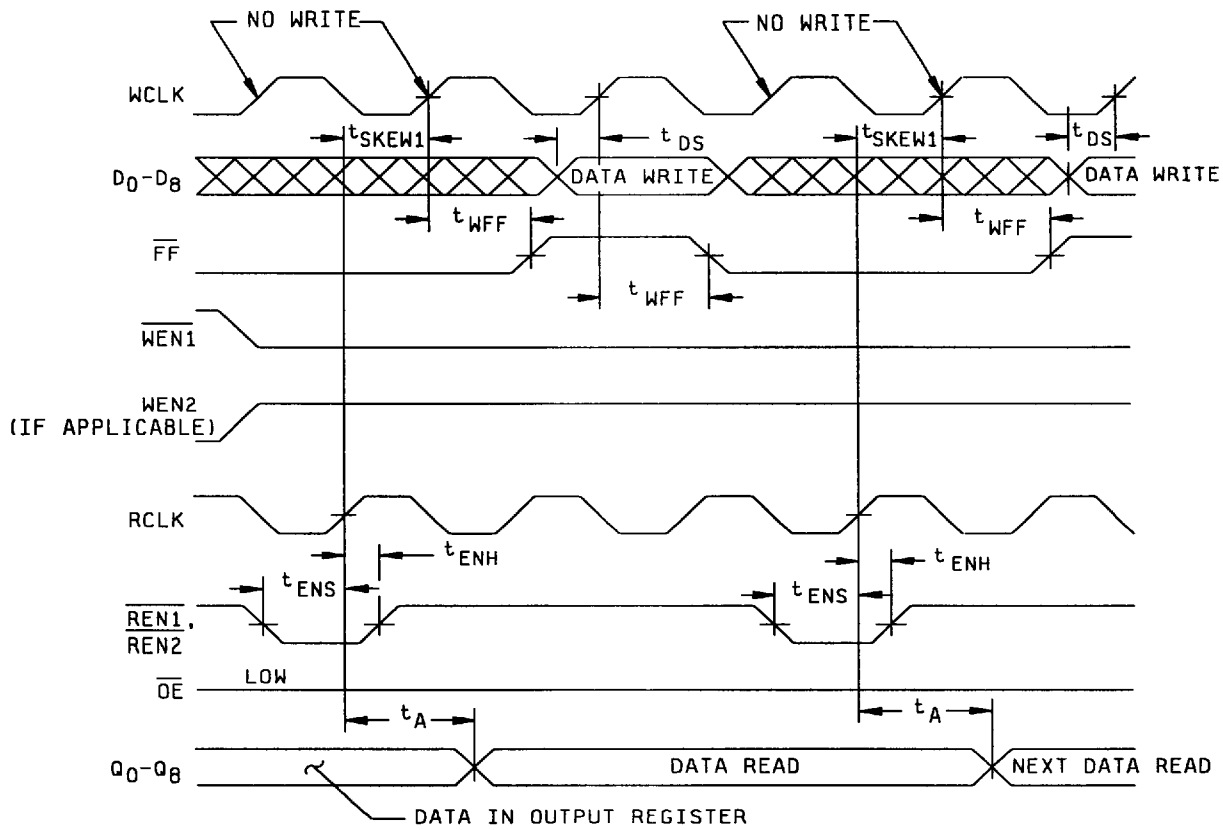


FIGURE 4. Timing waveforms - continued.

FULL FLAG TIMING



Note: For t_{SKEW1} tests, see note 5.

FIGURE 4. Timing waveforms - continued.

EMPTY FLAG TIMING

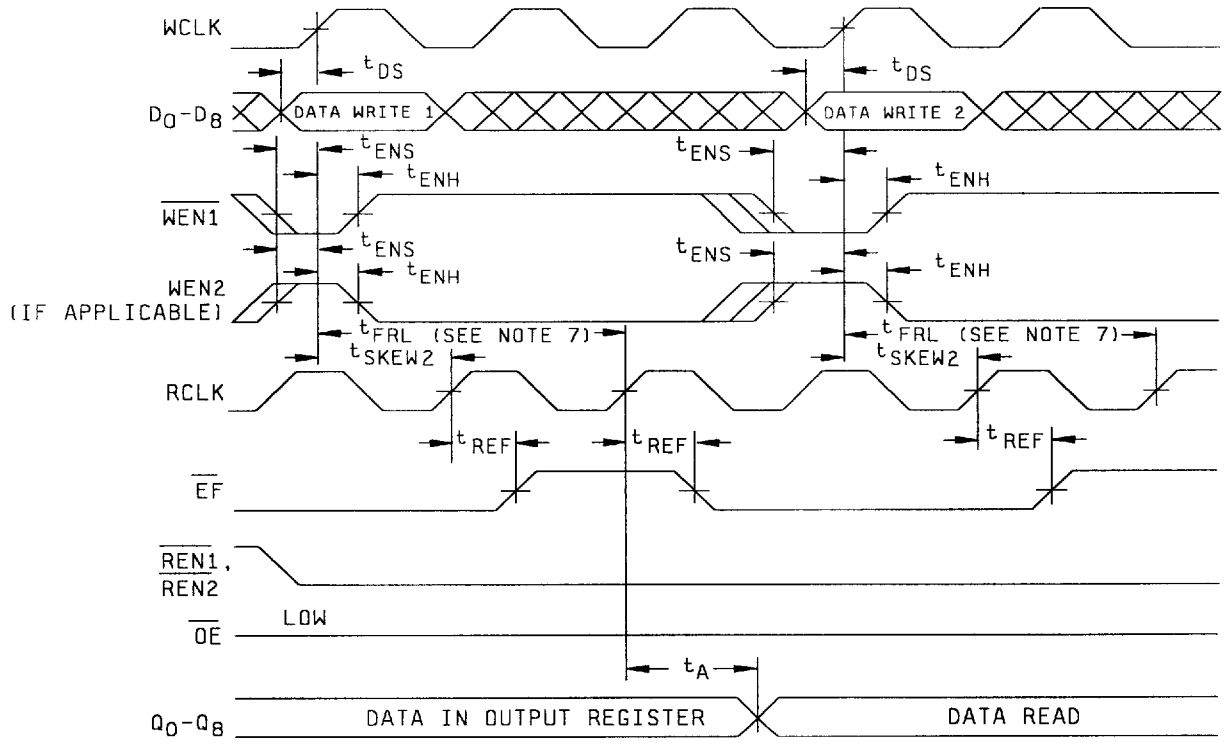


FIGURE 4. Timing waveforms - continued.

PROGRAMMABLE ALMOST-FULL FLAG TIMING

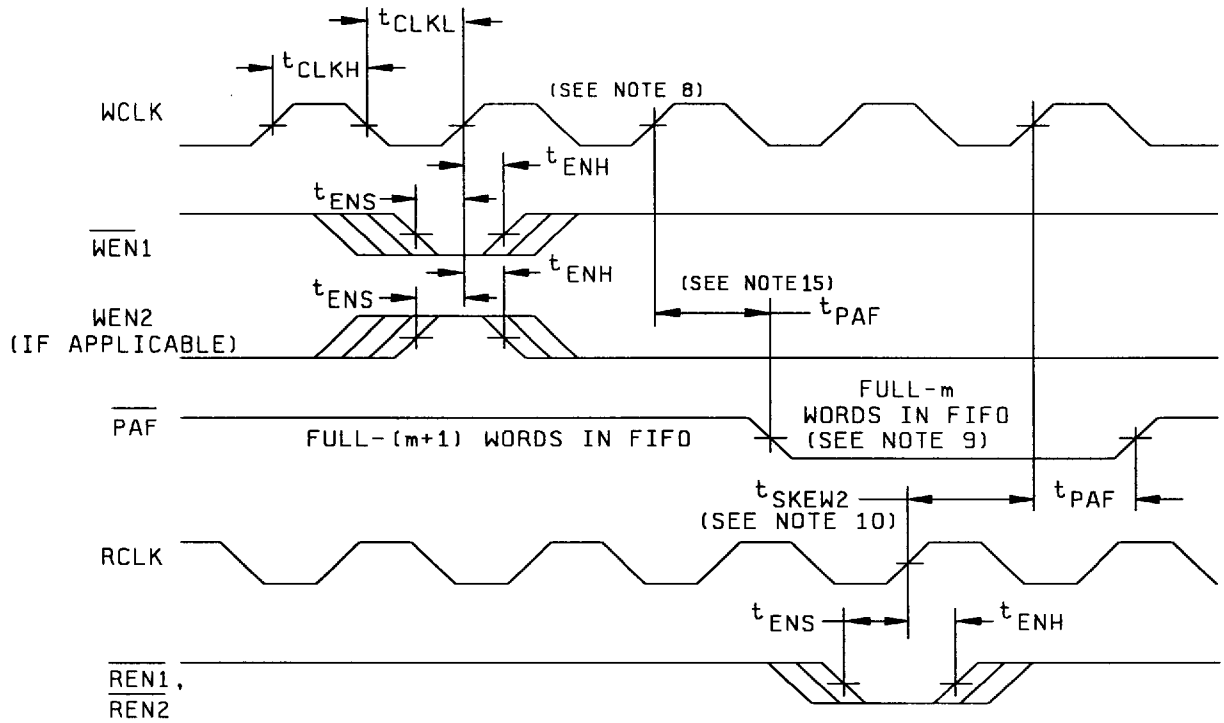


FIGURE 4. Timing waveforms - continued.

PROGRAMMABLE ALMOST-EMPTY FLAG TIMING

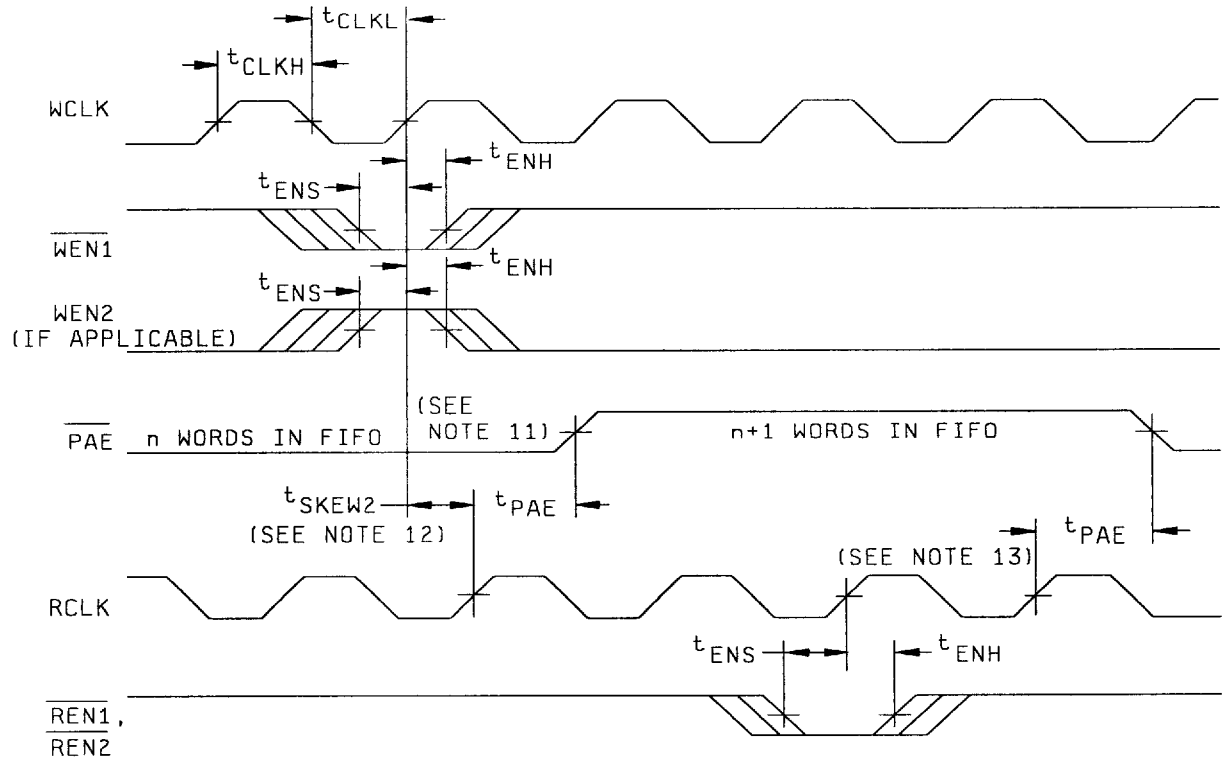


FIGURE 4. Timing waveforms - continued.

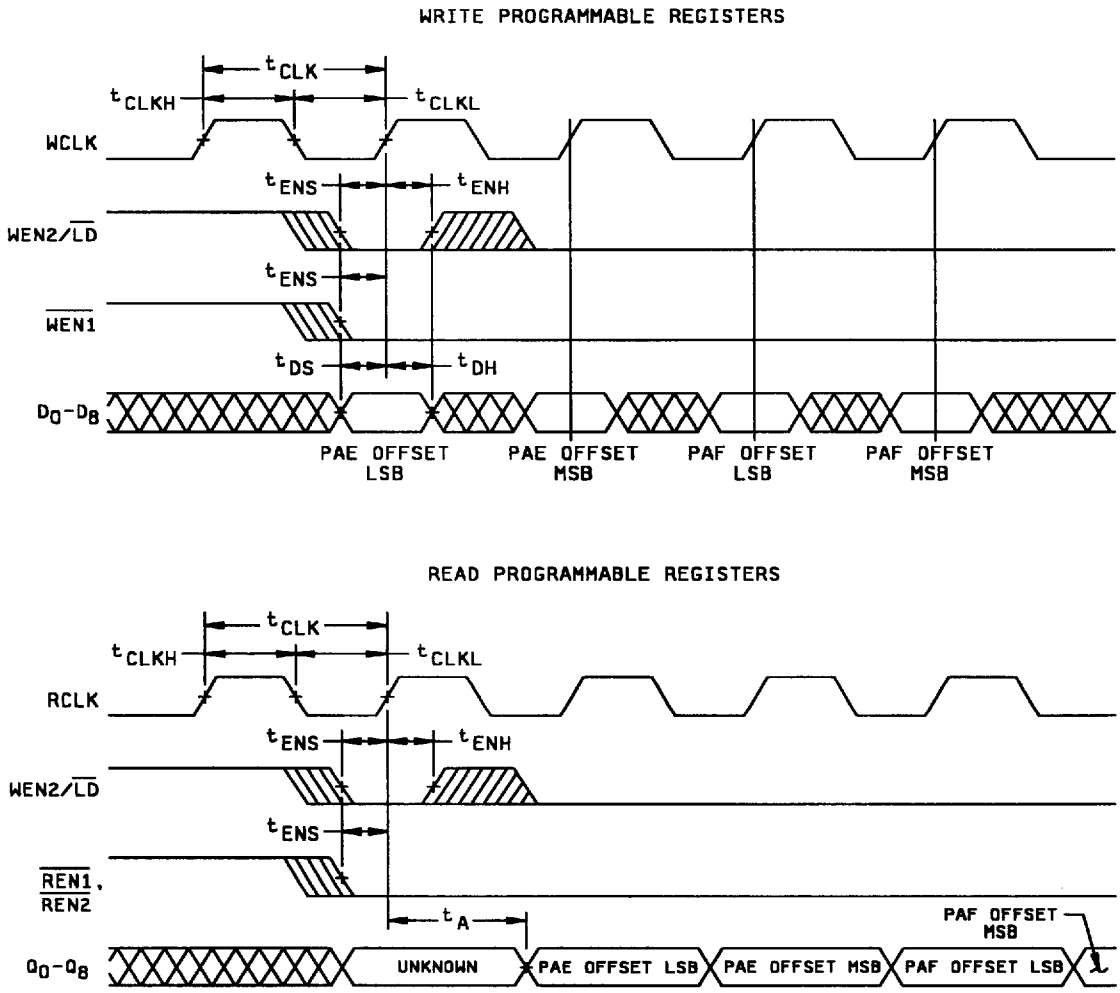


FIGURE 4. Timing waveforms - continued.

NOTES:

1. C_L = load capacitance and includes jig and probe capacitance.
2. The clocks (RCLK, WCLK) can be free-running during reset.
3. Holding WEN2/$\overline{LD}$ high during reset will make the pin act as a second write enable pin. Holding WEN2/$\overline{LD}$ low during reset will make the pin act as a load enable for the programmable flag offset registers.
4. After reset, the outputs will be low if $\overline{OE}$ = low and tri-state if $\overline{OE}$ = high.
5. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go high during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.
6. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go high during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{EF}$ may not change state until the next RCLK edge.
7. When $t_{SKEW2} \geq$ the minimum limit specified in table I, t_{FRL} (maximum) = $t_{CLK} + t_{SKEW2}$. When $t_{SKEW2} <$ the minimum limit, t_{FRL} (maximum) = either $2t_{CLK} + t_{SKEW2}$ or $t_{CLK} + t_{SKEW2}$. The latency timing applies only at the empty boundary ($\overline{EF}$ = LOW).
8. If a write is performed on this rising edge of the write clock, there will be Full-(m-1) words in the FIFO when $\overline{PAF}$ goes low.
9. 32768 - m words.
10. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then $\overline{PAF}$ may not change state until the next WCLK edge.
11. $\overline{PAE}$ offset = n.
12. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{PAE}$ to change state during the clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{PAE}$ may not change state until the next RCLK rising edge.
13. If a read is performed on this rising edge of the read clock, there will be Empty+n-1 words in the FIFO when $\overline{PAE}$ goes low.
14. The first word is available the cycle after $\overline{EF}$ goes HIGH, always.
15. $\overline{PAF}$ offset = m.

FIGURE 4. Timing waveforms - continued.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (per method 5005, table I)	Subgroups (per MIL-I-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9	1,7,9
2	Static burn-in I method 1015	Not required	Not required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11
7	Group A test requirements	1,2,3,4**,7,8A ,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B	1,2,3,7, 8A,8B,9,10, 11 Δ
9	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Test 1/	All device types
I_{LI}	±10% of specified value in table I
I_{LO}	±10% of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

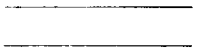
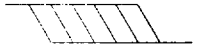
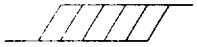
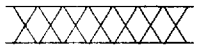
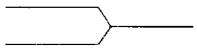
6.3 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Symbols, definitions, and functional descriptions.

Symbol	Name	I/O	Description
D0-D8	Data Inputs	I	Data inputs for an 9-bit bus.
Q0-Q8	Data Outputs	O	Data ouputs for an 9 -bit bus.
$\overline{WEN1}$	Write Enable 1	I	The only write enable when device is configured to have programmable flags. Data is written on a low-to-high transition of WCLK when $\overline{WEN1}$ is asserted and $\overline{FF}$ is high. If the FIFO is configured to have two write enables, data is written on a low to high transition of WCLK when $\overline{WEN1}$ is low and WEN2/$\overline{LD}$ and $\overline{FF}$ are high.
WEN2/$\overline{LD}$ Dual mode pin	Write Enable 2 Load	I	If high at reset, this pin operates as a seconrd write enable. If low at reset, this pin operates as a control to write or read the programmable flag offsets.$\overline{WEN1}$ must be low and WEN2 must be high to write data into the FIFO. Data will not be written into the FIFO if the $\overline{FF}$ is low. If the FIFO is configured to have programmable flags, WEN2/$\overline{LD}$ is held low to write or read the programmable flag offsets.
$\overline{REN1}$, $\overline{REN2}$	Read enable inputs	I	Enable the device for read operation. Both $\overline{REN1}$ and $\overline{REN2}$ must be asserted to allow a read operation.
WCLK	Write Clock	I	The rising edge clocks data into the FIFO when $\overline{WEN1}$ is low and WEN2/$\overline{LD}$ is high and the FIFO is not full. When $\overline{LD}$ is asserted, WCLK writes data into the programmable flag-offset register.
RCLK	Read Clock	I	The rising edge clocks data out of the FIFO when $\overline{REN1}$ and $\overline{REN2}$ are low and the FIFO is not empty. When WEN2/$\overline{LD}$ is low, RCLK reads data out of the programmable flag-offset register.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is low, the FIFO is empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is low, the FIFO is full. $\overline{FF}$ is synchronized to WCLK.
$\overline{PAE}$	Programmable almost empty	O	When $\overline{PAE}$ is low, the FIFO is almost empty based on the almost empty offset value programmed into the FIFO. $\overline{PAE}$ is synchronized to RCLK.
$\overline{PAF}$	Programmable almost full	O	When $\overline{PAF}$ is low, the FIFO is almost full based on the almost full offset value programmed into the FIFO. $\overline{PAF}$ is synchronized to WCLK.
$\overline{RS}$	Reset	I	Resets device to empty condition. A reset is required before an initial read or write operation after power-up.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is low, the data outputs drive the bus to which they are connected. If $\overline{OE}$ is high, the output data bus will be in a high impedance state.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 98-09-11

Approved sources of supply for SMD 5962-97631 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9763101QXA	65786	CY7C4271-15LMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for the part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65786	Cypress Semiconductor 3901 North First Street San Jose, CA 95134-1599

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.