TRSF3222E 3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH ±15-kV ESD PROTECTION

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FEATURES

- ESD Protection for RS-232 Bus Pins
 - ±15-kV Human-Body Model (HBM)
 - ±8-kV IEC 61000-4-2, Contact Discharge
 - ±15-kV IEC 61000-4-2, Air-Gap Discharge
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates With 3-V to 5.5-V V_{CC} Supply
- · Operates up to 1000 kbit/s
- Two Drivers and Two Receivers
- Low Standby Current . . . 1 μΑ Typ
- External Capacitors . . . 4 × 0.1 μF
- Accepts 5-V Logic Input With 3.3-V Supply

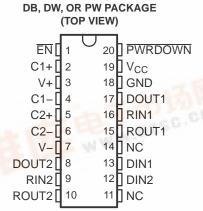
APPLICATIONS

- Battery-Powered Systems
- PDAs
- Notebooks
- Laptops
- Palmtop PCs
- Hand-Held Equipment

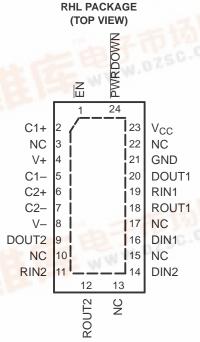
DESCRIPTION/ ORDERING INFORMATION

The TRSF3222E consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND).

The TRSF3222E meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The TRSF3222E operates at typical data signaling rates up to 1000 kbit/s and is an improved drop-in replacement for industry-popular '3222 two-driver, two-receiver functions.



NC - No internal connection



NC - No internal connection

The TRSF3222E can be placed in the power-down mode by setting the power-down ($\overline{PWRDOWN}$) input low, which draws only 1 µA from the power supply. When the device is powered down, the receivers remain active while the drivers are placed in the high-impedance state. Also, during power down, the onboard charge pump is disabled; V+ is lowered to V_{CC} , and V- is raised toward GND. Receiver outputs also can be placed in the high-impedance state by setting enable (\overline{EN}) high.

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Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TRSF3222E

3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH ±15-kV ESD PROTECTION



ORDERING INFORMATION

T _A	PAC	CKAGE ⁽¹⁾⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SOIC - DW	Tube of 25	TRSF3222ECDW	TRSF3222EC
	SOIC - DW	Reel of 2000	TRSF3222ECDWR	TROF3222EC
0°C to 70°C	SSOP – DB	Tube of 70	TRSF3222ECDB	RT22EC
0-0 10 70-0	220b – DB	Reel of 2000	TRSF3222ECDBR	RIZZEC
	TSSOP – PW	Tube of 70	TRSF3222ECPW	RT22EC
	1330P – PW	Reel of 2000	TRSF3222ECPWR	RIZZEC
	SOIC - DW	Tube of 25	TRSF3222EIDW	TRSF3222EI
	SOIC - DW	Reel of 2000	TRSF3222EIDWR	TROF3222EI
40°C to 95°C	SSOP – DB	Tube of 70	TRSF3222EIDB	DTOOF
–40°C to 85°C	220b – DB	Reel of 2000	TRSF3222EIDBR	RT22EI
	TOOD DW	Tube of 70	TRSF3222EIPW	RT22EI
	TSSOP – PW Reel of 2000		TRSF3222EIPWR	K 122E1

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLES

Each Driver(1)

IN	PUTS	OUTPUT
DIN	PWRDOWN	DOUT
X	L	Z
L	Н	Н
Н	Н	L

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

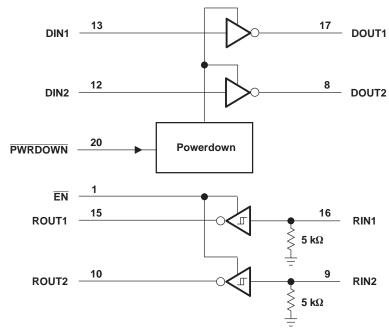
Each Receiver(1)

INP	UTS	OUTPUT
RIN	EN	ROUT
L	L	Н
Н	L	L
X	Н	Z
Open	L	Н

(1) H = high level, L = low level, X = irrelevant,Z = high impedance (off), Open = input disconnected or connected driver off

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LOGIC DIAGRAM (POSITIVE LOGIC)(1)



(1) Pin numbers shown are for the DB, DW, and PW packages.

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range ⁽²⁾		-0.3	6	V
V+	Positive-output supply voltage range (2)		-0.3	7	V
V-	Negative-output supply voltage range (2)		0.3	-7	V
V+ - V-	Supply voltage difference ⁽²⁾			13	V
VI	land to the same	Driver (EN, PWRDOWN)	-0.3	6	
	Input voltage range	Receiver	-25	25	V
.,	Output valtage range		-13.2	13.2	V
Vo	Output voltage range	Receiver	-0.3	V _{CC} + 0.3	V
		DB package		70	
0	Package thermal impedance (3)(4)	DW package		58	°C/W
θ_{JA}	Package thermal impedance (**/**)	PW package		83	°C/VV
		RHL package		TBD	
T_{J}	Operating virtual junction temperature			150	°C
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ All voltages are with respect to network GND.

⁽³⁾ Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.

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Recommended Operating Conditions⁽¹⁾

See Figure 5

				MIN	NOM	MAX	UNIT
	Supply voltage	$V_{CC} = 3.3 \text{ V}$	3	3.3	3.6	V	
	Supply voltage		$V_{CC} = 5 V$	4.5	5	5.5	V
V	Driver and control high-level input voltage	ver and control high-level input voltage DIN, EN, PWRDOWN	$V_{CC} = 3.3 \text{ V}$	2			V
V_{IH}	Driver and Control High-level Input Voltage	DIN, EN, PVVKDOVVN	$V_{CC} = 5 V$	2.4			V
V_{IL}	Driver and control low-level input voltage	DIN, EN, PWRDOWN				8.0	>
V_{I}	Driver and control input voltage	DIN, EN, PWRDOWN		0		5.5	V
V_{I}	Receiver input voltage			-25		25	V
т	Operating free-air temperature		TRSF3222EC	0		70	ů
IA	Operating free-all temperature	TRSF3222EI	-40		85		

⁽¹⁾ Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V.

Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
I	Input leakage current (EN, PWRDOWN)			±0.01	±1	μΑ
	Supply current	No load, PWRDOWN at V _{CC}		0.3	1	mA
ICC	Supply current (powered off)	No load, PWRDOWN at GND		1	10	μΑ

⁽¹⁾ Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V. (2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

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DRIVER SECTION

Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

	PARAMETER	TEST CONDI	TEST CONDITIONS			MAX	UNIT
V_{OH}	High-level output voltage	DOUT at $R_L = 3 \text{ k}\Omega$ to GND,	DIN = GND	5	5.4		V
V_{OL}	Low-level output voltage	DOUT at $R_L = 3 \text{ k}\Omega$ to GND,	$DIN = V_{CC}$	-5	-5.4		V
I _{IH}	High-level input current	$V_I = V_{CC}$	$V_I = V_{CC}$		±0.01	±1	μΑ
I _{IL}	Low-level input current	V _I at GND			±0.01	±1	μΑ
1	Short-circuit output current ⁽³⁾	V _{CC} = 3.6 V	V _O = 0 V		±35	±60	mA
I _{OS}	Short-circuit output current	V _{CC} = 5.5 V	v _O = 0 v		±33	±00	ША
ro	Output resistance	V_{CC} , V+, and V- = 0 V,	$V_O = \pm 2 \text{ V}$	300	10M		Ω
	Output leakage current	PWRDOWN = GND	$V_{CC} = 3 \text{ V to } 3.6 \text{ V},$ $V_{O} = \pm 12 \text{ V}$			±25	
I _{OZ}		PWRDOWN = GND	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $V_{O} = \pm 10 \text{ V}$			±25	μΑ

Switching Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

	PARAMETER	TEST CONDITIONS			MIN	TYP ⁽²⁾	MAX	UNIT
		_	$C_L = 1000 \text{ pF}$		250			
	Maximum data rate (See Figure 1)	$R_L = 3 \text{ k}\Omega$, One DOUT switching	$C_L = 250 \text{ pF},$	V_{CC} = 3 V to 4.5 V	1000			kbit/s
	(CCC rigure 1)	one Boot omicining	$C_L = 1000 \text{ pF},$	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	1000			
t _{sk(p)}	Pulse skew ⁽³⁾	$C_L = 150 \text{ pF to } 2500 \text{ pF},$	$R_L = 3 \text{ k}\Omega \text{ to } 7 \text{ k}\Omega,$	See Figure 2		300		ns
	Slew rate, transition region (see Figure 1)	$R_L = 7 \text{ k}\Omega,$	C _L = 150 pF to 1000 pF		8		90	
SR(tr)		D 010	C _L = 1000 pF		12		60	V/µs
		see Figure 1) $R_L = 3 \text{ k}\Omega$			24		150	

⁽¹⁾ Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 $V \pm 0.3$ V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 $V \pm 0.5$ V. (2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C. (3) Pulse skew is defined as $|t_{PLH}|$ of each channel of the same device.

Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V. All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C. Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

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RECEIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -1 \text{ mA}$	V _{CC} - 0.6	$V_{CC} - 0.1$		V
V_{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
\/	Desitive going input threshold veltage	$V_{CC} = 3.3 \text{ V}$		1.5	2.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 5 V		1.8	2.4	V
V	Nogative going input threshold voltage	V _{CC} = 3.3 V	0.6	1.2		V
V _{IT}	Negative-going input threshold voltage	V _{CC} = 5 V	0.8	1.5		V
V_{hys}	Input hysteresis (V _{IT+} - V _{IT-})			0.3		V
I_{OZ}	Output leakage current	<u>EN</u> = 1		±0.05	±10	μA
r _i	Input resistance	$V_I = \pm 3 \text{ V to } \pm 25 \text{ V}$	3	5	7	kΩ

⁽¹⁾ Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V. (2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

Switching Characteristics⁽¹⁾

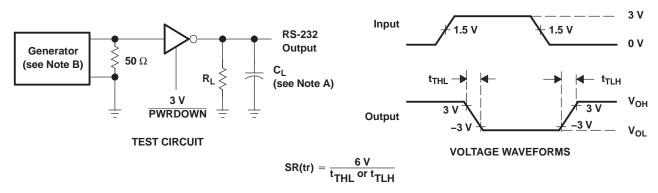
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	TYP ⁽²⁾	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150 pF, See Figure 3	300	ns
t _{PHL}	Propagation delay time, high- to low-level output	C _L = 150 pF, See Figure 3	300	ns
t _{en}	Output enable time	$C_L = 150 \text{ pF}, R_L = 3 \text{ k}\Omega, \text{ See Figure 4}$	200	ns
t _{dis}	Output disable time	$C_L = 150 \text{ pF}, R_L = 3 \text{ k}\Omega, \text{ See Figure 4}$	200	ns
t _{sk(p)}	Pulse skew ⁽³⁾	See Figure 3	300	ns

Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V. All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C. Pulse skew is defined as $|t_{PLH}-t_{PHL}|$ of each channel of the same device.

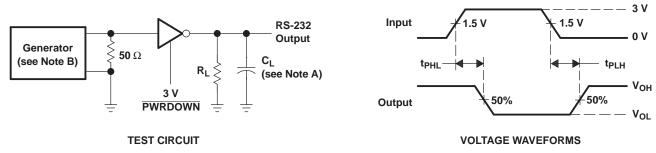
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PARAMETER MEASUREMENT INFORMATION



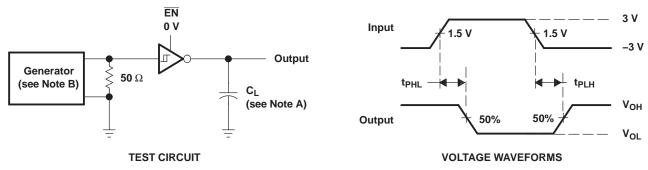
- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_0 = 50 \Omega$, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 1. Driver Slew Rate



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω , 50% duty cycle, $t_r \le$ 10 ns, $t_f \le$ 10 ns.

Figure 2. Driver Pulse Skew



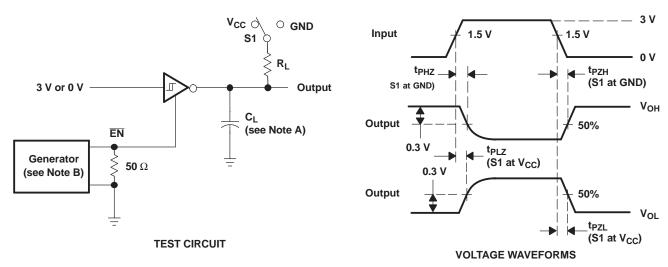
- A. C₁ includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: Z_0 = 50 Ω , 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 3. Receiver Propagation Delay Times

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PARAMETER MEASUREMENT INFORMATION (continued)

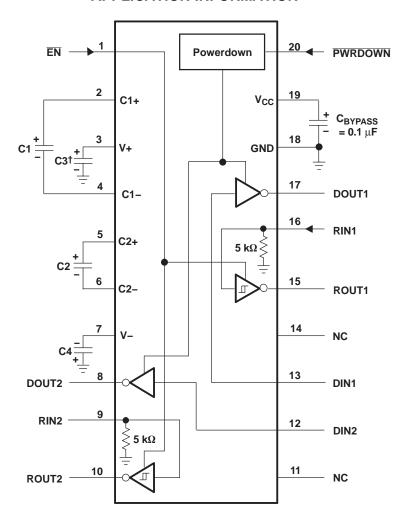


- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: Z_0 = 50 Ω , 50% duty cycle, $t_r \le 10$ ns. $t_f \le 10$ ns.

Figure 4. Receiver Enable and Disable Times

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APPLICATION INFORMATION



 † C3 can be connected to $V_{CC}\, or \, GND.$

NOTES: A. Resistor values shown are nominal.

- B. NC No internal connection
- C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V _{CC}	C1	C2, C3, and C4
3.3 V \pm 0.3 V	0.1 μ F	0.1 μ F
5 V \pm 0.5 V	0.047 μ F	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μ F

Figure 5. Typical Operating Circuit and Capacitor Values



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TRSF3222ECDB	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222ECDBG4	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222ECDBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222ECDBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222ECDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222ECDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222ECDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222ECDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222ECPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222ECPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222ECPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222ECPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222EIDB	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222EIDBG4	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222EIDBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222EIDBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222EIDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222EIDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222EIDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222EIDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222EIPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222EIPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222EIPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222EIPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:



PACKAGE OPTION ADDENDUM

26-Sep-2007

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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11-Mar-2008

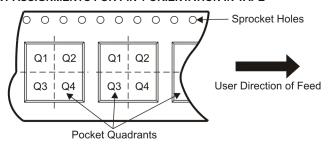
TAPE AND REEL INFORMATION



TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

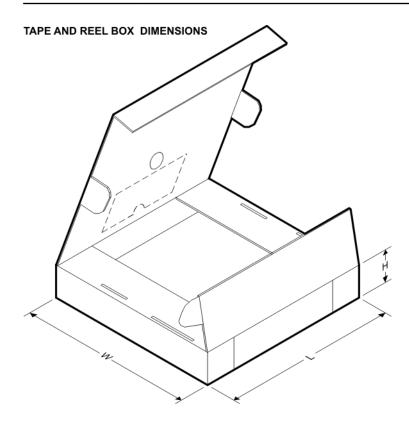
	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRSF3222ECDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
TRSF3222ECDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
TRSF3222ECPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TRSF3222EIDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
TRSF3222EIDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
TRSF3222EIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1



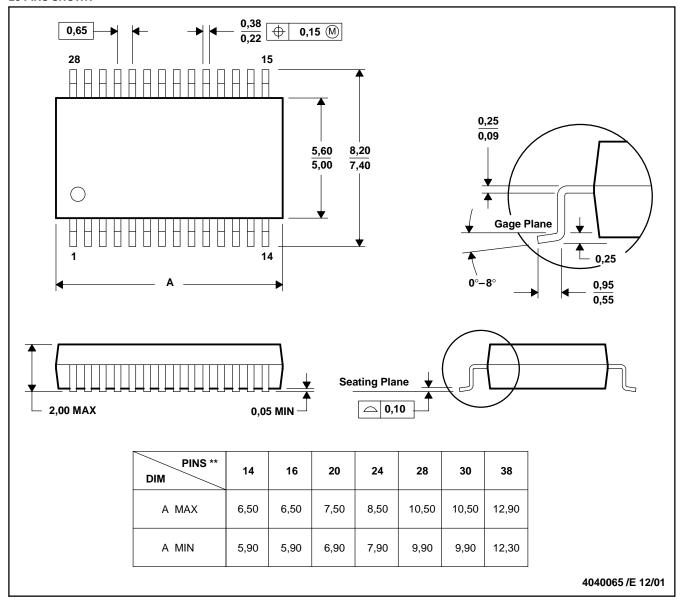
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRSF3222ECDBR	SSOP	DB	20	2000	346.0	346.0	33.0
TRSF3222ECDWR	SOIC	DW	20	2000	346.0	346.0	41.0
TRSF3222ECPWR	TSSOP	PW	20	2000	346.0	346.0	33.0
TRSF3222EIDBR	SSOP	DB	20	2000	346.0	346.0	33.0
TRSF3222EIDWR	SOIC	DW	20	2000	346.0	346.0	41.0
TRSF3222EIPWR	TSSOP	PW	20	2000	346.0	346.0	33.0

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

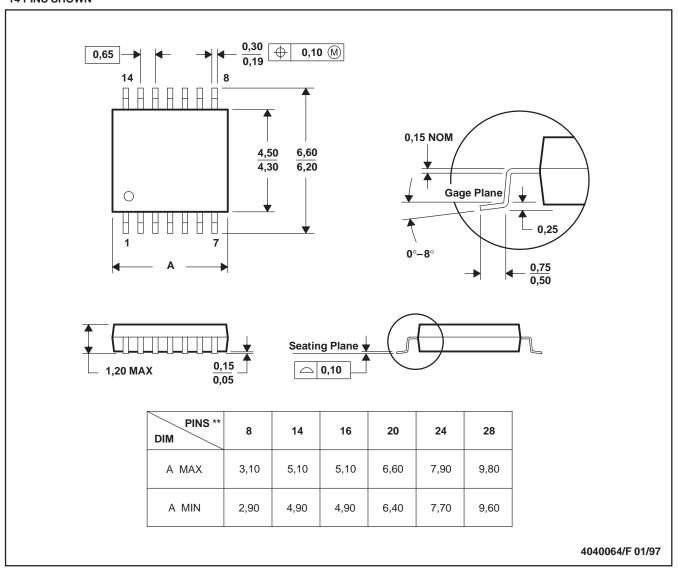
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

14 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

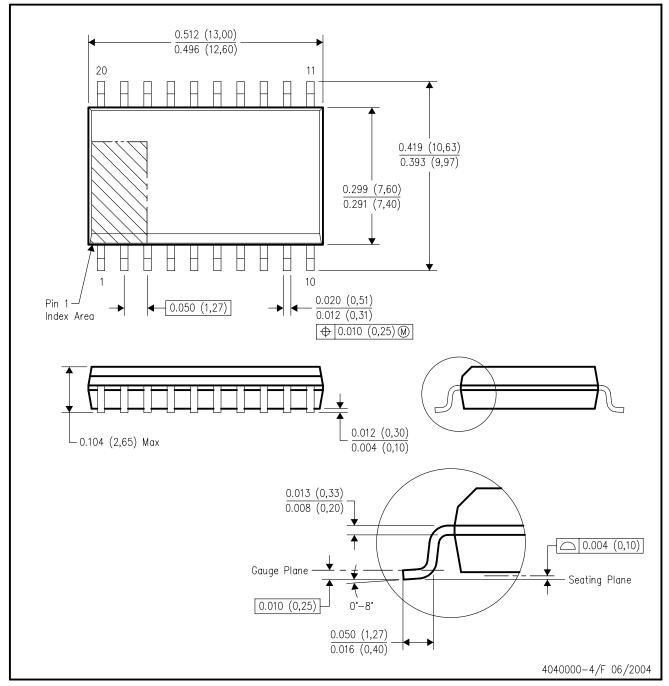
B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



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