REVISIONS

LTR	DESCRIPTION	DATE	APPROVAL
E	REV FAH61 INC 9/9/9 Replaces Rev D with change SH 1, 2	87-04-21 87-04-21	

ONLY THE PART DESCRIBED ON THIS DRAWING WHEN PROCURED FROM THE MANUFACTURERS INDICATED HEREON ARE APPROVED BY WESTINGHOUSE (97942) FOR USE IN RADIATION SENSITIVE SYSTEMS. ALTERNATE SOURCES SHALL NOT BE USED WITHOUT PRIOR NUCLEAR SURVIVABILITY TESTING AND APPROVAL BY THE S/V ENGINEERING SECTION.

Unless otherwise specified dimensions are in inches
DO NOT SCALE

Tolerances
Decimals: 2 places ± .01; 3 places ± .015
Angles: ± -

SOURCE CONTROL DRAWING

DRAWING TO BE CHANGED ONLY

BY APPROVAL OF PARTS ENGINEERING

LATEST REVLTR																									
SH NO	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50
LATEST REVLTR	E	E	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D						
SH NO	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25

SHEET REVISION STATUS

CONTRACT NO. F33657-81-C-0641
ORIGINAL DATE APVD 84-12-07
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CHKD UHLIG PARTS ENGR FRACALOSSI
APVD MUELLER APVD FOCHT
DESIGN ACTIVITY APPROVAL

PROCURING ACTIVITY APPROVAL

WESTINGHOUSE ELECTRIC CORPORATION
DEFENSE & ELECTRONIC SYSTEMS CENTER
Baltimore, MD., U.S.A. 21203

FED. SUP. CLASS 5962

MICROCIRCUIT, DIGITAL, CMOS, MULTIPLIER, 16 X 16 BIT

SIZE	FSCM NO.	DWG. NO.
A	97942	586R739

SCALE NONE WEIGHT SH 2 SHEET 1 OF 20

查询"586R739H01"供应商

WESTINGHOUSE PART NUMBER	CASE OUTLINE	APPROVED MANUFACTURERS
586R739H01	FIG. 1	A, B, C

SOURCE OF SUPPLY TABULATION

MANUFACTURERS

CODE LTR.	NAME	ADDRESS CODE H4
A	ANALOG DEVICES INC.	24355
B	INTEGRATED DEVICE TECHNOLOGY	61772
C	WEITEK CORP.	62994

SIZE	FSCM NO.	DWG NO.
A	97942	586R739

SCALE: NONE REV. E SHEET 2

1. SCOPE

1.1 Statement of scope. This drawing delineates the detailed requirements for passivated, silicon, monolithic microcircuits. Quality assurance provisions, including burn-in, to meet the military environmental and reliability requirements are also included. Device characteristics are similar to the manufacturer's part referenced in 6.1. Requirements which are specified herein but which are not specified or controlled in the manufacturer's published specification are indicated by an asterisk (*).

1.2 Physical dimensions. Physical dimensions shall be in accordance with the applicable case outline specified in the tabulation on sheet 2.

1.3 Absolute maximum ratings. The absolute maximum ratings shown herein should not be exceeded at any time during the test or operation of these devices.

Storage Temperature Range	-65 to +150C
Junction Temperature, T_J 1/	+175C
Lead Temperature (soldering, 10 seconds)	+300C
Supply Voltage, V_{CC}	-0.3 Vdc to 7.0 Vdc
Input Voltage Range	-0.3 Vdc to V_{CC}
Applied Output Voltage 2/	-0.3 Vdc to V_{CC}
Fan-out 3/	
L State	2
H State	8

1/ θ_{JC} = 7.0 C/W, θ_{JA}=20C/W

2/ Output must be in "H" or high impedance state.

3/ A fan-out of one is defined as a sink current of 2.0 mA when the output is in the "L" state and a source current of 50 uA when the output is in the "H" state.

1.4 Recommended operating conditions.

Supply Voltage, V_{CC}, Range	+4.5 Vdc to +5.5 Vdc
Ambient Operating Temperature Range	-55C to +125C

1.5 Primary electrical characteristics. See Table I.

2. APPLICABLE DOCUMENTS.

2.1 Issues of documents. The following documents, of the issue in effect on date of invitation for bids or request for proposal, form a part of this drawing to the extent specified herein.

GOVERNMENT AND NATIONALLY RECOGNIZED PUBLICATIONS

DOD-D-1000	Engineering Drawings
MIL-M-38510	Microcircuits, General Specification for
MIL-STD-883	Test Methods and Procedures for Microelectronics
H4	Federal Supply Code for Manufacturers

*3. REQUIREMENTS.

3.1 Order of precedence. This drawing takes precedence over documents referred to herein and shall be interpreted in accordance with DOD-D-1000.

3.2 General. The individual device requirements shall be in accordance with MIL-M-38510 for class B product and as specified herein. Devices are sensitive to electrostatic discharge and are classified as category A.

3.3 Design, construction, and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-M-38510 for class B product and herein.

3.3.1 Design documentation. The design documentation shall be in accordance with MIL-M-38510 and, unless otherwise specified in the contract or purchase order, shall be retained by the manufacturer but be available for review by the Procuring Agency or contractor upon request.

3.3.2 Case outline. The case outline shall be in accordance with 1.2 herein.

3.3.3 Terminal connections. The terminal connections shall be as specified on Figure 2.

3.3.4 Functional logic diagram. The device shall be functionally equivalent to the functional logic diagram shown on Figure 2 and timing diagram of Figure 3.

3.4 Lead or terminal material and finish. The lead or terminal material and finish shall be in accordance with MIL-M-38510.

3.5 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I herein and apply over the full recommended operating temperature range and recommended supply voltage range, unless otherwise specified.

3.6 Marking. Marking shall be in accordance with MIL-M-38510 except the part number shall be as follows:

Westinghouse H4 code identification number (97942) followed by a dash and the Westinghouse part number.

Example: 97942-586R739H01 or 97942-586R739H01 or 97942-586R739 H01

3.7 Product assurance requirements. Microcircuits furnished under this drawing shall have been subjected to, and passed all the requirements, tests, and inspections detailed herein including screening and quality conformance inspections.

3.7.1 Screening. Screening shall be in accordance with Method 5004 of MIL-STD-883 for class B product and 4.2 herein.

3.7.2 Qualification. Qualification inspection for the device type(s) specified herein shall not be required.

3.7.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 for class B product and 4.4 herein.

3.7.4 Chance in design or process. No change in device design, material, process or control shall be implemented without concurrent change to all affected documents, including the product assurance program documentation. The manufacturer shall notify the Procuring Agency of any major change of the product or product assurance program and obtain Procuring Agency approval before changed devices are shipped on the contract or purchase order. Such notification shall include a written detailed description of the change and data to demonstrate that the change will not adversely affect reliability, quality, performance, or interchangeability and that the changed product will continue to meet the requirements of this specification. The Procuring Agency will review the submitted change notification and, based upon the review, will approve or disapprove the change and notify the manufacturer. At the manufacturer's option, devices incorporating the changes may be manufactured and tested prior to Procuring Agency approval; however, all shipments of these devices shall be witheld until approval is granted by the Procuring Agency.

Major changes which are subjected to this requirement are those listed in MIL-M-38510 paragraph 3.4.2.

3.8 Functional test program. The supplier's test program shall be available for review at the supplier's facility by the Procuring Agency upon request. The test program shall be in report form or a print out of the test tape for computer controlled test equipment.

*4. QUALITY ASSURANCE PROVISIONS.

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and Method 5005 of MIL-STD-883 for class B product except as modified herein. For lots held more than 36 months, see reinspection procedures in 4.2 of MIL-M-38510.

4.2 Screening. Screening shall be in accordance with Method 5004 of MIL-STD-883 for class B product and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

(A) Burn-in test (Method 1015 of MIL-STD-883).

(1) Test condition A, B, C, D or E.

(2) T_A = 125C, minimum.

(B) Interim and final electrical test parameters shall be as specified in Table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

(C) Percent Defective Allowable (PDA) shall be as specified in MIL-M-38510.

4.3 Qualification inspection. Qualification inspection for the device type(s) specified herein shall not be required.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 for class B product. Groups A and B inspections shall be performed on each lot or as specified in MIL-STD-883, Method 5005. Manufacturers shall keep lot records for 3 years (minimum), monitor for compliance to the prescribed procedures, and observe that satisfactory manufacturing conditions and records on lots are maintained for these devices. The records, including as a minimum an attributes summary of all screening and quality conformance inspections conducted on each lot, shall be available for review by the Procuring Agency upon request.

4.4.1 Group A inspection. Group A inspection shall consist of the test subgroups and LTPD values shown in Table I of Method 5005 of MIL-STD-883 for class B product and as follows:

(A) Tests shall be as specified in Table II herein.

(B) Subgroups 4, 5 and 6 of Table I of Method 5005 of MIL-STD-883 shall be omitted.

(C) Subgroups 7 and 8 tests sufficiently to verify the truth table.

(D) Subgroup 10 and 11 tests need not be performed provided the conditions and limits specified in Table I herein are guaranteed.

(E) Group A inspection may be satisfied by combinational testing using the following LTPD's:

SUBGROUPS COMBINED)	COMBINED LTPD	MAX ACCEPT NO.	TEMP (C)
1 and 7	2	2	25
2 and 8	3	2	125
3 and 8	5	2	-55

4.4.2 Group B inspection. Group B inspection shall be as specified in Method 5005 of MIL-STD-883 for class B product except subgroup 8 need not be performed (see 3.2 herein).

4.4.3 Groups C and D inspections. Groups C and D inspections shall be as specified in Method 5005 of MIL-STD-883 for class B product and as follows:

(A) Groups C and D inspections are required on the initial order by each approved supplier and need not be performed on a periodic basis unless device changes warrant testing (see 4.4.3(E)).

(B) Generic test data may be used to satisfy the requirements for groups C and D inspections (see 4.6).

(C) End-point electrical parameters shall be as specified in Table II herein.

(D) Operating life test (Method 1005 of MIL-STD-883) conditions

(1) Test condition A, B, C, D, or E.

(2) T_A = 125C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and Method 1005 of MIL-STD-883.

(E) When a change to device design or processing is approved by the Procuring Agency, partial or complete group C and/or D testing may be required, depending on the nature of the change. The Procuring Agency shall determine the specific testing required and so notify the manufacturer.

4.5 Inspection of packaging. Inspection of packaging shall be in accordance with MIL-M-38510 except that the rough handling test shall not apply.

4.6 Generic test data. Generic test data may be used to satisfy the requirements of 4.4.3. Generic test data is defined as test data from devices manufactured during the same time period, by means of the same production technique, materials, controls and design, and in the same microcircuit group (see 3.1.3 of MIL-M-38510) as the deliverable devices. The same time period shall be interpreted as covering a maximum span of 180 days between the generic test sample fabrication and the fabrication of deliverable devices. The vendor is required to retain generic data for a period of not less than 36 months from the date of shipment.

*5. PACKAGING.

5.1 Packaging requirements. The requirements for packaging and package marking shall be in accordance with MIL-M-38510 and herein. Unless otherwise specified, packaging shall be to level C and shall include the requirements for category A devices (see 5.1 of MIL-M-38510).

5.2 Unit container marking. The unit container shall be marked with the following information:

(A) Westinghouse part number (see 3.6 herein).

(B) The actual manufacturer's name, registered trademark or H4 code identification number.

(C) Date code (plus lot control letter when applicable) or manufacturing code number (traceable to the device inspection and/or control tab.

(D) "ES/EM SHIELDED" (or equivalent).

For lots held over 36 months, a reinspection date code shall be added to the initial container (see 3.6.10 of MIL-M-38510).

5.3 Exterior shipping container marking. The exterior container shall be marked with the following information:

(A) The Procuring Agency's purchase order number.

(B) The manufacturer's name, registered trademark or H4 federal code identification number.

6. NOTES

6.1 Similarity. This drawing is for a selected item that is similar to the manufacturer's part shown below. No guarantees are made of interchangeability.

ITEM	MANUFACTURER'S PART NUMBER
H01	1016/7216

SIZE	FSCM NO.	DWG NO.
A	97942	586R739

SCALE:	REV. D	SHEET 8

6.2 Approved sources of supply. Identification of approved source(s) herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item described on the drawing.

6.3 Westinghouse internal.

6.3.1 Purchasing. A copy of this drawing should accompany each purchase order or invitation to quote.

6.3.2 Engineering, Manufacturing and Receiving Inspection.

6.3.2.1 Absolute maximum ratings. Absolute maximum ratings (see 1.3 herein) should not be exceeded during the test or operation of the device.

6.3.2.2 Handling. These devices must be handled with precautions to avoid damage due to accumulation of static charge. The handling practices described in Westinghouse (97942) process specification PS85171GR must be adhered to.

TABLE I. Electrical performance characteristics.

TEST	SYMBOL	CONDITION 1/	GROUP A SUB-GROUPS	PART NO.	LIMITS MIN	LIMITS MAX	UNITS
High-level output voltage	V_{OH}	V_{CC} = 4.5 Vdc I_{OH} = -0.4 mAdc	1,2,3	All	2.4	-	Vdc
Low-level output level	V_{OL}	V_{CC} = 4.5 Vdc, I_{OL} = 4.0 mAdc	1,2,3	All	-	0.5	Vdc
Input current, low-level	I_{IL}	V_{CC} = 5.5 Vdc, V_{IL} = 0 Vdc 2/	1,2,3	All	-	-10	uAdc
Input current, high-level	I_{IH}	V_{CC} = 5.5 Vdc, V_{IH} = 5.0 Vdc 3/	1,2,3	All	-	10	uAdc
Off-state output current, low level	I_{OZL}	V_{CC} = 5.5 Vdc V_{OZL} = 0.4 Vdc, Trim = Tril = V_{IH}	1,2,3	All	-	-50	uAdc
Off-state output current, high level	I_{OZH}	V_{CC} = 5.5 Vdc, V_{OZH} = 5.5 Vdc, Trim = Tril = V_{IH}	1,2,3	All	-	50	uAdc
Supply current	I_{CC1}	V_{CC} = 5.5 Vdc, 4/ All inputs at V_{IL}	1,2,3	All	-	80	mAdc
Supply current	I_{CC2}	V_{CC} = 5.5 Vdc, 4/ All inputs at V_{IH}	1,2,3	All	-	80	mAdc
Quiescent supply current	I_{CC3}	V_{CC} = 5.5 Vdc, Trim = Tril = 5.0 Vdc, All other inputs = 0 Vdc	1,2,3	All	-	2.0	mAdc
Quiescent supply current	I_{CC4}	V_{CC} = 5.5 Vdc, All inputs = 2.4 Vdc	1,2,3	All	-	40	mAdc
Functional tests	See 4.4.1(C) 5/		7,8	All	See 4.4.1(C)		-
Output delay time	t_D	5/, 6/, Load 1	9,10,11	All	-	45	ns

TABLE I - Electrical performance characteristics (contd).

TEST	SYMBOL	CONDITION 1/	GROUP A SUB-GROUPS	PART NO.	LIMITS MIN	LIMITS MAX	UNITS
Output disable time	t_{DIS},	5/, 6/, Load 2	9,10,11	All	-	45	ns
Output enable time	t_{ENA},	5/, 6/, Load 2	9,10,11	All	-	45	ns
Clocked multiply time	t_{MC},	5/, 6/, Load 1	9,10,11	All	-	180	ns
Unclocked multiply time	t_{MUC},	5/,6/, Load 1	9,10,11	All	-	225	ns

NOTES: 1/ -55C $\leq T_A \leq$ 125C, 4.5 Vdc $\leq V_{CC} \leq$ 5.5 Vdc, V_{IH} = 2.0 Vdc and V_{IL} = 0.8 Vdc, unless otherwise specified.

2/ Unspecified inputs are connected to V_{IH}.

3/ Unspecified inputs are connected to V_{IL}.

4/ Clock cycle = 6.0 MHz minimum.

5/ Tests may be performed at V_{CC} = 4.5 Vdc provided the manufacturer guarantees that the devices meet limits specified when tested at 4.5 Vdc $\leq V_{CC} \leq$ 5.5 Vdc.

6/ Switching times shall be measured with the device operated as specified in Figure 3 and herein. Timing conditions and output loads shall be as specified in Figure 4. Amplitude = 0V to 3V.

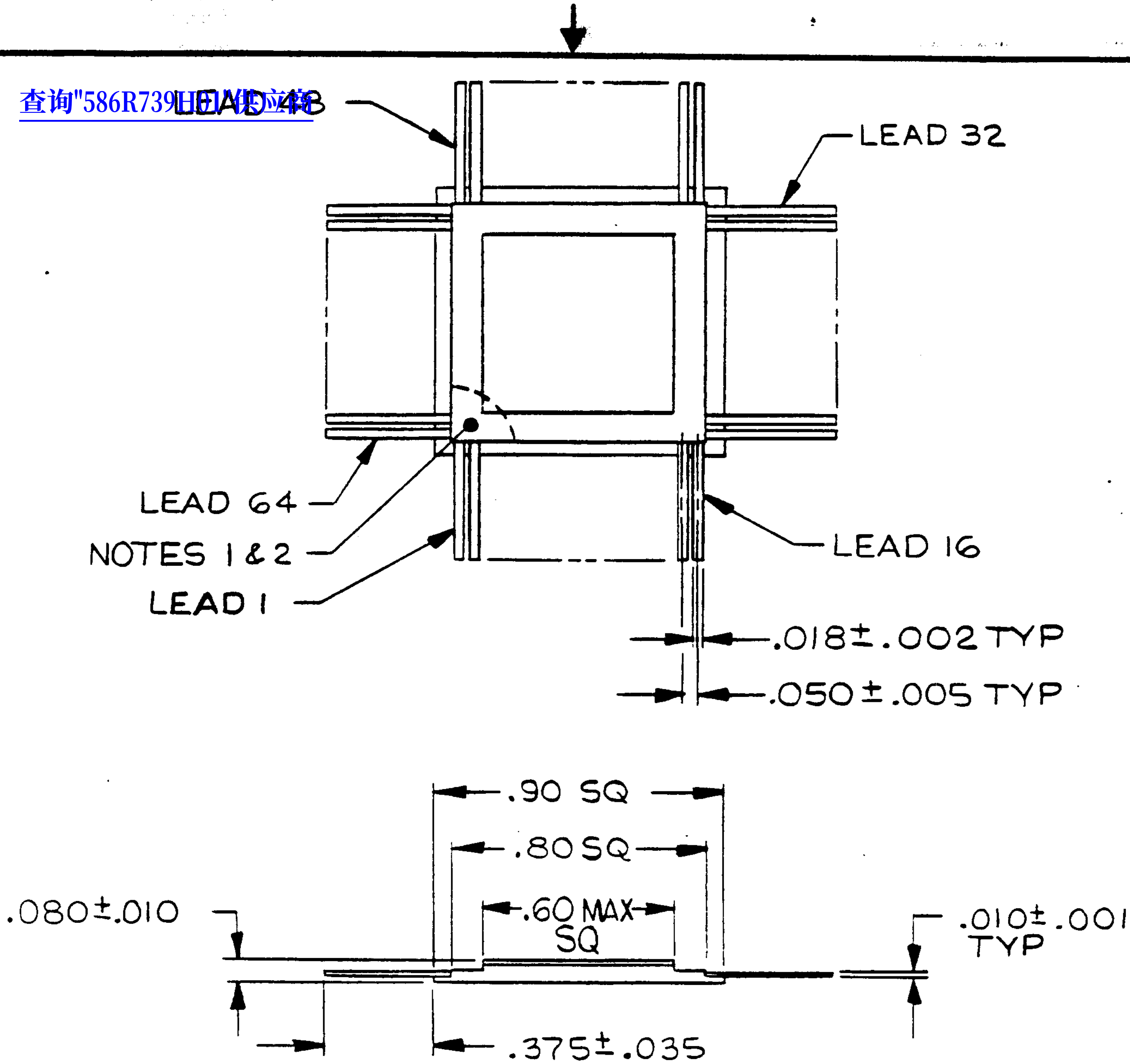
TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Group A Subgroups 1/ (per Method 5005, Table I)
Interim electrical parameters (pre-burn-in) (Method 5004)	1, 7
Final electrical test parameters (Method 5004)	1*, 2, 7, 9
Group A test requirements (Method 5005)	1, 2, 3, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (Method 5005)	1, 2, 3

* PDA applies to subgroup 1 (see 4.2c).

**Subgroups 10 and 11 need not be tested provided the manufacturer guarantees the conditions and limits specified (see 4.4.1 (D)).

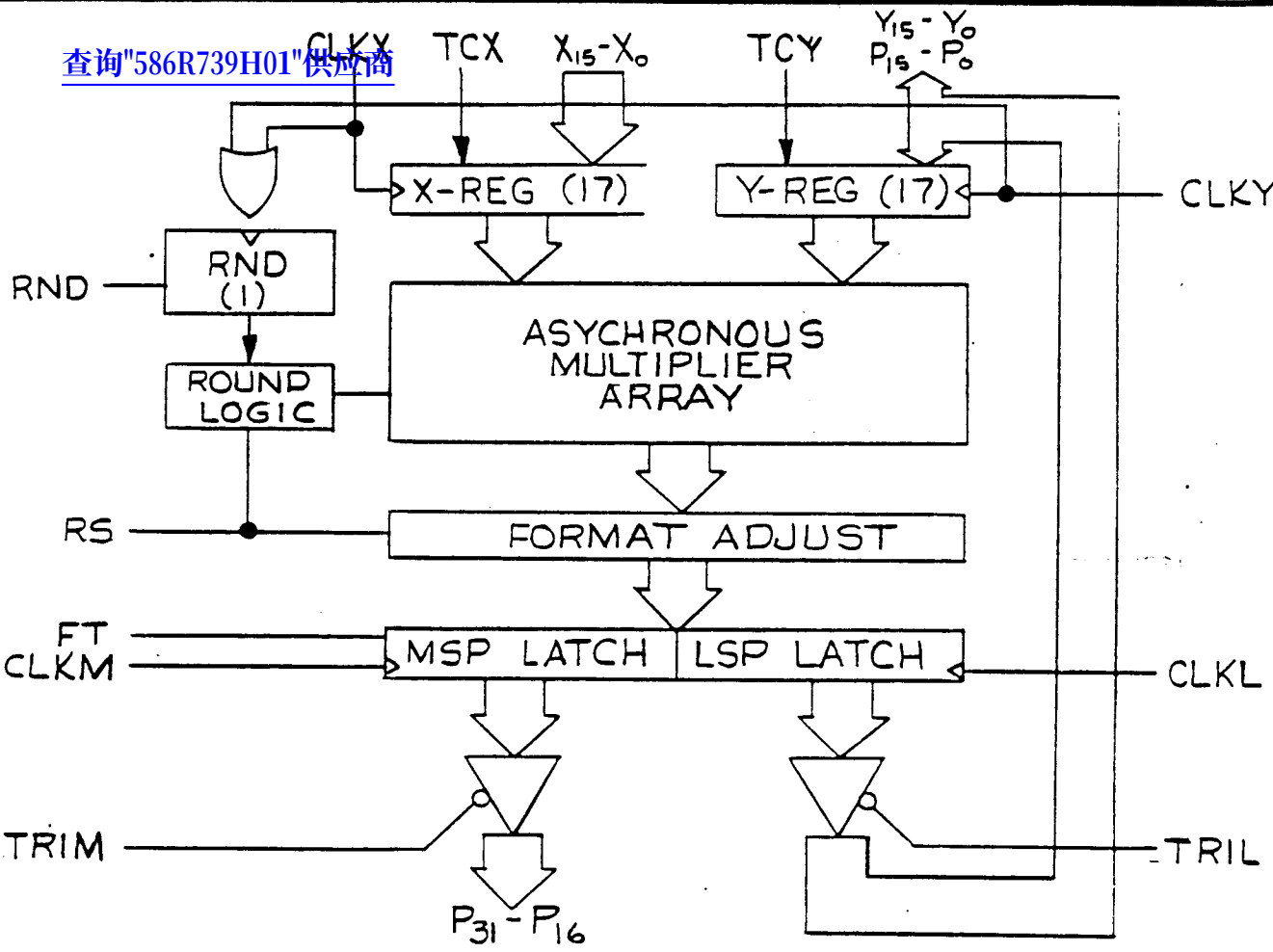
1/ Individual tests, conditions and limits required in each Group A Subgroup shall be as shown in Table I of this drawing.



NOTES:
1. Terminal identification numbers need not appear on package.
2. Terminal one shall be identified by the numeral one (1), a mechanical index on the lead or body or a mark on the top surface, within the region shown.
3. Weight: 3.0 grams maximum.
4. No epoxy or polymeric material shall be used for package lid/ seal attach.

FIGURE 1 - OUTLINE DIMENSIONS

SIZE	FSCM NO.	DWG NO.
A	97942	586R739
SCALE NONE	REV D	SHEET 13



NOTES: Controls (Positive Logic)

CLKX = X_{IN} Register/Latch Clock

CLKY = Y_{IN} Register/Latch Clock

CLKL = LSP Register/Latch Clock
CLKM = MSP Register/Latch Clock
TRIL = LSP Three-State Control
TRIM = MSP Three-State Control
RS = Right Shift MSP word down 1 bit, removes LSP sign bit.
FT = Feedthrough. Makes output latch transparent.
TCX, TCY = Denotes respective input words as two's complement (Logic H) or magnitude (logic L) data format (Registered control inputs strobed by respective clocks).
RND = Round = Adds 1 to MSB bit of LSP word, regardless of shift position (Registered control input strobed by CLKX or CLKY).

FIGURE 2A - LOGIC BLOCK DIAGRAM

FIGURE 2 - LOGIC BLOCK DIAGRAM AND TERMINAL CONNECTIONS

SIZE	FSCM NO.	DWG NO.
A	97942	586R739
SCALE —	REV D	SHEET 14

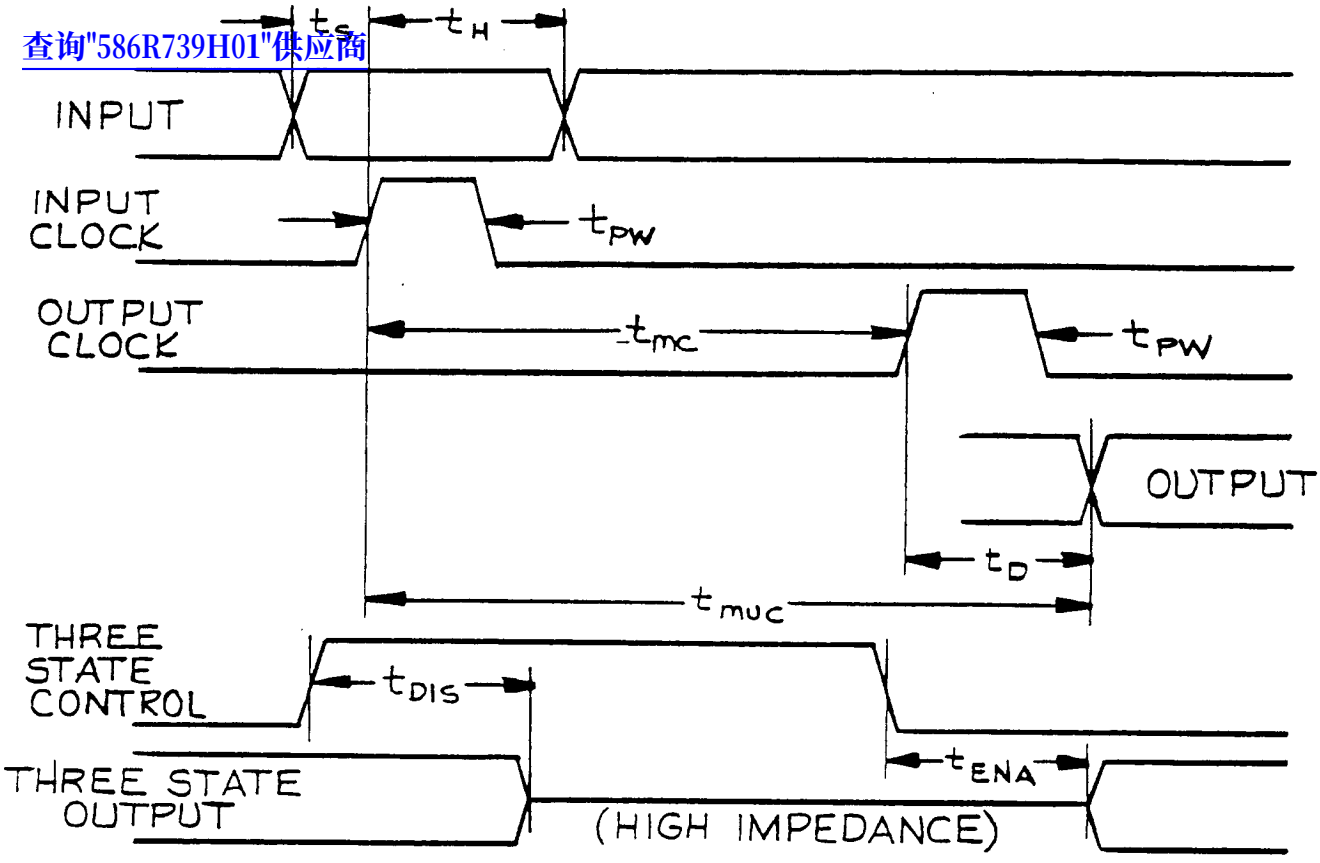
TERMINAL NUMBER		FUNCTION	TERMINAL NUMBER		FUNCTION
1	P_{31}		33	CLK Y	
2	P_{30}		34	CLK L	
3	P_{29}		35	TRIL	
4	P_{28}		36	X_0	
5	P_{27}		37	X_1	
6	P_{26}		38	X_2	
7	P_{25}		39	X_3	
8	P_{24}		40	X_4	
9	P_{23}	MSP OUTPUTS	41	X_5	
10	P_{22}		42	X_6	
11	P_{21}		43	X_7	
12	P_{20}		44	X_8	
13	P_{19}		45	X_9	X INPUTS
14	P_{18}		46	X_{10}	
15	P_{17}		47	X_{11}	
16	P_{16}		48	X_{12}	
17	P_{15} P_{15}		49	X_{13}	
18	P_{14}, Y_{14}		50	X_{14}	
19	P_{13}, Y_{13}		51	X_{15}	
20	P_{12}, Y_{12}		52	CLK X	
21	P_{11}, Y_{11}		53	RND	
22	P_{10}, Y_{10}		54	TCX	
23	P_9, Y_9		55	TCY	
24	P_8, Y_8		56	VCC	
25	P_7, Y_7	LSP OUTPUTS/Y	57	VCC	
26	P_6, Y_6	INPUTS	58	GND	
27	P_5, Y_5		59	GND	
28	P_4, Y_4		60	GND	
29	P_3, Y_3		61	FT	
30	P_2, Y_2		62	RS	
31	P_1, Y_1		63	TRIM	
32	P_0, Y_0		64	CLK M	

FIGURE 2B - TERMINAL CONNECTIONS

FIGURE 2 - LOGIC BLOCK DIAGRAM AND TERMINAL CONNECTIONS (CONTD)

SIZE	FSCM NO.	DWG NO.
A	97942	586R739

SCALE: NONE REV. D SHEET 15



A. GENERAL.

Devices are parallel array multipliers with double precision or single precision (uniform rounded or truncated) outputs.

The input registers are positive edge-triggered latches. The output latches are similarly positive edge-triggered latches, with a feedthrough control line which allows the user to bypass the registers completely, making them asynchronous. If the output clocks are disabled, then the feedthrough control can be used to convert the output registers to level latches.

The multipliers can operate with two's complement, unsigned magnitude, and mixed mode input formats. As such, they are ideal for expansion into larger multipliers, such as 32 by 32 bits, or 36 by 36 bits.

FIGURE 3 - TIMING DIAGRAM AND FUNCTIONAL DESCRIPTION

SIZE	FSCM NO.	DWG NO.
A	97942	586R739
SCALE —	REV D	SHEET 16

B. INPUT/OUTPUT FORMATS

I. INTEGER MAGNITUDE

X_{IN} — TCX = 0

X_{15}	X_{14}	X_{13}	…	X_2	X_1	X_0
2^{15}	2^{14}	2^{13}	…	2^2	2^1	2^0

TCY = 0 — Y_{IN}

Y_{15}	Y_{14}	Y_{13}	…	Y_2	Y_1	Y_0
2^{15}	2^{14}	2^{13}	…	2^2	2^1	2^0

MSP

P_{31}	P_{30}	P_{29}	…	P_{18}	P_{17}	P_{16}
2^{31}	2^{30}	2^{29}	…	2^{18}	2^{17}	2^{16}

RS = 1

LSP

P_{15}	P_{14}	P_{13}	…	P_2	P_1	P_0
2^{15}	2^{14}	2^{13}	…	2^2	2^1	2^0

NOTE: 1/ When doing unsigned magnitude or mixed mode multiplications, RS must be a 1 to get a valid product.

2/ When doing mixed mode (two's complement times unsigned magnitude) multiplies, P_{31} is the product sign bit.

FIGURE 3 - TIMING DIAGRAM AND FUNCTIONAL DESCRIPTION (CONTD)

2. FRACTIONAL TWO'S COMPLEMENT

X_{IN} TCX = 1

X_{15}	X_{14}	X_{13}	X_2	X_1	X_0
X SGN	2^{-1}	2^{-2}	2^{-13}	2^{-14}	2^{-15}

TCY = 1 Y_{IN}

Y_{15}	Y_{14}	Y_{13}	Y_2	Y_1	Y_0
YSGN	2^{-1}	2^{-2}	2^{-13}	2^{-14}	2^{-15}

MSP							LSP					
P_{31}	P_{30}	P_{29}		P_{18}	P_{17}	P_{16}		P_{15}	P_{14}	P_{13}	P_2	P_1	P_0
-2^0 SGN	2^{-1}	2^{-2}		2^{-13}	2^{-14}	2^{-15}	RS = 0	-2^0 SGN	2^{-16}	2^{-17}	2^{-28}	2^{-29}	2^{-30}
-2^1 SGN	2^{-0}	2^{-1}		2^{-12}	2^{-13}	2^{-14}	RS = 1	2^{-15}	2^{-16}	2^{-17}	2^{-28}	2^{-29}	2^{-30}

$$X = -1*X_{SIGN} + \sum_{n=1}^{15} X_n 2^{-n} \qquad P = -1*P_{SIGN} + \sum_{N=1}^{30} P_n 2^{-n}$$

The resulting values for X and P given in the above evaluation (Y is expressed in the same manner as X) are in fractional two's complement format. The value for the sign variable is 0 for the positive or zero numbers and 1 for negative numbers.

RS = 0 An overflow occurs in the attempted multiplication of the two's complement number 1.0000 ... (-1 base 10) with itself, yielding a result of the same number, i.e.,

$$(-1)_{10} * (-1)_{10} = (-1)_{10}$$

The product sign bit is available redundantly as MSB of both the MSP and LSP words.

RS = 1 No overflow occurs when multiplying $-1_{(10)}$ times $-1_{(10)}$. The product is a true $+1.0_{(10)}$; i.e., product bit P_{30} is a 1, all other bits are 0.

FIGURE 3 - TIMING DIAGRAM AND FUNCTIONAL DESCRIPTION (CONTD)

SIZE	FSCM NO.	DWG NO.
A	97942	586R739
SCALE -	REV D	SHEET 18

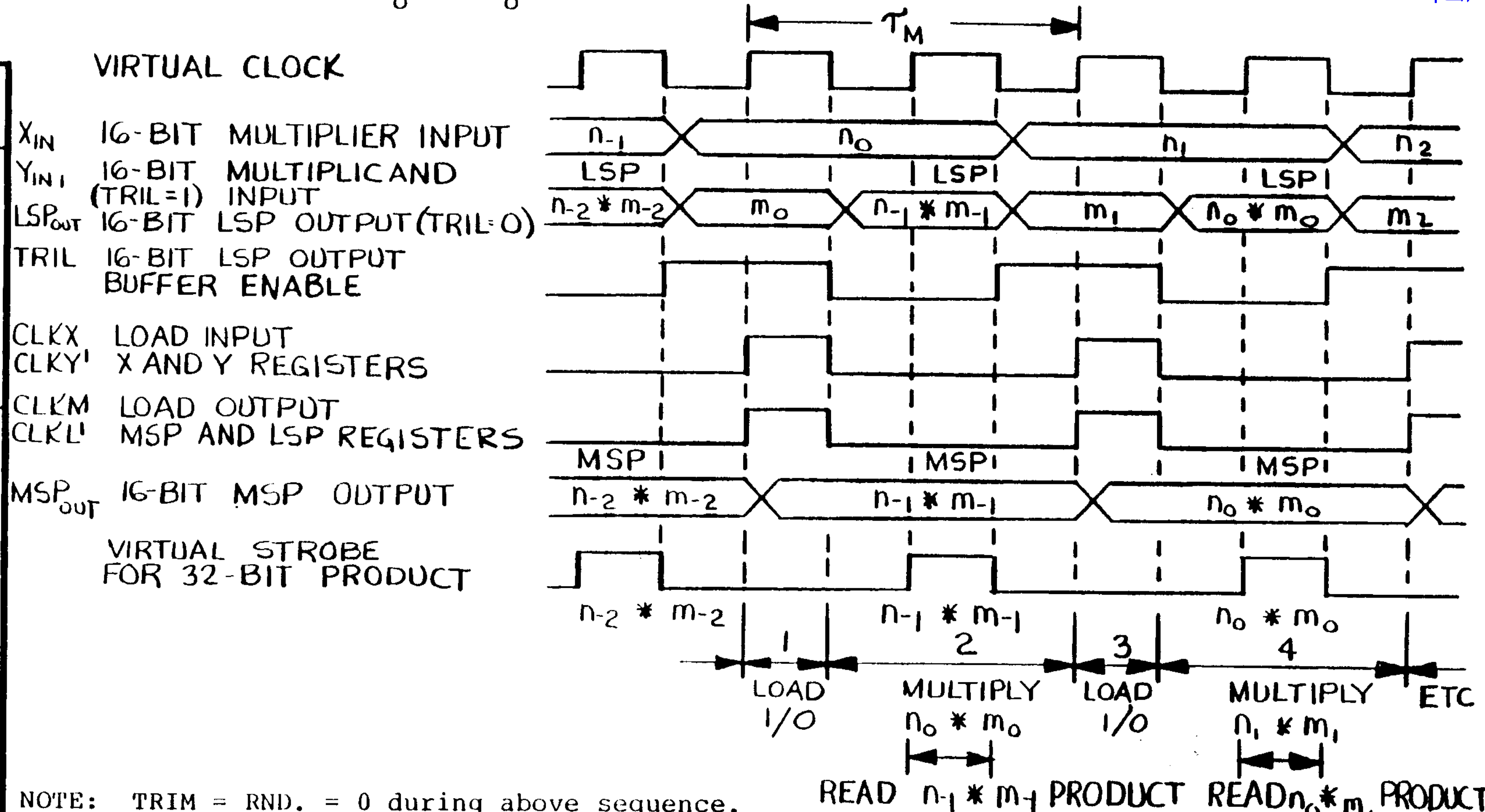
3. TYPICAL OPERATING SEQUENCE (3 PORT)

a. Load 16-bit multiplier (n_o) and 16-bit multiplicand (m_o) into X and Y input registers, respectively. Simultaneously load output registers with the product of two previous operands, n_{-1} and m_{-1}.

b. Wait for completion of $r_o * m_o$ multiplication. Read product of previous operands.

c. Load MSPS and LSP output registers with product of n_o and m_o. Simultaneously load input registers with n_1 and m_1.

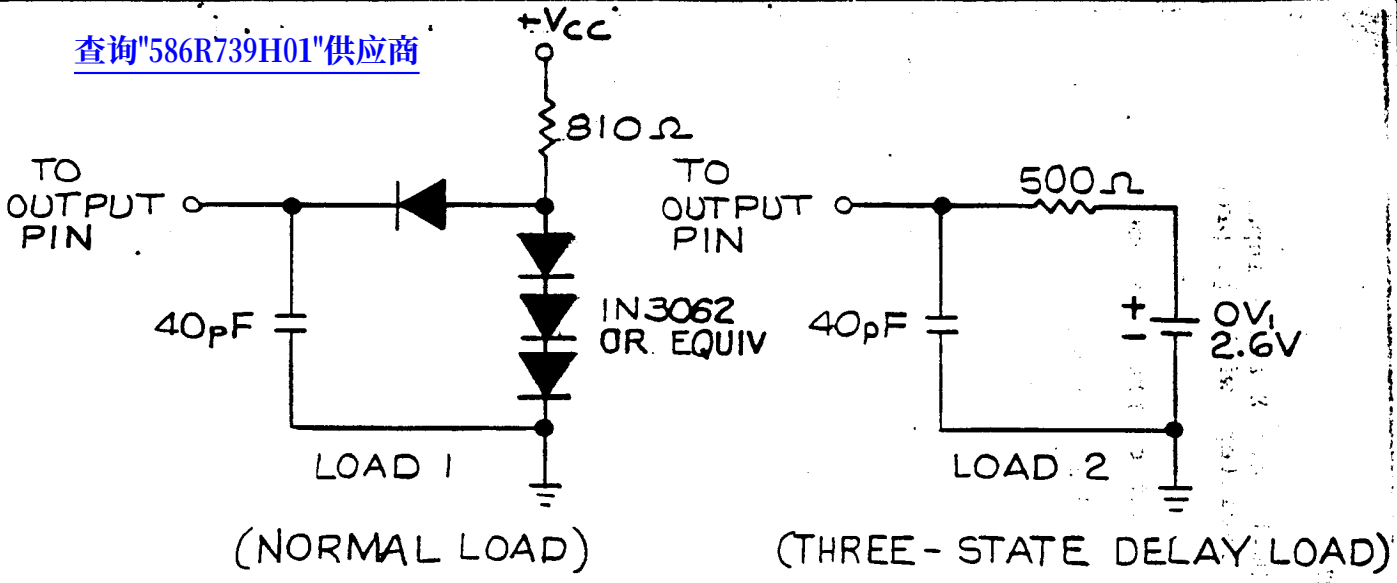
d. Read product of n_o and m_o.



NOTE: TRIM = RND. = 0 during above sequence.

FIGURE 3 - TIMING DIAGRAM AND FUNCTIONAL DESCRIPTION (CONTD)

SIZE	FSCM NO.	DWG NO.
A	97942	586R739
SCALE —	REV D	SHEET 19



TIMING CONDITIONS		
PARAMETER	SYMBOL	CONDITION
Clock Pulse Width	t_{PW}	25 ns
Set-Up Time	t_S	25 ns
Hold-Time	t_H	0

FIGURE 4 - OUTPUT LOAD CIRCUITS AND TIMING CONDITIONS

SIZE	FSCM NO.	DWG NO.
A	97942	586R739
SCALE —	REV D	SHEET 20