



DS4266

General Description

The DS4266 surface-mount ceramic crystal oscillator is part of Maxim's DS4-XO crystal oscillator product family. The DS4266 is a 266MHz crystal oscillator designed to support high-performance DDR memory applications that require a stable, low-jitter, and tight duty-cycle clock source. The device provides an overall accuracy and stability better than $\pm 50\text{ppm}$, including aging. Jitter performance is better than 0.7psRMS typically over a 12kHz to 20MHz bandwidth, and duty-cycle performance is better than 48%/52%.

The DS4266 has an output frequency of 266MHz, and it supports LVDS and LVPECL output types. The DS4266 is constructed using a fundamental crystal in conjunction with high-performance silicon germanium PLL technology, enabling very low phase noise and phase jitter performance. The device operates from a 3.3V $\pm 5\%$ power supply and consumes a maximum current of 100mA.

The DS4266 is packaged in a miniature 5mm x 3.2mm x 1.49mm, 10-lead LCCC ceramic package, making it suitable for applications where board space is critical.

Applications

DDR Memory Clock Source

DDR Clock Oscillator

Features

- ◆ < 0.7psRMS (typ) from 12kHz to 20MHz Jitter
- ◆ LVDS or LVPECL Output Types
- ◆ 3.3V Operating Voltage
- ◆ 5.0mm x 3.2mm x 1.49mm, 10-Pin LCCC Ceramic Package
- ◆ -40°C to +85°C Operating Temperature Range
- ◆ Lead-Free/RoHS Compliant

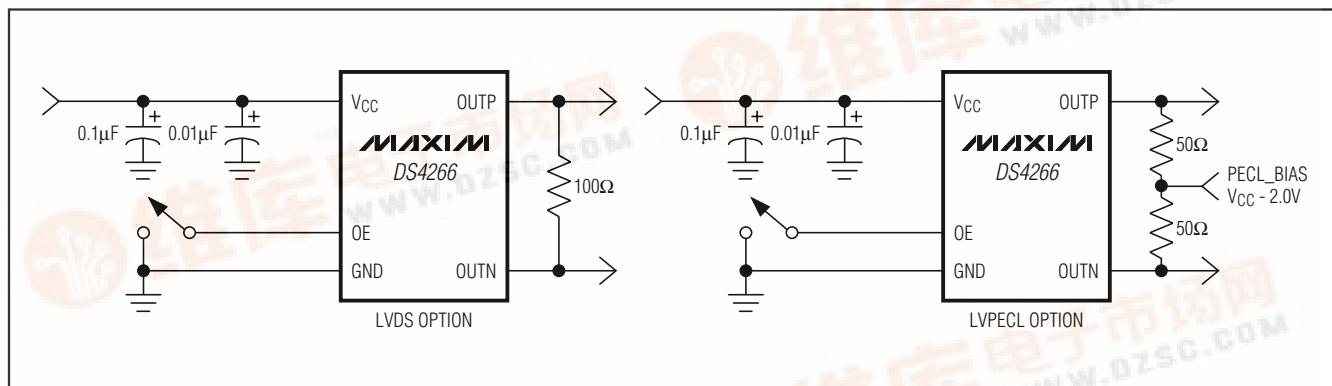
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS4266D+	-40°C to +85°C	10 LCCC
DS4266P+	-40°C to +85°C	10 LCCC

+Denotes a lead(Pb)-free/RoHS-compliant package. The lead finish is JESD97 category e4 (Au over Ni) and is compatible with both lead-based and lead-free soldering processes.

Pin Configuration and Selector Guide appear at end of data sheet.

Typical Operating Circuits



DDR Clock Oscillator

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC}) -0.3V, +4V
 Operating Temperature Range -40°C to +85°C
 Junction Temperature +150°C

Storage Temperature Range -55°C to +85°C
 Soldering Temperature Profile
 (3 passes max of reflow) Refer to the IPC/JEDEC
 J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.135V to 3.465V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V _{CC}	(Note 1)	3.135	3.3	3.465	V
Operating Current	I _{CC_D}	LVDS, output loaded or unloaded	52	75		mA
	I _{CC_PU}	LVPECL, output unloaded	49	70		
	I _{CC_PI}	LVPECL, output load 50Ω at V _{CC} - 2.0V	74	100		
Output Frequency	f _{OUT}			f _{NOM}		MHz
Oscillator Startup Time	t _{STARTUP}	(Note 2)		50		ms
Frequency Stability	Δf _{TOTAL}	Over temperature range, aging, load, supply, and initial tolerance (Note 3)	-50	f _{NOM}	+50	ppm
Frequency Stability Over Temperature with Initial Tolerance	Δf _{TEMP}	V _{CC} = 3.3V	-35		+35	ppm
Initial Tolerance	Δf _{INITIAL}	V _{CC} = 3.3V, T _A = +25°C		±20		ppm
Frequency Change Due to ΔV _{CC}	Δf _{VCC}	V _{CC} = 3.3V ±5%	-3		+3	ppm/V
Frequency Change Due to Load Variation	Δf _{LOAD}	±10% variation in termination resistance		±1		ppm
Aging (15 Years)	Δf _{AGING}		-7		+7	ppm
Jitter	JRMS	Integrated phase RMS; 12kHz to 5MHz, V _{CC} = 3.3V, T _A = +25°C		0.7		ps
		Integrated phase RMS; 12kHz to 20MHz, V _{CC} = 3.3V, T _A = +25°C		0.7		
		Integrated phase RMS; 12kHz to 80MHz, V _{CC} = 3.3V, T _A = +25°C		1.0		
Input-Voltage High (OE)	V _{IH}	(Note 1)	0.7 x V _{CC}			V
Input-Voltage Low (OE)	V _{IL}	(Note 1)	0	0.3 x V _{CC}		V
Input Leakage (OE)	I _{LEAK}	GND ≤ OE ≤ V _{CC}	-50	+5.0		μA

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.135V to 3.465V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVDS						
Output High Voltage	$V_{OHLVDSO}$	100Ω differential load (Note 1)		1.475		V
Output Low Voltage	$V_{OPLLVDSO}$	100Ω differential load (Note 1)	0.925			V
Differential Output Voltage	$ V_{ODLVDSO} $	100Ω differential load	250	425		mV
Output Common-Mode Voltage Variation	$V_{LVDSOCOM}$	100Ω differential load		150		mV
Change in Differential Magnitude or Complementary Inputs	$\Delta V_{ODLVDSO}$	100Ω differential load		25		mV
Offset Output Voltage	$V_{OFFLVDSO}$	100Ω differential load (Note 1)	1.125	1.275		V
Differential Output Impedance	R_{OLVDSO}		80	140		Ω
Output Current	$I_{VSSLVDSO}$	OUTN or OUTP shorted to ground and measure the current in the shorting path		40		mA
	I_{LLVDSO}	OUTN or OUTP shorted together	6.5			
Output Rise Time (Differential)	t_{RLVDSO}	20% to 80%	175			ps
Output Fall Time (Differential)	t_{FLVDSO}	80% to 20%	175			ps
Duty Cycle	D_{CYCLE_LVDS}		48	52		%
Propagation Delay from OE Going Low to Logical 1 at OUTP	t_{PA1}			200		ns
Propagation Delay from OE Going High to Output Active	t_{P1A}			200		ns
LVPECL						
Output High Voltage	V_{OH}	Output connected to 50Ω at PECL_BIAS at V_{CC} - 2.0V	V_{CC} - 1.085	V_{CC} - 0.88		V
Output Low Voltage	V_{OL}	Output connected to 50Ω at PECL_BIAS at V_{CC} - 2.0V	V_{CC} - 1.825	V_{CC} - 1.62		V
Differential Voltage	V_{DIFF_PECL}	Output connected to 50Ω at PECL_BIAS at V_{CC} - 2.0V	0.595	0.710		V
Rise Time	t_{R-PECL}		200			ps
Fall Time	t_{F-PECL}		200			ps
Duty Cycle	D_{CYCLE_PECL}		48	52		%
Propagation Delay from OE Going Low to Output High Impedance	t_{PAZ}			200		ns
Propagation Delay from OE Going High to Output Active	t_{PZA}			200		ns

Note 1: All voltages referenced to ground.

Note 2: AC parameters are guaranteed by design and not production tested.

Note 3: Frequency stability is calculated as: $\Delta f_{TOTAL} = \Delta f_{TEMP} + \Delta f_{VCC} \times (3.3 \times 5\%) + \Delta f_{LOAD} + \Delta f_{AGING}$.

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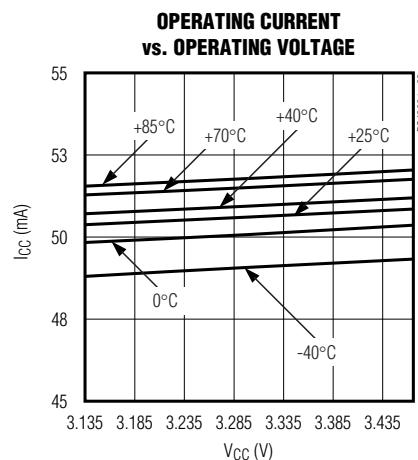
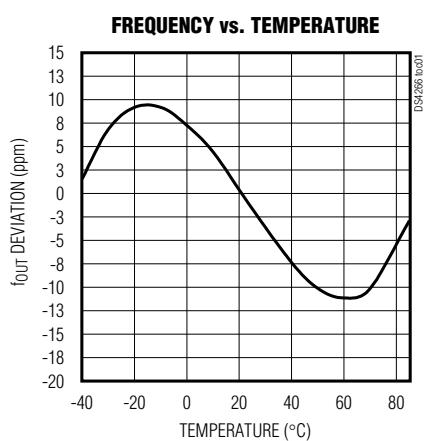
DDR Clock Oscillator

Single-Sideband Phase Noise at $f_O = f_{NOM}$

$f_M =$	SINGLE-SIDEBAND PHASE NOISE AT $f_O = f_{NOM}$ (dBc/Hz)
	266MHz
10Hz	-65
100Hz	-95
1kHz	-113
10kHz	-113
100kHz	-118
1MHz	-137
10MHz	-149
20MHz	-153

Typical Operating Characteristics

($V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1	OE	Active-High Output Enable. Has an internal pullup $100\text{k}\Omega$ resistor.
2, 7-10	N.C.	No Connection. Must be floated.
3	GND	Ground
4	OUTP	Positive Output for LVPECL or LVDS
5	OUTN	Negative Output for LVPECL or LVDS
6	V _{CC}	Supply Voltage
—	EP	Exposed Paddle. Do not connect this pad or place exposed metal under the pad.

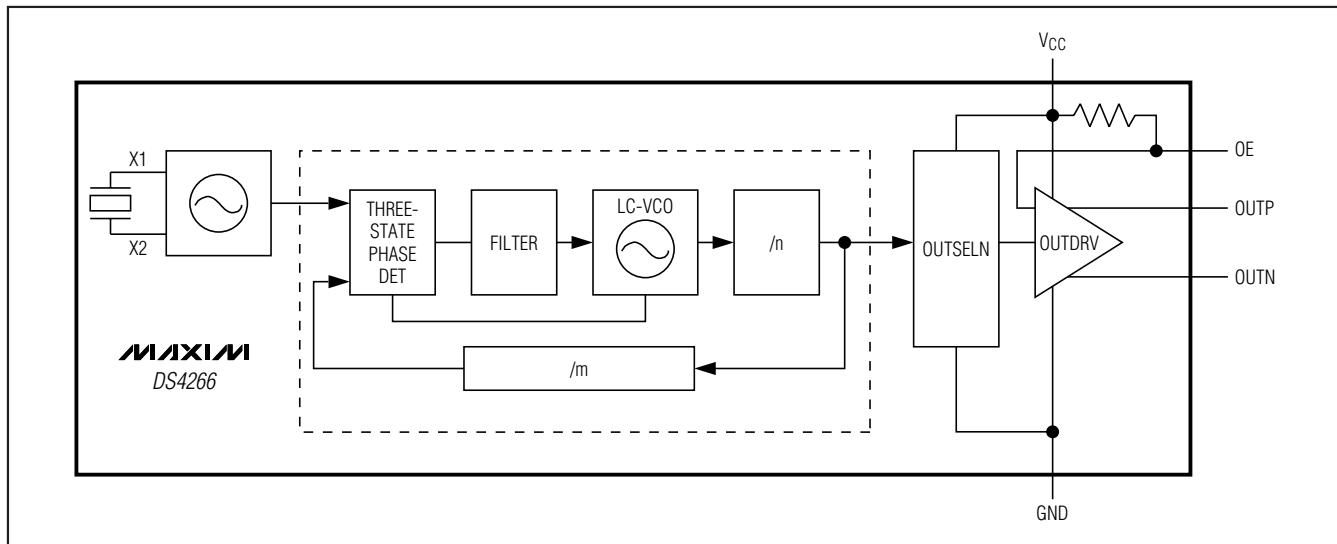


Figure 1. Functional Diagram

Detailed Description

The DS4266 consists of a fundamental-mode crystal and synthesizer IC packaged in a 5mm x 3.2mm x 1.49mm, 10-pin LCCC ceramic package. The device produces a frequency output of 266.00MHz. Two differential output types are available: LVDS and LVPECL. The device output can be enabled or disabled through the OE signal input. When the OE signal is low, LVPECL

outputs go to the PECL_BAS level of Vcc - 2.9V, while the LVDS outputs are a logical 1. See Figures 2 and 3 for LVDS and LVPECL output timing diagrams.

Additional Information

For more available frequencies in the DS4-XO family, refer to the DS4125 data sheet at www.maxim-ic.com/DS4125.

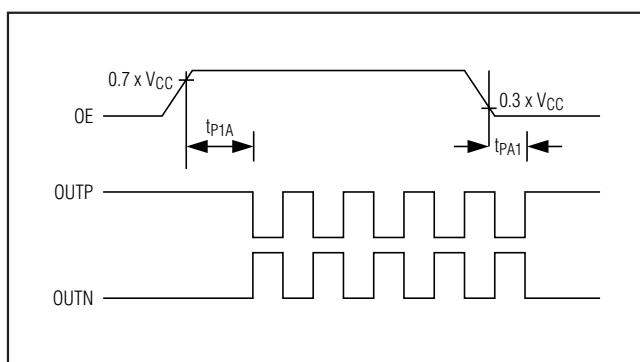


Figure 2. LVDS Output Timing Diagram When OE Is Enabled and Disabled

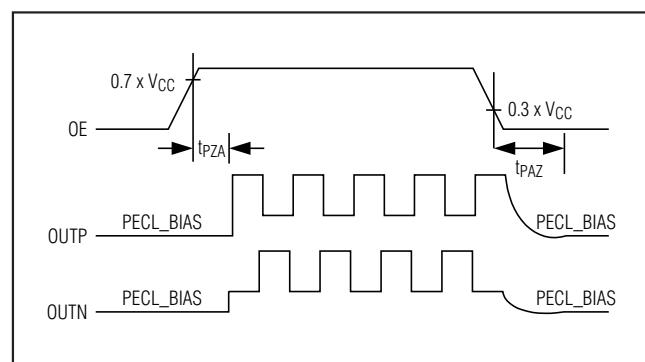


Figure 3. LVPECL Output Timing Diagram When OE Is Enabled and Disabled

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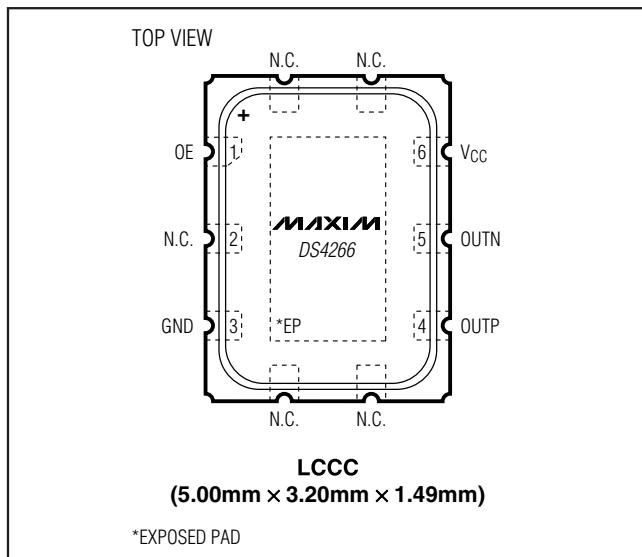
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Selector Guide

PART	FREQUENCY (NOM) (MHz)	FREQUENCY STABILITY (ppm)	OUTPUT TYPE	TOP MARK
DS4266D+	266	± 50	LVDS	66D
DS4266P+	266	± 50	LVPECL	66P

+Denotes a lead(Pb)-free/RoHS-compliant package. The lead finish is JESD97 category e4 (Au over Ni) and is compatible with both lead-based and lead-free soldering processes.

Pin Configuration



Chip Information

SUBSTRATE CONNECTED TO GROUND

PROCESS: BiPolar SiGe

Thermal Information

THETA-JA (°C/W)
90

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
10 LCCC	L1053+H2	21-0389

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