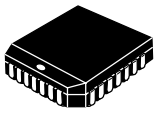
MC10H602, MC100H602

9-Bit Latch TTL to ECL Translator

ON Semiconductor®

http://onsemi.com



PLCC−28
FN SUFFIX
CASE 776

Description

The MC10H/100H602 is a 9−bit, dual supply TTL to ECL translator with latch. Devices in the ON Semiconductor 9−bit translator series utilize the PLCC−28 for optimal power pinning, signal flow−through and electrical performance.

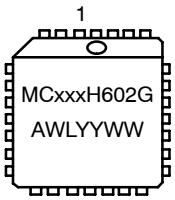
The H602 features D−type latches. Latching is controlled by Latch Enable (LEN), while the Master Reset input resets the latches. A post−latch logic enable is also provided (ENECL), allowing control of the output state without destroying latch data. All control inputs are ECL level.

The 10H version is compatible with MECL 10H™ ECL logic levels. The 100H version is compatible with 100K levels.

Features

- 9−Bit Ideal for Byte−Parity Applications
- Flow−Through Configuration
- Extra TTL and ECL Power/Ground Pins to Minimize Switching Noise
- Dual Supply
- 3.5 ns Max D to Q
- PNP TTL Inputs for Low Loading
- Pb−Free Packages are Available*

MARKING DIAGRAM*



xxx	= 10 or 100
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

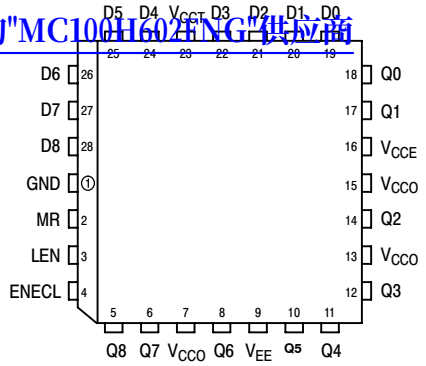


Figure 1. PLCC−28 Pinout (Top View)

Table 1. PIN NAMES

PIN	FUNCTION
GND	TTL Ground (0 V)
V_{CCE}	ECL V_{CC} (0 V)
V_{CCO}	ECL V_{CC} (0 V) — Outputs
V_{CCT}	TTL Supply (+5.0 V)
V_{EE}	ECL Supply (−5.2/−4.5 V)
D0 − D8	Data Inputs (TTL)
Q0 − Q8	Data Outputs (ECL)
ENECL	Enable Control (ECL)
LEN	Latch Enable (ECL)
MR	Master Reset (ECL)

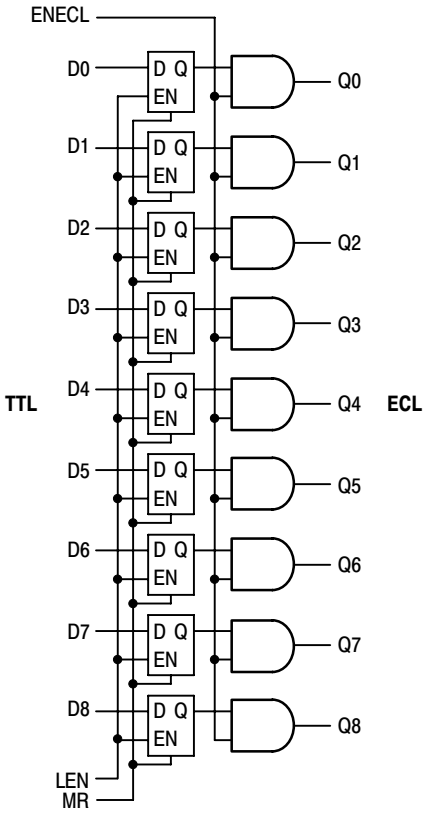


Figure 2. LOGIC SYMBOL

Table 2. TRUTH TABLE

D	LEN	MR	ENECL	Q
L	L	L	H	L
H	L	L	H	H
X	H	L	H	Q_0
X	X	H	H	L
X	X	X	L	L

Table 3. DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5% (10H version); V_{EE} = −4.2 V to −5.5 V (100H version)

Symbol	Parameter		0°C		25°C		75°C		Unit
			Min	Max	Min	Max	Min	Max	
	Power Supply Current								
I_{EE}	ECL	10H 100H		−125 −122		−125 −123		−125 −132	mA
I_{CCH} I_{CCL}	TTL			48 50		48 50		48 50	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 4. 10H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5%

Symbol	Parameter	Condition	0°C		25°C		75°C		Unit
			Min	Max	Min	Max	Min	Max	
I_{INH} I_{INL}	Input HIGH Current Input LOW Current		 0.5	255	 0.5	175	 0.5	175	μA μA
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage		−1170 −1950	−840 −1480	−1130 −1950	−810 −1480	−1070 −1950	−735 −1450	mV
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	50 Ω to −2.0 V	−1020 −1950	−840 −1630	−980 −1950	−810 −1630	−920 −1950	−735 −1600	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 5. 100H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −4.2 V to −5.5 V

Symbol	Parameter	Condition	0°C		25°C		75°C		Unit
			Min	Max	Min	Max	Min	Max	
I_{INH} I_{INL}	Input HIGH Current Input LOW Current		 0.5	255	 0.5	175	 0.5	175	μA μA
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage		−1165 −1810	−880 −1475	−1165 −1810	−880 −1475	−1165 −1810	−880 −1475	mV
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	50 Ω to −2.0 V	−1025 −1810	−880 −1620	−1025 −1810	−880 −1620	−1025 −1810	−880 −1620	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 6. TTL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5% (10H version); V_{EE} = −4.2 V to −5.5 V (100H version)

Symbol	Parameter	Condition	0°C		25°C		75°C		Unit
			Min	Max	Min	Max	Min	Max	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage		2.0	 0.8	2.0	 0.8	2.0	 0.8	V V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V V_{IN} = 7.0 V		20 100		20 100		20 100	μA
I_{IL}	Input LOW Current	V_{IN} = 0.5 V		−0.6		−0.6		−0.6	mA
V_{IK}	Input Clamp Voltage	I_{IN} = −18 mA		−1.2		−1.2		−1.2	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 7. AC CHARACTERISTICS (V_{CC} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5% (10H version); V_{EE} = −4.2 V to −5.5 V (100H version)

Symbol	Parameter		0°C		25°C		75°C		Unit
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay to Output	D LEN MR ENECL	1.4 2.0 2.0 1.6	3.0 3.4 3.4 3.2	1.5 2.1 2.1 1.7	3.2 3.5 3.5 3.3	1.7 2.4 2.5 1.8	3.5 3.7 3.9 3.7	ns
t_s	Set−Up Time, D to LEN		2.0		2.0		2.0		ns
t_h	Hold Time, D to LEN		1.0		1.0		1.0		ns
t_w(L)	LEN Pulse Width, LOW		2.0		2.0		2.0		ns
t_R t_F	Output Rise/Fall Time 20% − 80%		0.5	1.5	0.5	1.5	0.5	1.5	ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

ORDERING INFORMATION

Device	Package	Shipping†
MC10H602FN	PLCC−28	37 Units / Rail
MC10H602FNG	PLCC−28 (Pb−Free)	37 Units / Rail
MC10H602FNR2	PLCC−28	500 / Tape & Reel
MC10H602FNR2G	PLCC−28 (Pb−Free)	500 / Tape & Reel
MC100H602FN	PLCC−28	37 Units / Rail
MC100H602FNG	PLCC−28 (Pb−Free)	37 Units / Rail
MC100H602FNR2	PLCC−28	500 / Tape & Reel
MC100H602FNR2G	PLCC−28 (Pb−Free)	500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

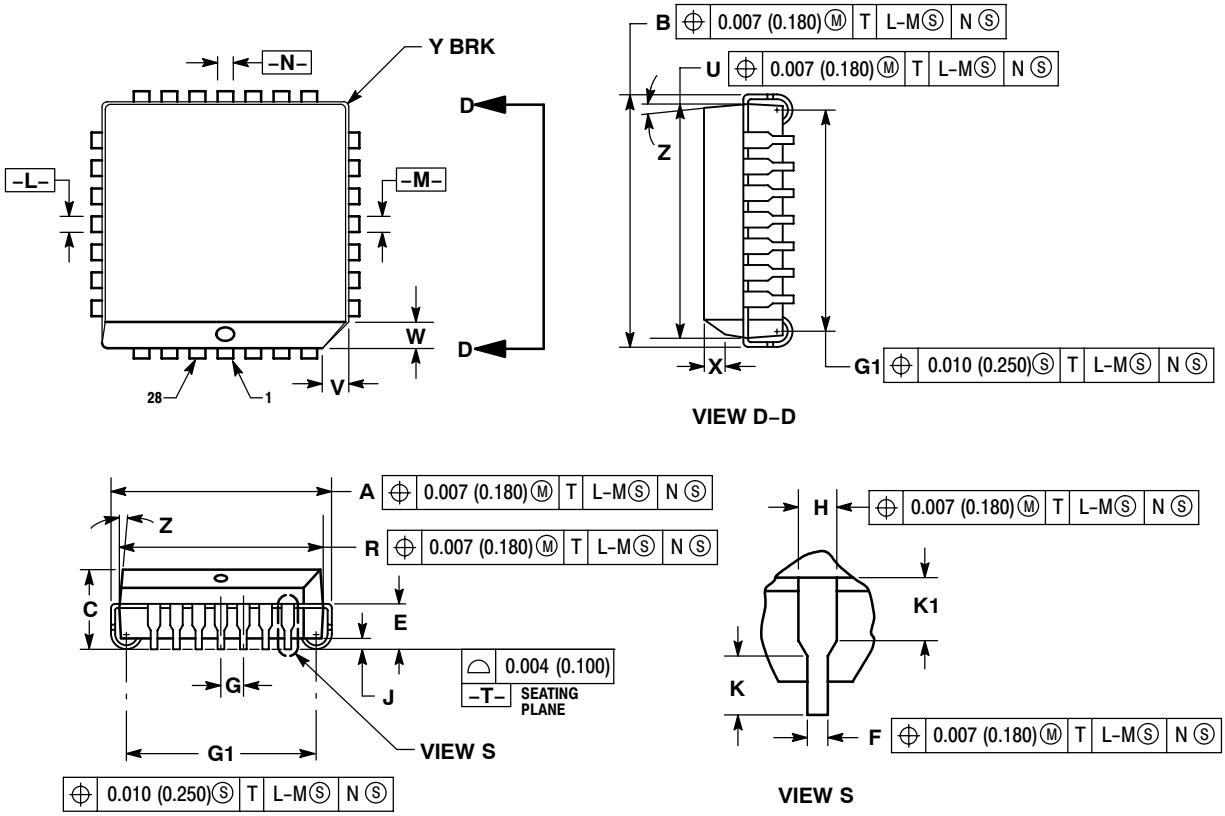
AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

PLCC−28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776−02
ISSUE E



NOTES:
1. DATUMS −L−, −M−, AND −N− DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM −T−, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

ECLinPS is a trademark of Semiconductor Components Industries, LLC (SCILLC).
MECL 10H is a trademark of Motorola, Inc.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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