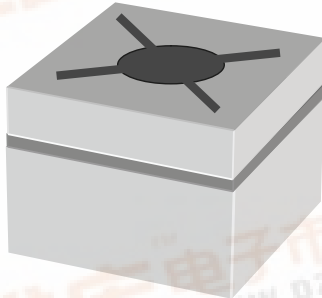


## Specification of GaAlAs IR Emitting Diode Chip



21594

## FEATURES

- Package type: chip
- Package form: single chip
- Technology: double hetero
- Dimensions chip (L x W x H in mm): 0.37 x 0.37 x 0.17
- Peak wavelength:  $\lambda = 850$  nm
- Compliant to RoHS directive 2002/95/EC and in accordance to WEEE 2002/96/EC

RoHS  
COMPLIANT

## DESCRIPTION

T8514VB is an infrared, 850 nm emitting diode in GaAlAs double hetero technology with high radiant power and high speed. Anode is the bond pad on top.

## GENERAL INFORMATION

The datasheet is based on Vishay optoelectronics sample testing under certain predetermined and assumed conditions, and is provided for illustration purpose only. Customers are encouraged to perform testing in actual proposed packaged and used conditions. Vishay optoelectronics die products are tested using Vishay optoelectronics based quality assurance procedures and are manufactured using Vishay optoelectronics established processes. Estimates such as those described and set forth in this datasheet for semiconductor die will vary depending on a number of packaging, handling, use, and other factors. Therefore sold die may not perform on an equivalent basis to standard package products.

## PRODUCT SUMMARY

COMPONENT	$I_e$ (mW/sr)	$\varphi$ (deg)	$\lambda_p$ (nm)	$t_r$ (ns)
T8514VB	3.3	-	850	25

## Note

Test condition see table "Basic Characteristics"

## ORDERING INFORMATION

ORDERING CODE	PACKAGING	REMARKS	PACKAGE FORM
T8514VB-SF-F	Wafer sawn on foil	MOQ: 25 000 pcs	Chip

## Note

MOQ: minimum order quantity

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Forward current		$I_F$	100	mA
Reverse voltage		$V_R$	5	V
Surge forward current	$t_p = 100 \mu s$	$I_{FSM}$	1	A
Junction temperature		$T_j$	125	°C
Operating temperature range		$T_{amb}$	- 40 to + 100	°C
Storage temperature range chip		$T_{stg1}$	- 40 to + 100	°C
Storage temperature range on foil		$T_{stg2}$	- 40 to + 50	°C

## Note

$T_{amb} = 25$  °C, unless otherwise specified

BASIC CHARACTERISTICS <sup>(1)</sup>						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Forward voltage	$I_F = 100 \text{ mA}$	$V_F$		1.44		V
Radiant power <sup>(2)</sup>	$I_F = 100 \text{ mA}$	$\phi_e$		23		mW
Radiant intensity <sup>(3)</sup>	$I_F = 100 \text{ mA}$	$I_e$		3.3		mW/sr
Radiant power (epoxy encapsulated)	$I_F = 100 \text{ mA}$	$\phi_e$		52		mW
Radiant power chip <sup>(4)</sup>	$I_F = 50 \text{ mA}$	$\phi_e$	4.5	5.9		mW
Temperature coefficient of radiant power	$I_F = 100 \text{ mA}$	$TK_{\phi_e}$		- 0.35		%/K
Reverse voltage	$I_R = 10 \text{ }\mu\text{A}$	$V_R$	5	18		V
Temperature coefficient of forward voltage	$I_F = 1 \text{ mA}$	$TK_{V_F}$		- 1.8		mV/K
Angle of half intensity	$I_F = 100 \text{ mA}$	$\varphi$		$> \pm 80$		deg
Peak wavelength	$I_F = 30 \text{ mA}$	$\lambda_p$		850		nm
Spectral bandwidth	$I_F = 30 \text{ mA}$	$\lambda_{0.5}$		34		nm
Rise time/fall time	$I_F = 100 \text{ mA}$	$t_r, t_f$		25	50	ns

**Notes**

- (1)  $T_{amb} = 25 \text{ }^\circ\text{C}$ , unless otherwise specified  
 (2) The measurements are based on samples of die which are mounted on a TO-18 gold header without resin coating  
 (3) The radiant intensity,  $I_e$ , is measured on the geometric axis of the TO-18 header  
 (4) The radiant power,  $\phi_e$ , is measured with chip on bare plate and aperture angle about  $30^\circ$ , as indicated on the label of each wafer

**BASIC CHARACTERISTICS**

$T_{amb} = 25 \text{ }^\circ\text{C}$ , unless otherwise specified

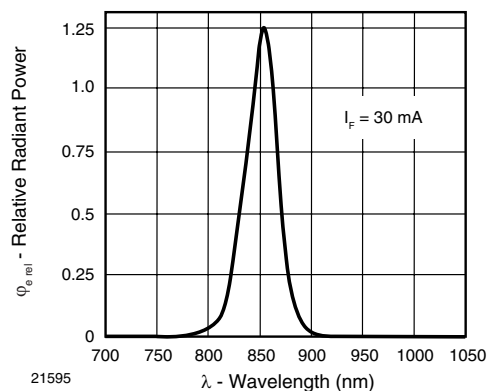


Fig. 1 - Relative Spectral Emission  
 $\phi_{e \text{ rel}} = f(\lambda)$

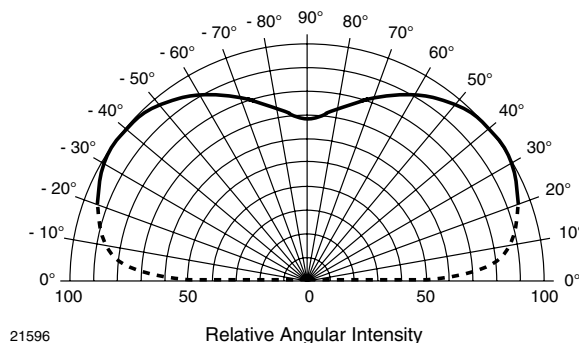
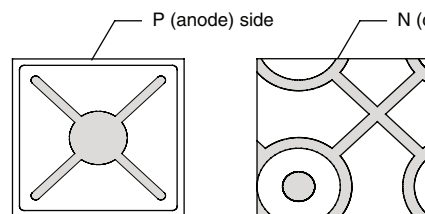


Fig. 2 - Radiant Characteristics  
 $I_{rel} = f(\varphi)$

**DIMENSIONS**

Electrode pattern:



21597

Sectional view (schematic):

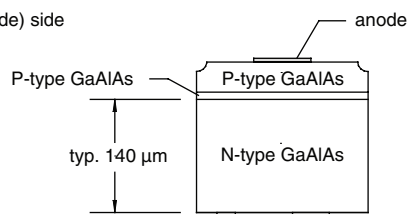


Fig. 3

MECHANICAL DIMENSIONS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Length of chip edge (x-direction)	$L_x$		0.37		mm
Length of chip edge (y-direction)	$L_y$		0.37		mm
Emission area	$A_E$	0.325 x 0.325			mm <sup>2</sup>
Die height	H		0.17		mm
Diameter of bondpad	d		0.14		mm

ADDITIONAL INFORMATION (1)	
Frontside metallization, anode	Aluminum
Backside metallization, cathode	Gold alloy
Dicing	Sawing
Die bonding technology	Epoxy bonding

**Note**

- (1) All chips are checked in accordance with the Vishay Semiconductor, specification of visual inspection FVOV6870.  
The visual inspection shall be made in accordance with the "specification of visual inspection as referenced". The visual inspection of chip backside is performed with stereo microscope with incident light and 40x to 80x magnification.  
The quality inspection (final visual inspection) is performed by production. An additional visual inspection step as special release procedure by QM is not installed.

**HANDLING AND STORAGE CONDITIONS**

- The hermetically sealed shipment lots shall be opened in temperature and moisture controlled cleanroom environment only. It is mandatory to follow the rules for disposition of material that can be hazardous for humans and environment.
- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Singulated die are not to be handled with tweezers. A vacuum wand with non metallic ESD protected tip should be used.

**PACKING**

Chips are fixed on adhesive foil. Upon request the foils can be mounted on plastic frame or disco frame. For shipment, the wafers are arranged to stacks and hermetically sealed in plastic bags to ensure protection against environmental influence (humidity and contamination).

Use for recycling reliable operators only. We can help getting in touch with your nearest sales office. By agreement we will take back packing material, if it is sorted. You will have to bear the costs of transport. We will invoice you for any costs incurred for packing material that is returned unsorted or which we are not obliged to accept.

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