REVISIONS			
	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
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SHEET	15	16	17	18	19	20	21	22	23	24	25								
REV STATUS OF SHEETS				REV															
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
97-10-07

REVISION LEVEL

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, DIGITAL, MEMORY, RADIATION HARDENED, CMOS, 4 X 32 K X 40 SRAM, MULTICHIP MODULE (MCM)

SIZE	CAGE CODE	
A	67268	**5962-96840**

SHEET 1 OF 25

DSCC FORM 2233
APR 97

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

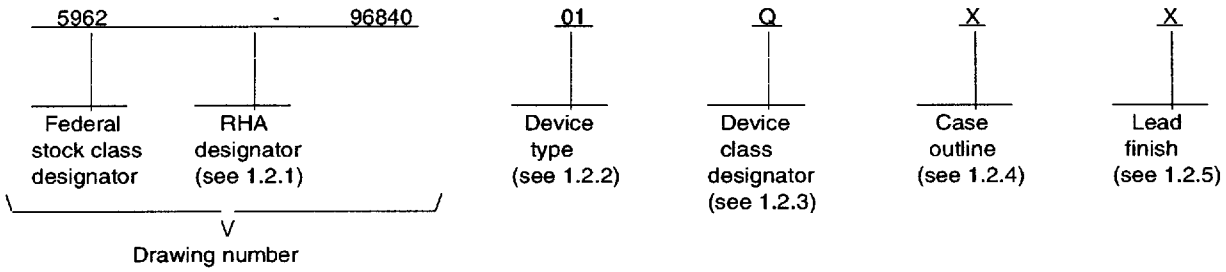
5962-E073-97

9004708 0031078 808

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HX84050	4 X 32 k X 40 CMOS, SOI, SRAM, Multichip Module (MCM)

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	200	Quad flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/

Storage temperature range	-65° C to +125° C
Supply voltage range (V_{DD})	-0.5 V dc to 6.5 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{DD} + 0.3 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{DD} + 0.3 V dc
Output voltage applied to high-Z state	-0.3 V dc to V_{DD} + 0.3 V dc
Maximum power dissipation (P_D)	5.6 W 3/
Lead temperature (soldering, 10 seconds)	+288° C
Chip thermal resistance, junction-to-case (θ_{JC})	4.0° C/W 4/
Maximum junction temperature (T_J)	+175° C

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	4.5 V dc to 5.5 V dc
Supply voltage (V_{SS})	0.0 V dc
High level input voltage range, CMOS levels (V_{IH})	0.7 V_{DD} to V_{DD} + 0.3 V dc
Low level input voltage range, CMOS levels (V_{IL})	-0.3 V dc to 0.3 V_{DD}
Module thermal resistance, junction-to-case (θ_{JC})	1.0° C/W (module power) 4/
Case operating temperature range (T_C)	-55° C to +125° C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise specified, all voltages are referenced to V_{SS} (V_{SS} = ground).
3/ Maximum power dissipation with 20 chips utilized at 50 percent (each subsystem is maximum utilized, alternating between banks) and outputs loaded as in figure 5.
4/ Assumes a uniform temperature on the bottom surface of the package, and a uniform power distribution over the top surface of the die, and all die at equal power level.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, bulletin, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issue of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation (see 6.2).

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standard Test Procedure for the Characterization of LATCH-UP in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.5 Timing waveforms and output load circuit. The timing waveform and output load circuit shall be as specified on figure 5.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 6.

3.2.6 Functional test. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{DD} = 4.5 V, I_{OH} = -3.5 mA, V_{IH} = 3.15 V, V_{IL} = 1.35 V	1, 2, 3	All	4.2		V
Low level output voltage	V_{OL}	V_{DD} = 4.5 V, I_{OL} = 7.0 mA, V_{IH} = 3.15 V, V_{IL} = 1.35 V	1, 2, 3	All		0.4	V
High level input leakage current	I_{IH}	V_{DD} = 5.5 V, V_{IN} = V_{DD}, all other pins = V_{SS}	1, 2, 3	All	-50	50	µA
Low level input leakage current	I_{IL}	V_{DD} = 5.5 V, V_{IN} = V_{SS}, all other pins = V_{DD}	1, 2, 3	All	-50	50	µA
High level output leakage current	I_{OZH}	V_{DD} = 5.5 V, V_{IN} = V_{DD}, all other pins = V_{SS}	1, 2, 3	All	-50	50	µA
Low level output leakage current	I_{OZL}	V_{DD} = 5.5 V, V_{IN} = V_{DD}, all other pins = V_{DD}	1, 2, 3	All	-50	50	µA
Data retention voltage	V_{DR}	V_{DD} = 2.5 V	1, 2, 3	All	2.5		V
Operating supply current	I_{CC1}	$\overline{CS}$ = V_{SS}, CE = V_{DD}, V_{DD} = 5.5 V, f = 20 MHz 2/	1, 2, 3	All		525	mA
Supply current, deselected	I_{CC2}	$\overline{CS}$ = CE = V_{DD}, V_{DD} = 5.5 V, f = 20 MHz 2/	1, 2, 3	All		30	mA
Supply current, standby	I_{CC3}	$\overline{CS}$ = CE = V_{DD}, V_{DD} = 5.5 V, f = 0.0 MHz 2/	1, 2, 3	All		30	mA
Supply current, disabled	I_{CC4}	$\overline{CS}$ = CE = V_{SS}, V_{DD} = 5.5 V, f = 20 MHz 2/	1, 2, 3	All		30	mA
Supply current, disabled, idle	I_{CC5}	$\overline{CS}$ = CE = V_{SS}, V_{DD} = 5.5 V, f = 0.0 MHz 2/	1, 2, 3	All		30	mA
Data retention current	I_{CC6}	V_{DD} = 2.5 V, V_{IN} = 2.5 V	1, 2, 3	All		10	mA
Input capacitance, $\overline{CS}$ and CE inputs 3/	C_{IN1}	V_{IN} = V_{DD} or V_{SS}, f = 1.0 MHz, T_A = +25°C	4	All		50	pF
Input capacitance, address, $\overline{OE}$, and $\overline{WE}$ inputs 3/	CIN2	V_{IN} = V_{DD} or V_{SS}, f = 1.0 MHz, T_A = +25°C	4	All		70	pF
Output capacitance 3/	C_{OUT}	V_{OUT} = V_{DD} or V_{SS}, f = 1.0 MHz, T_A = +25°C	4	All		26	pF
Functional tests		See 4.4.1c	7, 8	All			
READ CYCLE							
Read cycle time	t_{AVAV}	See figures 5 and 6 4/	9, 10, 11	All	30		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
READ CYCLE - Continued.							
Address access time	t_{AVQV}	See figures 5 and 6 4/	9, 10, 11	All		26	ns
Chip enable/select access time	t_{EHQV}, t_{SLQV}		9, 10, 11	All		30	ns
Output hold after address change	t_{AXQX}		9, 10, 11	All	3.0		ns
Output enable access time	t_{GLQV}		9, 10, 11	All		13	ns
Chip select/enable to output active 5/	t_{SLQX}, t_{EHQX}		9, 10, 11	All	5.0		ns
Output enable to output active 5/	t_{GLQX}		9, 10, 11	All	0		ns
Chip select to output disable 5/	t_{SHQZ}		9, 10, 11	All		16	ns
Chip enable to output disable	t_{ELQZ}		9, 10, 11	All		16	ns
Output enable to output disable 6/	t_{GHQZ}		9, 10, 11	All		16	ns
WRITE CYCLE							
Write enable to output disable 6/	t_{WLQZ}	See figures 5 and 6 4/	9, 10, 11	All	0	16	ns
Data setup to end of write	t_{DVWH}		9, 10, 11	All	20		ns
Data hold after end of write	t_{WHDX}		9, 10, 11	All	1.0		ns
Output active after end of write	t_{WHQX}		9, 10, 11	All	5.0		ns
Write cycle time	t_{AVAV}		9, 10, 11	All	30		ns
Chip enable to end of write	t_{EHWH}		9, 10, 11	All	25		ns
Chip select to end of write	t_{SLWH}		9, 10, 11	All	25		ns
Address setup to end of write	t_{AVWH}		9, 10, 11	All	25		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

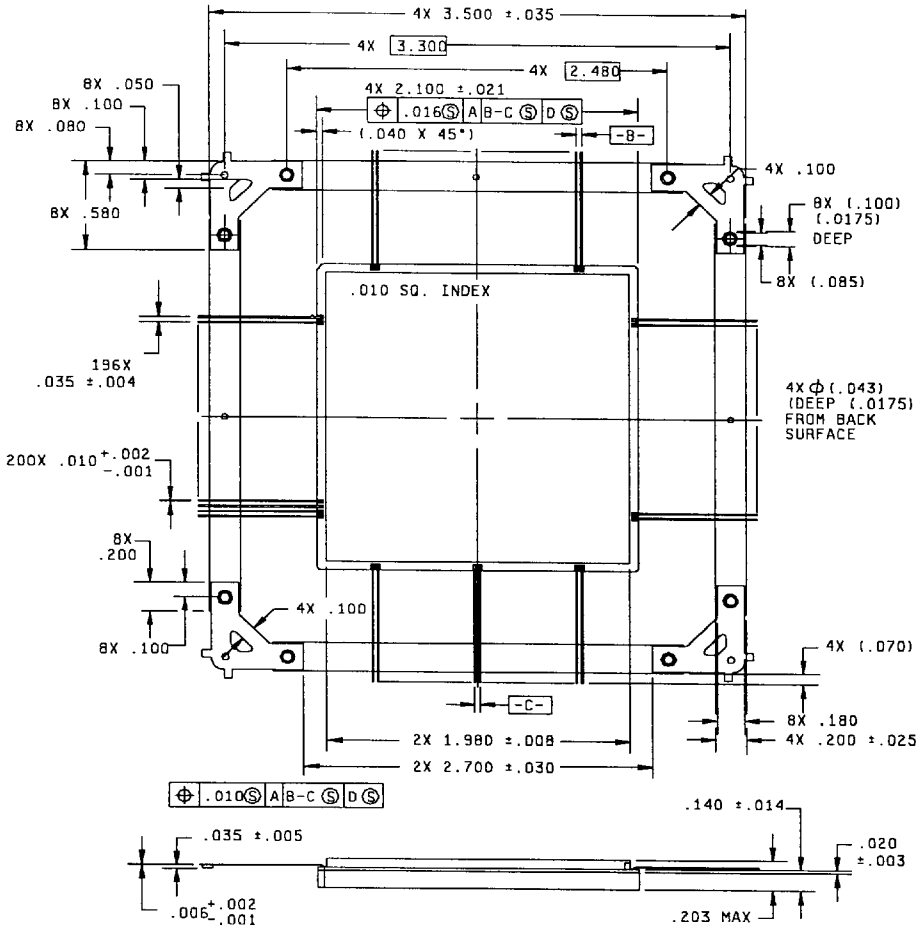
Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
WRITE CYCLE - Continued.							
Address setup to start of write	t_{AVWL}		9, 10, 11	All	5.0		ns
Write pulse width	t_{WLWH}		9, 10, 11	All	20		ns
Address hold after end of write	t_{WHAX}	See figures 5 and 6 4/	9, 10, 11	All	0		ns
Write disable pulse width 3/	t_{WHWL}		9, 10, 11	All	6.0		ns

1/ Devices supplied to this drawing have been characterized through all levels M, D, L, R, F, G, and H of irradiation. However, this device is only tested at the `H` level. Unless otherwise specifed in table IA ,pre and postirradiation values are identical. When performing postirradiation electrical measurements for any RHA level, $T_A = +25°C \pm 5.0°C$. Unless otherwise specified, all parameters are tested to worst case conditions .
2/ Conditions apply as follows: One bank of memory (five 32 k X 8 die) with $\overline{CS}$, CE, and f as specified, all other die banks have $\overline{CS} = V_{DD}$, $CE = V_{SS}$, and f as specified.
3/ Tested initially and after any design or process changes which may affect that parameter, and therefore shall be guaranteed to the limits specified in table IA.
4/ All ac measurements assume transition times $\le$ 5.0 ns. All ac measurements apply to both Memory Subsystem A and Memory Subsystem B, reference figure 4.
5/ Transition is measured ±500 mV from steady state voltage.
6/ Transition is measured ±400 mV from steady state voltage.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device type	T_A = temperature ±10°C 4/	Memory pattern	V_{DD} = 4.5 V		Bias for latch-up test V_{DD} = 5.5 V no latch-up LET = 4/
			Effective LET no upsets [MEV/(mg/cm²)]	Maximum device cross section (μm^2) (LET = 190)	
All	+125°C	5/	≥75	≤.056	≥120

1/ For SEP test conditions, see 4.5.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Data is for a single 32 k X 8 device.
4/ Worst case temperature $T_A = +125°C$.
5/ Testing shall be performed using checkerboard and checkerboard bar test patterns.



NOTE: Dimensions are in inches.

FIGURE 1. Case outline X.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216	SIZE A		5962-96840
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Case outline	X		Case outline	X	
Terminal number	Signal name	Signal type	Terminal number	Signal name	Signal type
1	VSS	PWR/GND	51	VSS	PWR/GND
2	I_ADRS(04)	INPUT	52	VDD	PWR/GND
3	I_ADRS(03)	INPUT	53	D_ADRS(05)	INPUT
4	I_ADRS(02)	INPUT	54	D_ADRS(06)	INPUT
5	I_ADRS(01)	INPUT	55	D_ADRS(07)	INPUT
6	VDD	PWR/GND	56	VDD	PWR/GND
7	VSS	PWR/GND	57	VSS	PWR/GND
8	I_ADRS(00)	INPUT	58	D_ADRS(08)	INPUT
9	I_DATA(09)	3-STATE	59	D_DATA(10)	3-STATE
10	I_DATA(08)	3-STATE	60	D_DATA(11)	3-STATE
11	I_DATA(07)	3-STATE	61	D_DATA(12)	3-STATE
12	VDD	PWR/GND	62	VDD	PWR/GND
13	VSS	PWR/GND	63	VSS	PWR/GND
14	I_DATA(06)	3-STATE	64	D_DATA(13)	3-STATE
15	I_DATA(05)	3-STATE	65	D_DATA(14)	3-STATE
16	I_DATA(04)	3-STATE	66	D_DATA(15)	3-STATE
17	I_DATA(03)	3-STATE	67	D_DATA(16)	3-STATE
18	VDD	PWR/GND	68	VDD	PWR/GND
19	VSS	PWR/GND	69	VSS	PWR/GND
20	I_DATA(02)	3-STATE	70	D_DATA(17)	3-STATE
21	I_DATA(01)	3-STATE	71	D_DATA(18)	3-STATE
22	I_DATA(00)	3-STATE	72	D_DATA(19)	3-STATE
23	I_$\overline{CS1}$	INPUT	73	D_$\overline{WE}$	INPUT
24	VDD	PWR/GND	74	VDD	PWR/GND
25	VSS	PWR/GND	75	VSS	PWR/GND
26	VSS	PWR/GND	76	VSS	PWR/GND
27	VDD	PWR/GND	77	VDD	PWR/GND
28	D_$\overline{CS1}$	INPUT	78	D_$\overline{OE}$	INPUT
29	D_DATA(00)	3-STATE	79	D_DATA(20)	3-STATE
30	D_DATA(01)	3-STATE	80	D_DATA(21)	3-STATE
31	D_DATA(02)	3-STATE	81	D_DATA(22)	3-STATE
32	VSS	PWR/GND	82	VSS	PWR/GND
33	VDD	PWR/GND	83	VDD	PWR/GND
34	D_DATA(03)	3-STATE	84	D_DATA(23)	3-STATE
35	D_DATA(04)	3-STATE	85	D_DATA(24)	3-STATE
36	D_DATA(05)	3-STATE	86	D_DATA(25)	3-STATE
37	D_DATA(06)	3-STATE	87	D_DATA(26)	3-STATE
38	VSS	PWR/GND	88	VSS	PWR/GND
39	VDD	PWR/GND	89	VDD	PWR/GND
40	D_DATA(07)	3-STATE	90	D_DATA(27)	3-STATE
41	D_DATA(08)	3-STATE	91	D_DATA(28)	3-STATE
42	D_DATA(09)	3-STATE	92	D_DATA(29)	3-STATE
43	D_ADRS(00)	INPUT	93	D_ADRS(09)	INPUT
44	VSS	PWR/GND	94	VSS	PWR/GND
45	VDD	PWR/GND	95	VDD	PWR/GND
46	D_ADRS(01)	INPUT	96	D_ADRS(10)	INPUT
47	D_ADRS(02)	INPUT	97	D_ADRS(11)	INPUT
48	D_ADRS(03)	INPUT	98	D_ADRS(12)	INPUT
49	D_ADRS(04)	INPUT	99	VDD	PWR/GND
50	VSS	PWR/GND	100	VSS	PWR/GND

FIGURE 2. Terminal connections.

Case outline	X		Case outline	X	
Terminal number	Signal name	Signal type	Terminal number	Signal name	Signal type
101	VSS	PWR/GND	151	VSS	PWR/GND
102	VDD	PWR/GND	152	VDD	PWR/GND
103	D_CE0	INPUT	153	I_ADRS(12)	INPUT
104	D_CE1	INPUT	154	I_ADRS(11)	INPUT
105	D_ADRS(13)	INPUT	155	I_ADRS(10)	INPUT
106	VDD	PWR/GND	156	VDD	PWR/GND
107	VSS	PWR/GND	157	VSS	PWR/GND
108	D_ADRS(14)	INPUT	158	I_ADRS(09)	INPUT
109	D_DATA(30)	3-STATE	159	I_DATA(29)	3-STATE
110	D_DATA(31)	3-STATE	160	I_DATA(28)	3-STATE
111	D_DATA(32)	3-STATE	161	I_DATA(27)	3-STATE
112	VDD	PWR/GND	162	VDD	PWR/GND
113	VSS	PWR/GND	163	VSS	PWR/GND
114	D_DATA(33)	3-STATE	164	I_DATA(26)	3-STATE
115	D_DATA(34)	3-STATE	165	I_DATA(25)	3-STATE
116	D_DATA(35)	3-STATE	166	I_DATA(24)	3-STATE
117	D_DATA(36)	3-STATE	167	I_DATA(23)	3-STATE
118	VDD	PWR/GND	168	VDD	PWR/GND
119	VSS	PWR/GND	169	VSS	PWR/GND
120	D_DATA(37)	3-STATE	170	I_DATA(22)	3-STATE
121	D_DATA(38)	3-STATE	171	I_DATA(21)	3-STATE
122	D_DATA(39)	3-STATE	172	I_DATA(20)	3-STATE
123	D_$\overline{CS0}$	INPUT	173	I_$\overline{OE}$	INPUT
124	VDD	PWR/GND	174	VDD	PWR/GND
125	VSS	PWR/GND	175	VSS	PWR/GND
126	VSS	PWR/GND	176	VSS	PWR/GND
127	VDD	PWR/GND	177	VDD	PWR/GND
128	I_$\overline{CS0}$	INPUT	178	I_$\overline{WE}$	INPUT
129	I_DATA(39)	3-STATE	179	I_DATA(19)	3-STATE
130	I_DATA(38)	3-STATE	180	I_DATA(18)	3-STATE
131	I_DATA(37)	3-STATE	181	I_DATA(17)	3-STATE
132	VSS	PWR/GND	182	VSS	PWR/GND
133	VDD	PWR/GND	183	VDD	PWR/GND
134	I_DATA(36)	3-STATE	184	I_DATA(16)	3-STATE
135	I_DATA(35)	3-STATE	185	I_DATA(15)	3-STATE
136	I_DATA(34)	3-STATE	186	I_DATA(14)	3-STATE
137	I_DATA(33)	3-STATE	187	I_DATA(13)	3-STATE
138	VSS	PWR/GND	188	VSS	PWR/GND
139	VDD	PWR/GND	189	VDD	PWR/GND
140	I_DATA(32)	3-STATE	190	I_DATA(12)	3-STATE
141	I_DATA(31)	3-STATE	191	I_DATA(11)	3-STATE
142	I_DATA(30)	3-STATE	192	I_DATA(10)	3-STATE
143	I_ADRS(14)	INPUT	193	I_ADRS(08)	INPUT
144	VSS	PWR/GND	194	VSS	PWR/GND
145	VDD	PWR/GND	195	VDD	PWR/GND
146	I_ADRS(13)	INPUT	196	I_ADRS(07)	INPUT
147	I_CE1	INPUT	197	I_ADRS(06)	INPUT
148	I_CE0	INPUT	198	I_ADRS(05)	INPUT
149	VDD	PWR/GND	199	VDD	PWR/GND
150	VSS	PWR/GND	200	VSS	PWR/GND

FIGURE 2. Terminal connections - Continued.

Mode	Inputs 1/ 2/					Power
	CE0/CE1	$\overline{CS0}$/$\overline{CS}$ 1	$\overline{WE}$	$\overline{OE}$	D_DATA 0-39, I_DATA 0-39	
Write	High	Low	Low	Don't care	Data-in	Active
Read	High	Low	High	Low	Data-out	Active
Standby	Don't care	High	Don't care	Don't care	High-Z	Standby
Standby	Low	Don't care	Don't care	Don't care	High-Z	Standby

1/ V_{IN} for don't care inputs = V_{IH} or V_{IL}.

2/ When $\overline{OE}$ = high, I/O is High-Z.

FIGURE 3. Truth table.

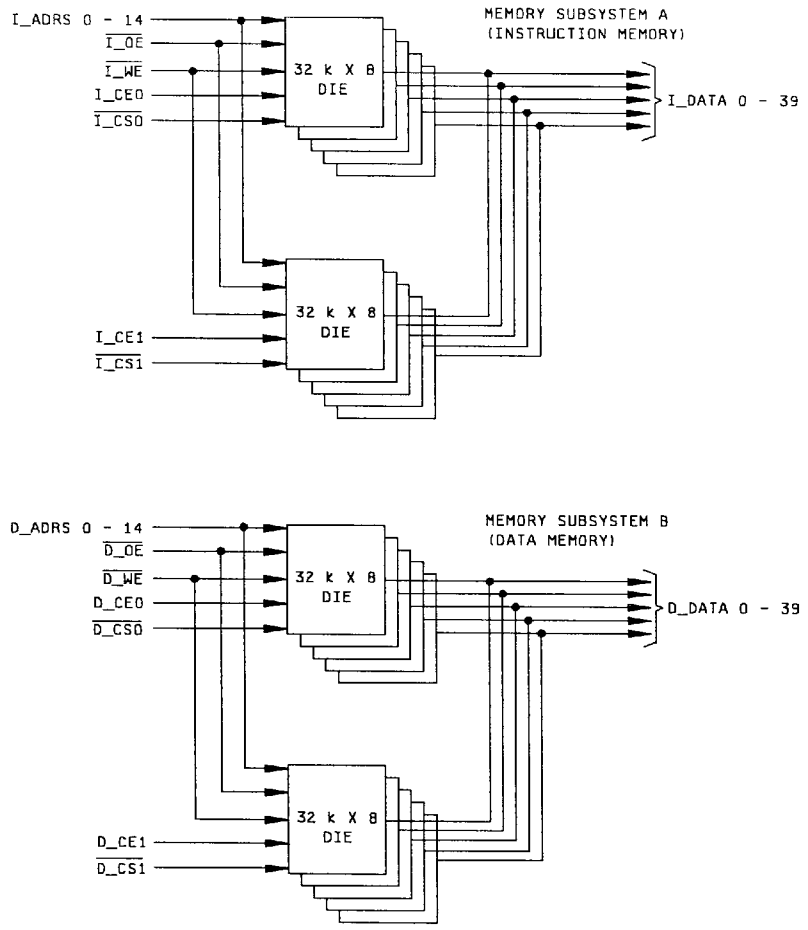
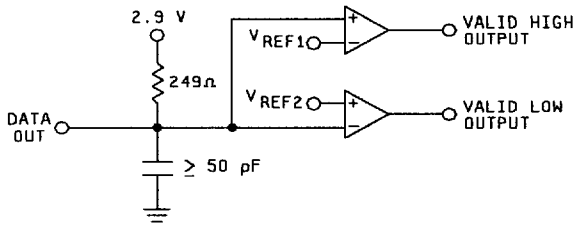


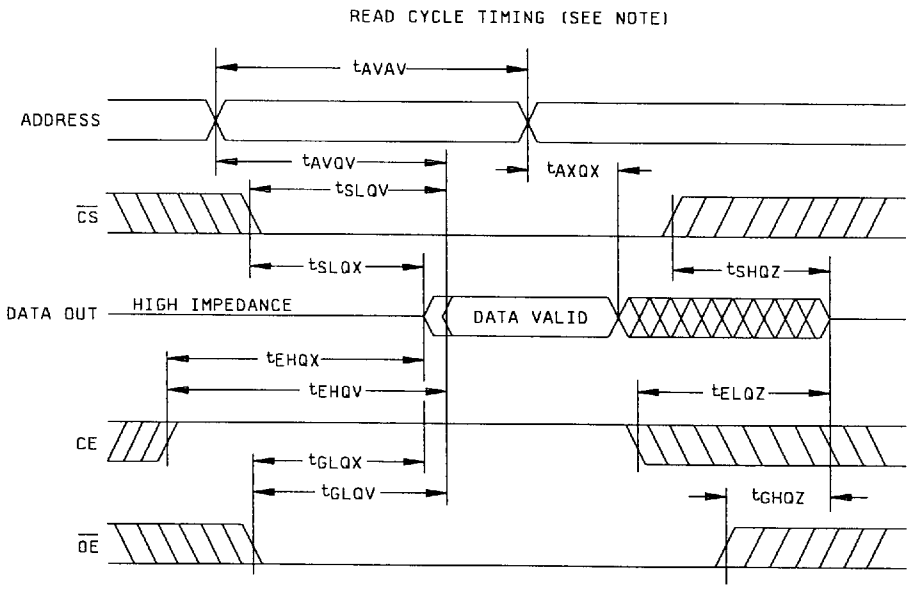
FIGURE 4. Logic diagram.



AC test conditions	
Input pulse levels	0.5 V to V_{DD} - 0.5 V
Input rise/fall times	≤5.0 ns
Input timing reference	$V_{DD}/2$
Output timing reference	$V_{DD}/2$

NOTE: Capacitance includes scope and jig values (minimum values).

FIGURE 5. Timing waveforms and output load circuit.



NOTE: $\overline{WE}$ is high for read cycle.

FIGURE 5. Timing waveforms and output load circuit. - Continued

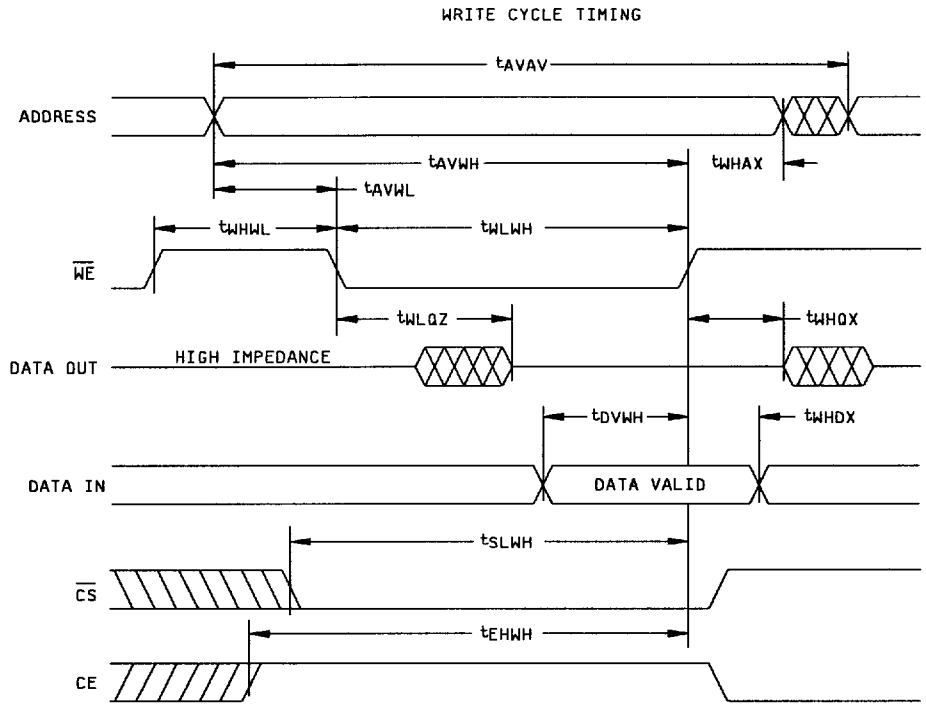
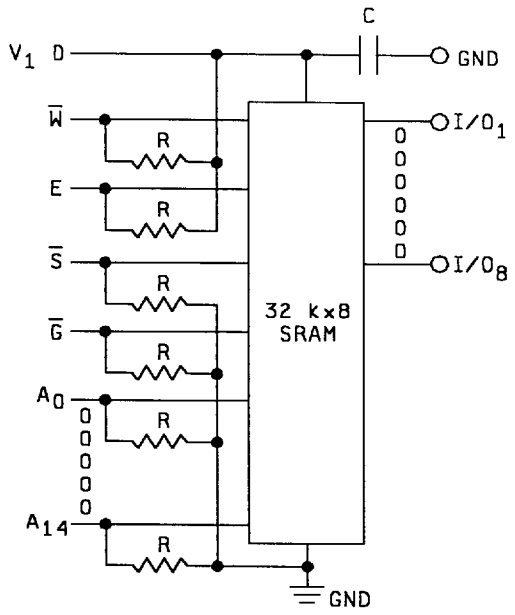


FIGURE 5. Timing waveforms and output load circuit. - Continued.



Notes:
1. Power pins connected to V_1
2. The absolute voltage ratings of 1.3 shall not be exceeded.
3. ESC precautions shall be followed.
4. The pattern in the memory array will be checkerboard for irradiation and accelerated aging test.
5. Pin conditions:

S = GND	V = V_{CC}	G = GND
E = V_{CC}	A_0 - A_{14} = GND	I/O_1 - I/O_8 = Floating
V_1 = V_{CC}	R = 10 kΩ ±10%	C = 0.1 μF ±10%
V_{CC} = 5.0 V		

Figure 6. Radiation exposure circuit

3.2.1 Microcircuit die. For device class M. Device class M devices covered by this drawing shall be in microcircuit group number H41 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Element evaluation.

4.2.1 Microcircuit dice. Microcircuit dice shall be produced on a QML certified line and probed at wafer level according to the manufacturer's QM plan.

4.2.2 Capacitors. Capacitor element evaluation shall be performed according to the manufacturer's QM plan.

4.2.3 Package evaluation. Packages shall be electrically tested by the package manufacturer. Element evaluation shall be performed according to the manufacturer's QM plan.

4.3 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.3.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.3.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

d. Those devices whose measured characteristics, after burn-in, exceed the specified delta (Δ) limits or electrical parameter limits specified in table IIB, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the PDA specified in the manufacturer's QM plan.

4.4 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.5.1 through 4.5.4).

4.5 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.5.1 through 4.5.4).

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.3)			1, 7, 9
2	Static burn-in I (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements	1, 2, 3, 4**, 7 8A, 8B, 9, 10, 11	2, 3, 4**, 7 8A, 8B, 9, 10, 11	2, 3, 4**, 7 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters	1, 2, 3, 7, 8A 8B, 9, 10, 11	1, 2, 3, 7, 8A 8B, 9, 10, 11	1, 2, 3, 7, 8A 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters	1, 7, 9	1, 7, 9	1, 7, 9
10	Group E end-point electrical parameters	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * Indicates PDA applies to subgroups 1 and 7.
5/ ** See 4.5.1c.
6/ Δ Indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the electrical parameters measured prior to the required burn-in(see table IIA).
7/ See 4.6.

TABLE IIB. Delta limits at +25°C.

Test 1/	Device types
	All
I_{CC3} (checkerboard pattern written)	±4.0 mA of value specified in table IA,
I_{IL}, I_{IH}	±10% or 1 μA, of value specified in table IA, whichever is greater
V_{OL}	±10% or 40 mV, of value specified in table IA, whichever is greater
V_{OH}	±10% or 60 mV, of value specified in table IA, whichever is greater

1/ The above parameters shall be recorded before and after the required burn-in and life tests to determine the delta.

4.5.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

d. O/V (latch-up) tests shall be measured at die level only and only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, with all input and output terminal types tested sufficient to verify capacitance.

4.5.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein.

4.5.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.5.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.5.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.5.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

c. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

d. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.5.4.1.1 Accelerated aging test. Accelerated aging shall be performed on all devices requiring a RHA level greater than 5 k rads(Si). The postanneal end point electrical parameter limits shall be as specified in table IA herein and shall be the preirradiation end point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may effect the RHA response of the device.

4.5.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.5.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing for class M devices shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Unless otherwise specified, test 10 devices with 0 defects.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices. SEP testing shall be performed on a technology process on the SEC or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be normal to the die surface and 60° to the normal, inclusive (i.e., 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ion/cm^2/s. The cross section shall be verified to be flux independent by measuring the cross section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be V_{DD} = 4.5 V dc for the upset measurements and V_{DD} = 5.5 V dc for the latchup measurements.

g. For SEP test limits see table IB herein.

4.6 Delta measurements for device classes Q and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latchup (SEP).

APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

30.2 Algorithm B (pattern 2).

30.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

30.3 Algorithm C (pattern 3).

30.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 97-10-07

Approved sources of supply for SMD 5962-96840 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H9684001VXC	34168	HX84050VHC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34168	Honeywell, Incorporated Solid State Electronics Center 12001 Hwy 55 Plymouth, MN 55441-4744

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.