查询"TPS73719-Q1"供应商

1-A LOW-DROPOUT REGULATOR WITH REVERSE CURRENT PROTECTION

FEATURES

- Qualified for Automotive Applications
- Stable with 1.0-μF or Larger Ceramic Output Capacitor
- Input Voltage Range: 2.2 V to 5.5 V
- Ultra-Low Dropout Voltage: 130 mV typ at 1 A
- Excellent Load Transient Response, Even With Only 1.0-μF Output Capacitor
- NMOS Topology Delivers Low Reverse Leakage Current
- 1.0% Initial Accuracy
- 3% Overall Accuracy Over Line, Load, and Temperature
- Less Than 20-nA (Typ) Quiescent Current in Shutdown Mode
- Thermal Shutdown and Current Limit for Fault Protection
- Available in Multiple Output Voltage Versions
  - Adjustable Output: 1.20 V to 5.5 V
  - Custom Outputs Available Using Factory Package-Level Programming

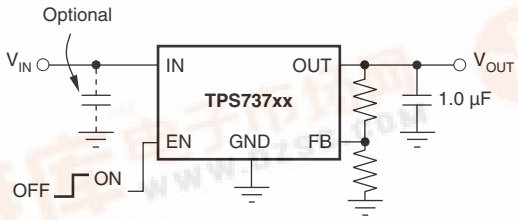
APPLICATIONS

- Point of Load Regulation for DSPs, FPGAs, ASICs, and Microprocessors
- Post-Regulation for Switching Supplies
- Portable/Battery-Powered Equipment

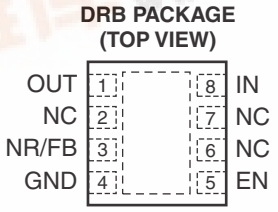
DESCRIPTION/ORDERING INFORMATION

The TPS737xx family of linear low-dropout (LDO) voltage regulators uses an NMOS pass element in a voltage-follower configuration. This topology is relatively insensitive to output capacitor value and ESR, allowing a wide variety of load configurations. Load transient response is excellent, even with a small 1.0-μF ceramic output capacitor. The NMOS topology also allows very low dropout.

The TPS737xx family uses an advanced BiCMOS process to yield high precision while delivering very low dropout voltages and low ground pin current. Current consumption, when not enabled, is under 20 nA and ideal for portable applications. These devices are protected by thermal shutdown and foldback current limit.



Typical Application Circuit



NC – No internal connection

ORDERING INFORMATION(1)

T_A	V_{OUT} (TYP)	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	3.3 V	SON – DRB	Reel of 3000	TPS73733QDRBRQ1	733Q
	1.9 V			TPS73719QDRBRQ1	719Q
	Adjustable			TPS73701QDRBRQ1	PREVIEW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

V_{IN} range	–0.3 V to 6.0 V
V_{EN} range	–0.3 V to 6.0 V
V_{OUT} range	–0.3 V to 5.5 V
V_{NR}, V_{FB} range	–0.3 V to 6.0 V
Peak output current	Internally limited
Output short-circuit duration	Indefinite
Continuous total power dissipation	See Dissipation Ratings Table
Junction temperature range, T_J	–55°C to 150°C
Storage temperature range	–65°C to 150°C
ESD rating, HBM	2000 V
ESD rating, CDM	500 V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the *Electrical Characteristics* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS(1)

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le$ 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
High-K(2)(3)	DRB	1.2°C/W	40°C/W	25.0 mW/°C	2.50 W	1.38 W	1.0 W

(1) See *Power Dissipation* in the *Applications* section for more information related to thermal design.
(2) The JEDEC High-K (2s2p) board design used to derive this data was a 3-inch x 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on the top and bottom of the board.
(3) Based on preliminary thermal simulations.

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ELECTRICAL CHARACTERISTICS

over operating temperature range (T_J = –40°C to 125°C), V_{IN} = ($V_{OUT(nom)}$ + 1.0 V)(1), I_{OUT} = 10 mA, V_{EN} = 2.2 V, C_{OUT} = 2.2 µF (unless otherwise noted). Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1), (2)			2.2		5.5	V
V_{FB}	Internal reference (TPS73701)		T_J = 25°C	1.192	1.2	1.216	V
V_{OUT}	Output voltage range (TPS73701)(3)			V_{FB}		5.5 – V_{DO}	V
	Accuracy(1), (4)	Nominal	T_J = 25°C	–1.0		+1.0	%
			5.36 V < V_{IN} < 5.5 V, V_{OUT} = 5.08 V, 10 mA < I_{OUT} < 800 mA, –40°C < T_J < 85°C, TPS73701	–2.0		+2.0	
		Over V_{IN}, I_{OUT}, and temperature	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5.5 V, 10 mA ≤ I_{OUT} ≤ 1 A	–3.0	±0.5	+3.0	
ΔV_{OUT}%/ ΔV_{IN}	Line regulation(1)		$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V		0.01		%/V
ΔV_{OUT}%/ ΔI_{OUT}	Load regulation		1 mA ≤ I_{OUT} ≤ 1 A		0.002		%/mA
			10 mA ≤ I_{OUT} ≤ 1 A		0.0005		
V_{DO}	Dropout voltage(5) (V_{IN} = $V_{OUT(nom)}$ – 0.1 V)		I_{OUT} = 1 A		130	500	mV
Z_O(DO)	Output impedance in dropout		2.2 V ≤ V_{IN} ≤ V_{OUT} + V_{DO}		0.25		Ω
I_{CL}	Output current limit		V_{OUT} = 0.9 × $V_{OUT(nom)}$	1.05	1.6	2.2	A
I_{SC}	Short-circuit current		V_{OUT} = 0 V		450		mA
I_{REV}	Reverse leakage current(6) ($-I_{IN}$)		V_{EN} ≤ 0.5 V, 0 V ≤ V_{IN} ≤ V_{OUT}		0.1		µA
I_{GND}	GND pin current		I_{OUT} = 10 mA (I_Q)		400		µA
			I_{OUT} = 1 A		1300		
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.5 V, V_{OUT} ≤ V_{IN} ≤ 5.5 V		20		nA
I_{FB}	FB pin current (TPS73701)				0.1	0.6	µA
PSRR	Power-supply rejection ratio (ripple rejection)		f = 100 Hz, I_{OUT} = 1 A		58		dB
			f = 10 kHz, I_{OUT} = 1 A		37		
V_N	Output noise voltage BW = 10 Hz to 100 kHz		C_{OUT} = 10 µF		27 × V_{OUT}		μV_{RMS}
t_{STR}	Startup time		V_{OUT} = 3 V, R_L = 30 Ω, C_{OUT} = 1 µF		600		µs
$V_{EN(HI)}$	EN pin high (enabled)			1.7		V_{IN}	V
$V_{EN(LO)}$	EN pin low (shutdown)			0		0.5	V
$I_{EN(HI)}$	EN pin current (enabled)		V_{EN} = 5.5 V		20		nA
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing		160		°C
			Reset, temperature decreasing		140		
T_J	Operating junction temperature			–40		125	°C

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.2V, whichever is greater.
(2) For $V_{OUT(nom)}$ < 1.6 V, when V_{IN} ≤ 1.6 V, the output will lock to V_{IN} and may result in an overvoltage condition on the output. To avoid this situation, disable the device before powering down V_{IN}.
(3) TPS73701 is tested at V_{OUT} = 1.2 V.
(4) Tolerance of external resistors not included in this specification.
(5) V_{DO} is not measured for fixed output versions with $V_{OUT(nom)}$ < 2.3 V, because minimum V_{IN} = 2.2 V.
(6) Fixed-voltage versions only; see the *Applications* section for more information.

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FUNCTIONAL BLOCK DIAGRAMS

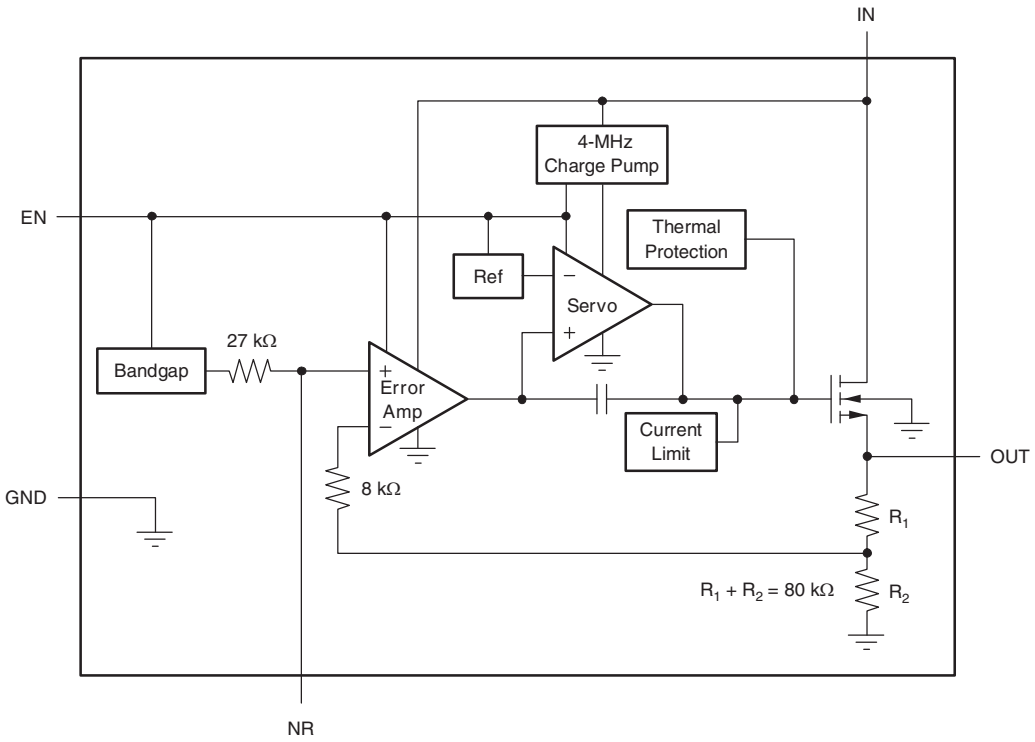
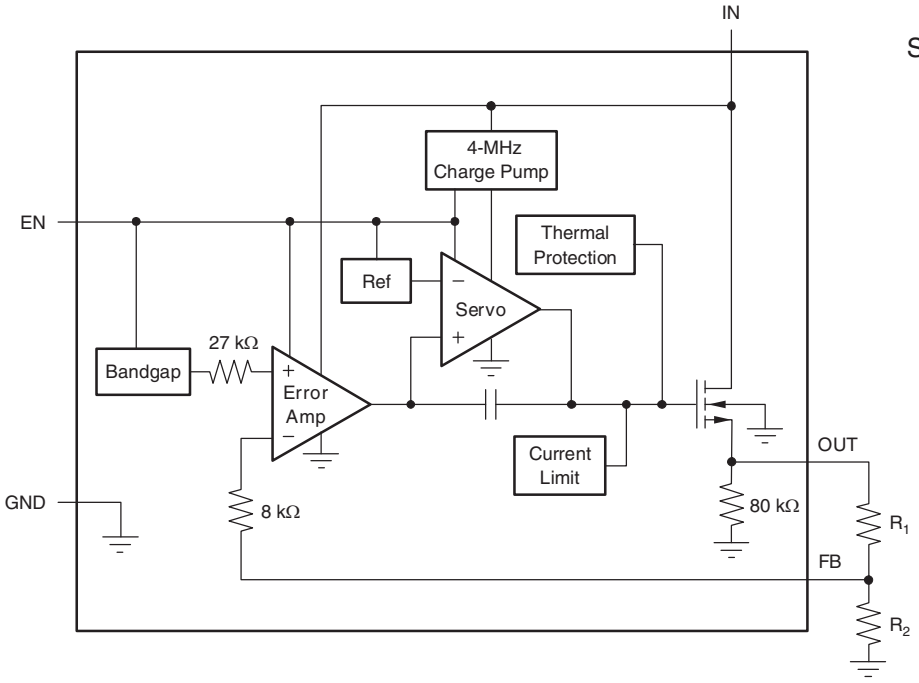


Figure 1. Fixed Voltage Version



Standard 1% Resistor Values for Common Output Voltages

V_O	R_1	R_2
1.2 V	Short	Open
1.5 V	23.2 kΩ	95.3 kΩ
1.8 V	28.0 kΩ	56.2 kΩ
2.5 V	39.2 kΩ	36.5 kΩ
2.8 V	44.2 kΩ	33.2 kΩ
3.0 V	46.4 kΩ	30.9 kΩ
3.3 V	52.3 kΩ	30.1 kΩ

NOTE: $V_{OUT} = (R_1 + R_2)/R_2 \times 1.204$; $R_1 \parallel R_2 \cong 19$ kΩ for best accuracy.

Figure 2. Adjustable Voltage Version

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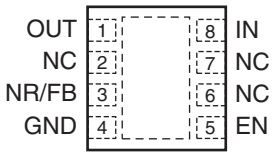
DRB PACKAGE
3mm x 3mm SON
(TOP VIEW)



NC – No internal connection

Table 1. Terminal Functions

TERMINAL		DESCRIPTION
NAME	NO.	
IN	8	Unregulated input supply
GND	4, Pad	Ground
EN	5	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. Refer to the *Shutdown* section under *Applications Information* for more details. EN must not be left floating and can be connected to IN if not used.
NR	3	Fixed voltage versions only. Connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, reducing output noise to very low levels.
FB	3	Adjustable voltage version only. This is the input to the control loop error amplifier, and it is used to set the output voltage of the device.
OUT	1	Regulator output. A 1.0-µF or larger capacitor of any type is required for stability.
NC	2, 6, 7	No internal connection

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TYPICAL CHARACTERISTICS

T_J = 25°C, V_{IN} = ($V_{OUT(nom)}$ + 1.0 V), I_{OUT} = 10 mA, V_{EN} = 2.2 V, C_{OUT} = 2.2 µF (unless otherwise noted)

LOAD REGULATION

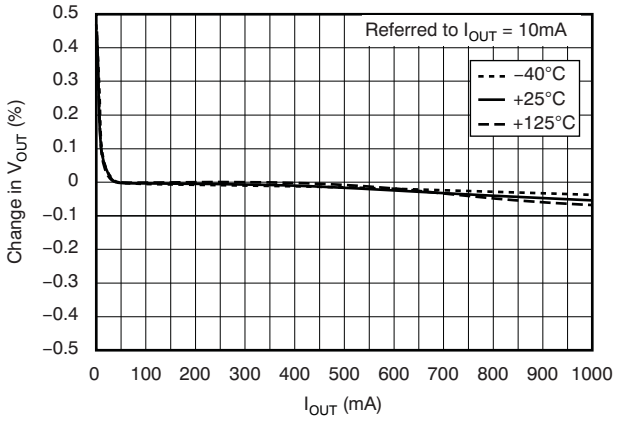

Figure 3.

LINE REGULATION

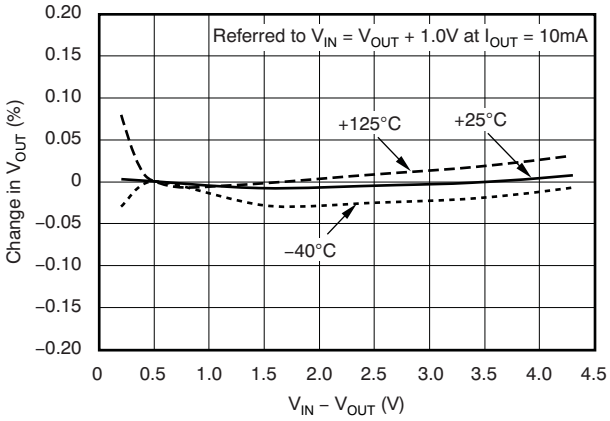

Figure 4.

DROPOUT VOLTAGE vs OUTPUT CURRENT

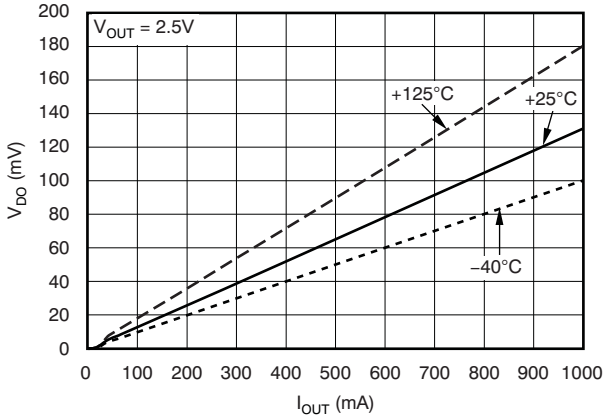

Figure 5.

DROPOUT VOLTAGE vs TEMPERATURE

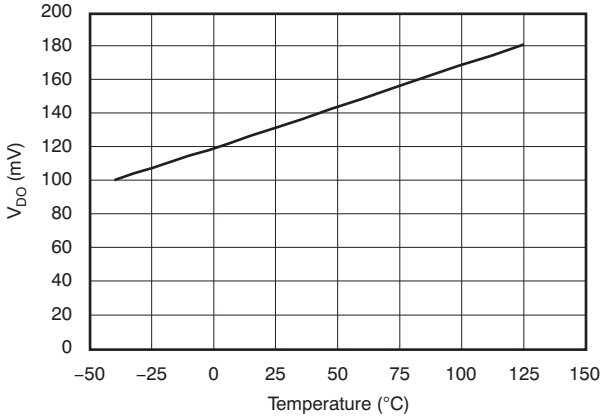

Figure 6.

OUTPUT VOLTAGE HISTOGRAM

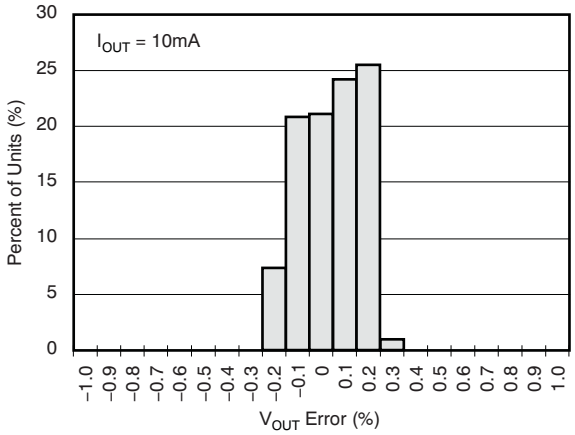

Figure 7.

DROPOUT VOLTAGE DRIFT HISTOGRAM

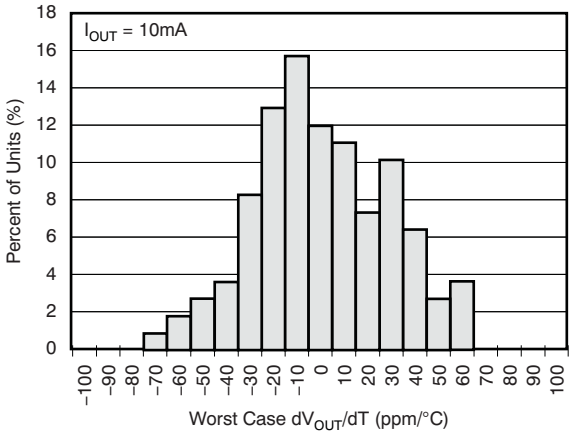

Figure 8.

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TYPICAL CHARACTERISTICS (continued)

T_J = 25°C, V_{IN} = ($V_{OUT(nom)}$ + 1.0 V), I_{OUT} = 10 mA, V_{EN} = 2.2 V, C_{OUT} = 2.2 µF (unless otherwise noted)

GROUND PIN CURRENT vs OUTPUT CURRENT

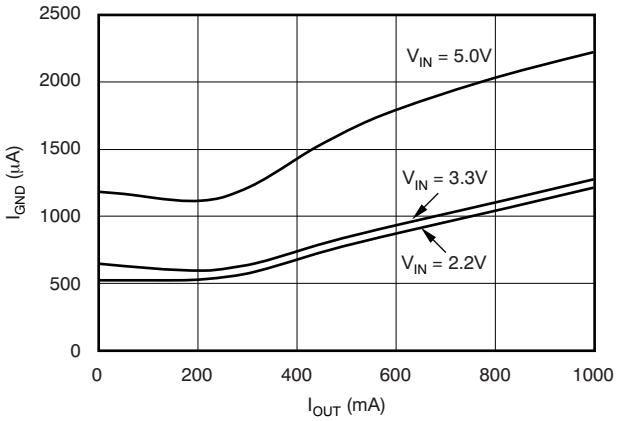

Figure 9.

GROUND PIN CURRENT vs TEMPERATURE

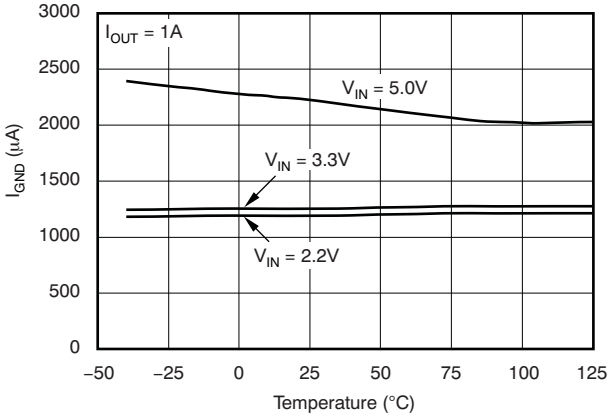

Figure 10.

GROUND PIN CURRENT IN SHUTDOWN vs TEMPERATURE

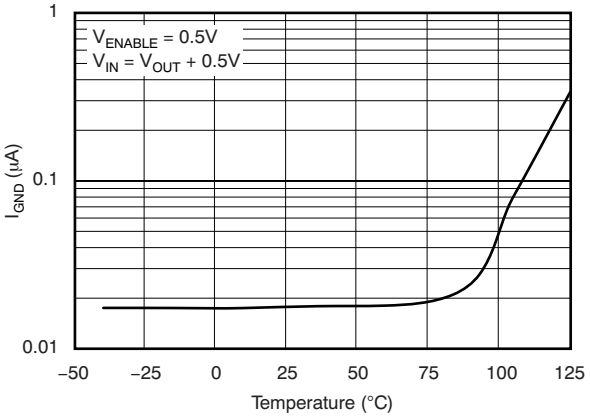

Figure 11.

CURRENT LIMIT vs V_{OUT} (FOLDBACK)

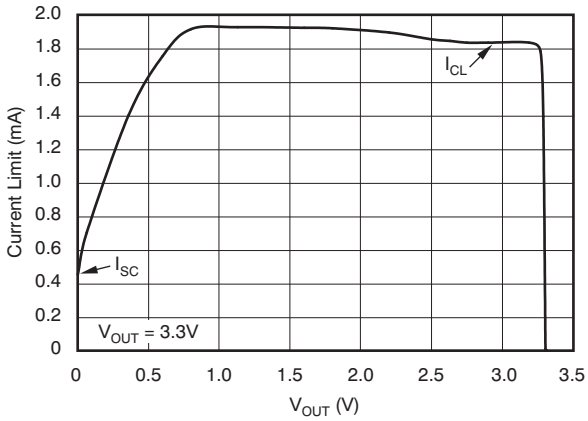

Figure 12.

CURRENT LIMIT vs V_{IN}

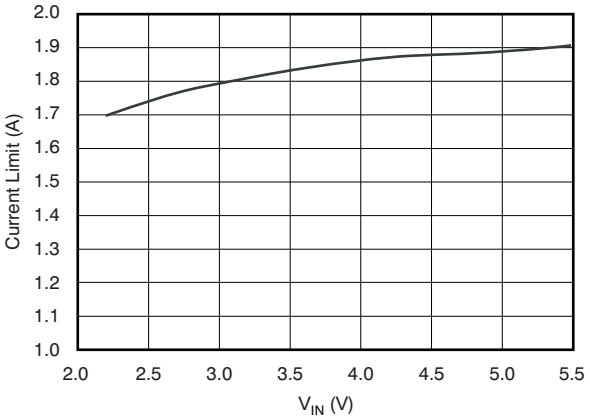

Figure 13.

CURRENT LIMIT vs TEMPERATURE

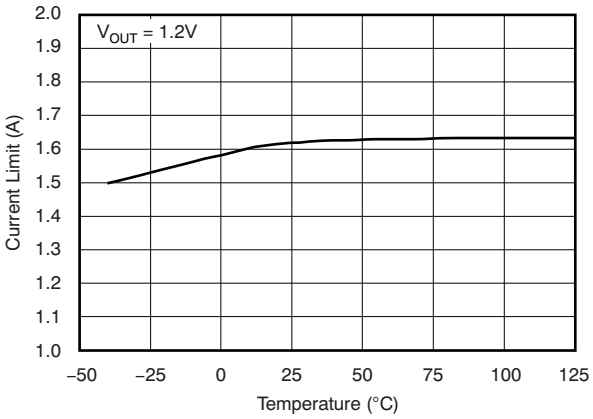

Figure 14.

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TYPICAL CHARACTERISTICS (continued)

T_J = 25°C, V_{IN} = ($V_{OUT(nom)}$ + 1.0 V), I_{OUT} = 10 mA, V_{EN} = 2.2 V, C_{OUT} = 2.2 µF (unless otherwise noted)

PSRR (RIPPLE REJECTION) vs FREQUENCY

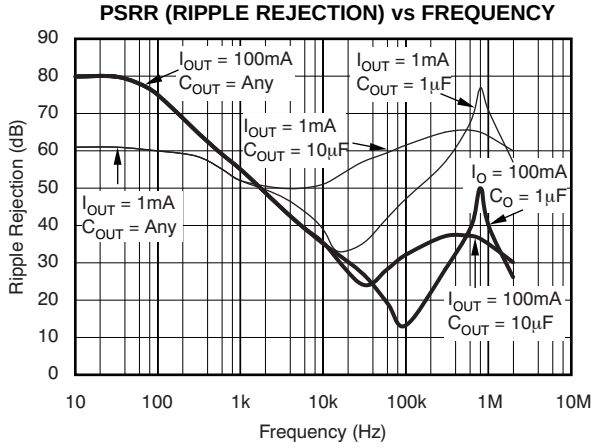

Figure 15.

PSRR (RIPPLE REJECTION) vs $V_{IN} - V_{OUT}$

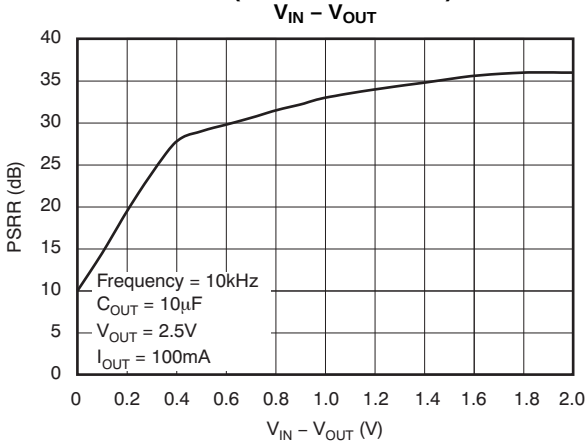

Figure 16.

NOISE SPECTRAL DENSITY

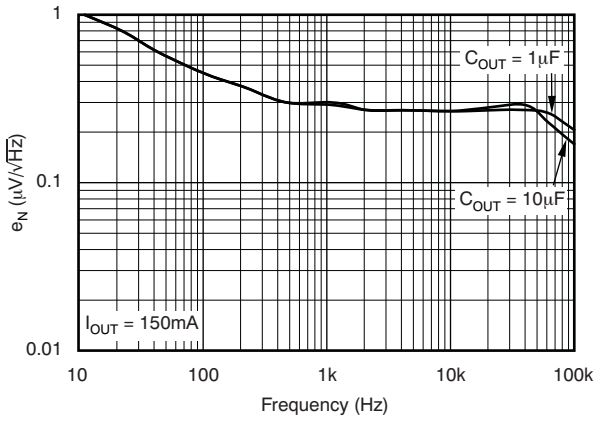

Figure 17.

TPS73701
RMS NOISE VOLTAGE vs C_{FB}

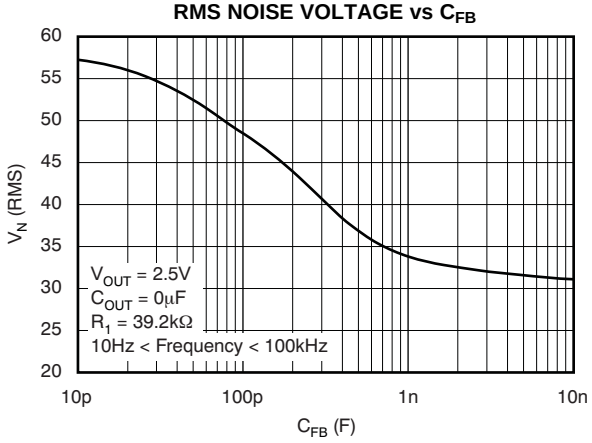

Figure 18.

RMS NOISE VOLTAGE vs C_{OUT}

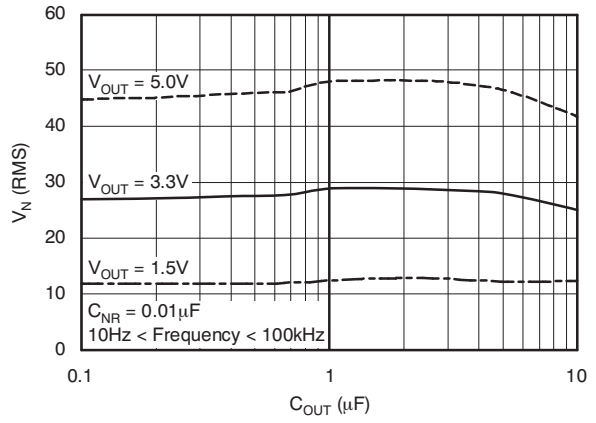

Figure 19.

RMS NOISE VOLTAGE vs C_{NR}

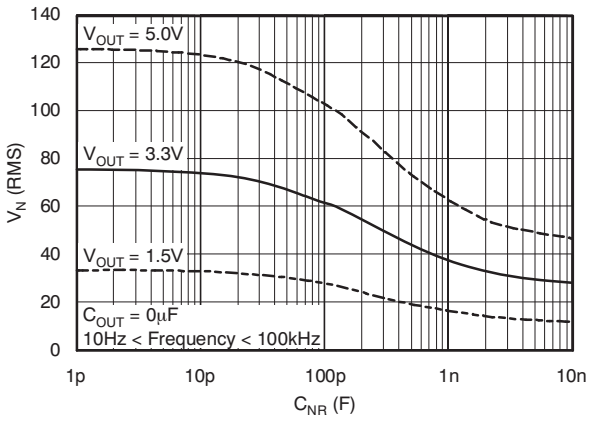

Figure 20.

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TYPICAL CHARACTERISTICS (continued)

T_J = 25°C, V_{IN} = ($V_{OUT(nom)}$ + 1.0 V), I_{OUT} = 10 mA, V_{EN} = 2.2 V, C_{OUT} = 2.2 µF (unless otherwise noted)

TPS73733
LOAD TRANSIENT RESPONSE

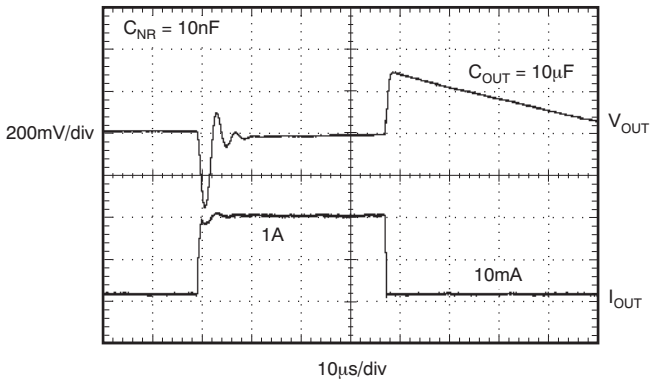

Figure 21.

TPS73733
LINE TRANSIENT RESPONSE

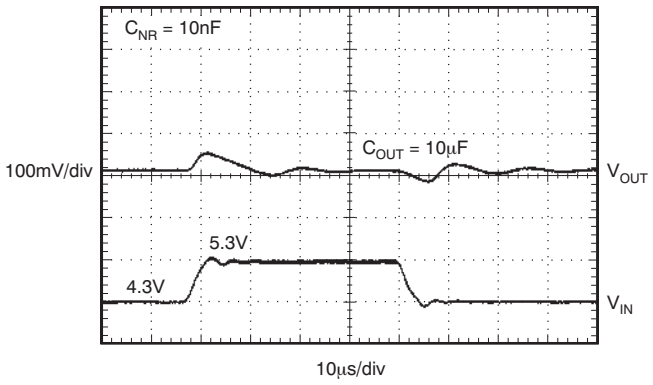

Figure 22.

TPS73701
TURN-ON RESPONSE

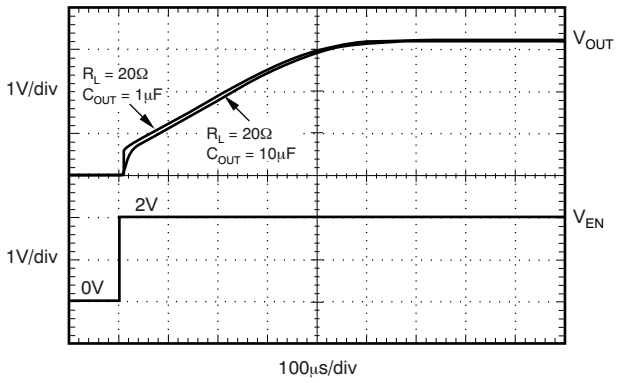

Figure 23.

TPS73701
TURN-OFF RESPONSE

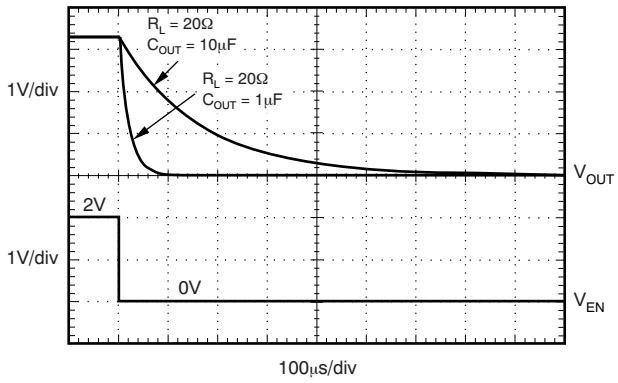

Figure 24.

TPS73701, V_{OUT} = 3.3V
POWER-UP/POWER-DOWN

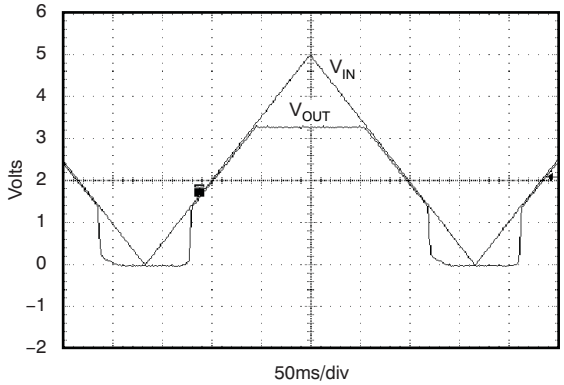

Figure 25.

I_{ENABLE} vs TEMPERATURE

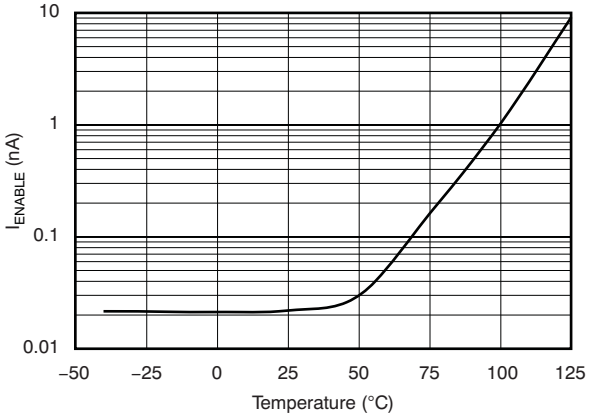

Figure 26.

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TYPICAL CHARACTERISTICS (continued)

T_J = 25°C, V_{IN} = ($V_{OUT(nom)}$ + 1.0 V), I_{OUT} = 10 mA, V_{EN} = 2.2 V, C_{OUT} = 2.2 µF (unless otherwise noted)

TPS73701
I_{FB} vs TEMPERATURE

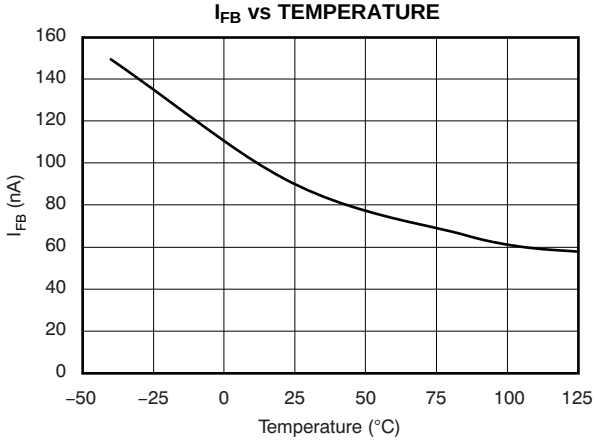

Figure 27.

TPS73701
I_{FB} vs TEMPERATURE

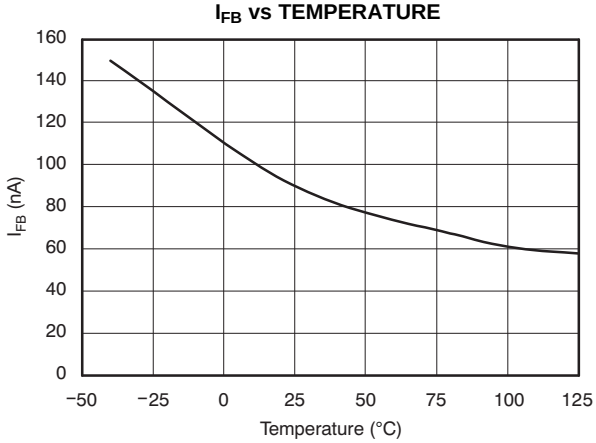

Figure 28.

TPS73701
LOAD TRANSIENT, ADJUSTABLE VERSION

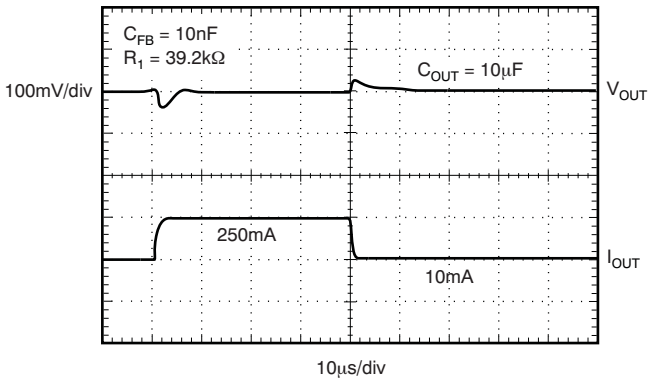

Figure 29.

TPS73701
LINE TRANSIENT, ADJUSTABLE VERSION

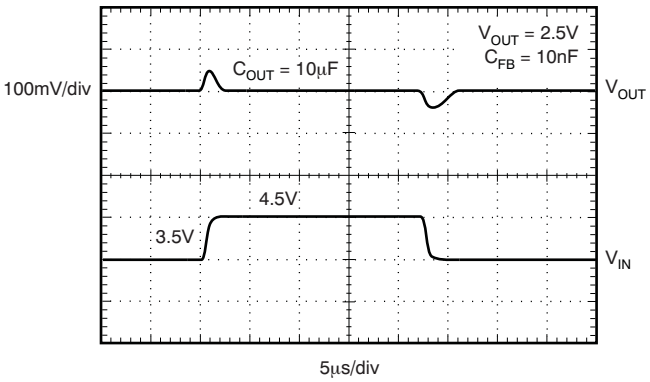

Figure 30.

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APPLICATION INFORMATION

The TPS737xx belongs to a family of new generation LDO regulators that use an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features combined with an enable input make the TPS737xx ideal for portable applications. This regulator family offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and over-current protection, including foldback current limit.

Figure 31 shows the basic circuit connections for the fixed voltage models. Figure 32 gives the connections for the adjustable output version (TPS73701).

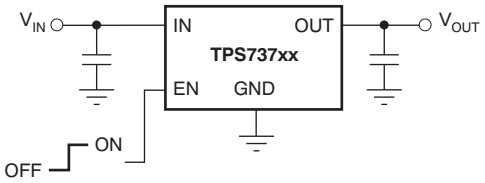

Figure 31. Typical Application Circuit for Fixed-Voltage Versions

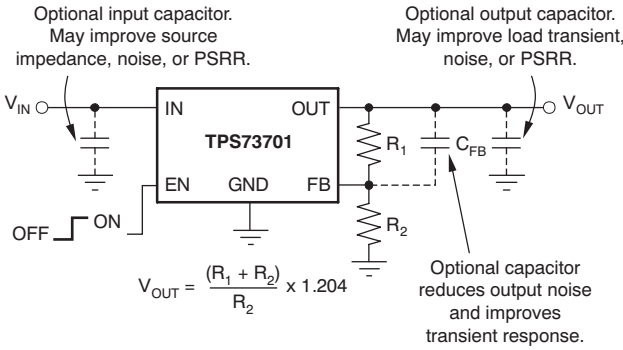

Figure 32. Typical Application Circuit for Adjustable-Voltage Version

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 32. Sample resistor values for common output voltages are shown in Figure 2.

For best accuracy, make the parallel combination of R_1 and R_2 approximately equal to 19 kΩ. This 19 kΩ, in addition to the internal 8-kΩ resistor, presents the same impedance to the error amp as the 27-kΩ bandgap reference output. This impedance helps compensate for leakages into the error amp terminals.

Input and Output Capacitor Requirements

Although an input capacitor is not required for stability if input impedance is very low, it is good analog design practice to connect a 0.1-µF to 1-µF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS737xx requires a 1.0-µF output capacitor for stability. It is designed to be stable for all available types and values of capacitors. In applications where multiple low ESR capacitors are in parallel, ringing may occur when the product of C_{OUT} and total ESR drops below 50 nΩF. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance will meet this requirement.

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Output Noise

A precision bandgap reference is used to generate the internal reference voltage, V_{REF}. This reference is the dominant noise source within the TPS737xx and it generates approximately 32 μV_{RMS} (10 Hz to 100 kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_N = 32\mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \quad (1)$$

Since the value of V_{REF} is 1.2V, this relationship reduces to:

$$V_N(\mu V_{RMS}) = 27\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}\,(V) \quad (2)$$

for the case of no C_{NR}.

An internal 27kΩ resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor, C_{NR}, is connected from NR to ground. For C_{NR} = 10 nF, the total noise in the 10-Hz to 100-kHz bandwidth is reduced by a factor of ~3.2, giving the approximate relationship in Equation 3 for C_{NR} = 10 nF.

$$V_N(\mu V_{RMS}) = 8.5\left(\frac{\mu V_{RMS}}{V}\right) x\, V_{OUT}(V) \quad (3)$$

This noise reduction effect is shown as RMS Noise Voltage vs C_{NR} in the Typical Characteristics section.

The TPS73701 adjustable version does not have the NR pin available. However, connecting a feedback capacitor, C_{FB}, from the output to the feedback pin (FB) reduces output noise and improve load transient performance. This capacitor should be limited to 0.1 µF.

The TPS737xx uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above V_{OUT}. The charge pump generates ~250 µV of switching noise at ~4 MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT}.

Board Layout Recommendation to Improve PSRR and Noise Performance

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the printed circuit board (PCB) be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Internal Current Limit

The TPS737xx internal current limit helps protect the regulator during fault conditions. Foldback current limit helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5 V. See Figure 12 in the Typical Characteristicssection.

Enable Pin and Shutdown

The enable pin (EN) is active high and is compatible with standard TTL-CMOS levels. A V_{EN} below 0.5 V (max) turns the regulator off and drops the GND pin current to approximately 10 nA. When EN is used to shutdown the regulator, all charge is removed from the pass transistor gate, and the output ramps back up to a regulated V_{OUT} (see Figure 23).

When shutdown capability is not required, EN can be connected to V_{IN}. However, the pass gate may not be discharged using this configuration, and the pass transistor may be left on (enhanced) for a significant time after V_{IN} has been removed. This scenario can result in reverse current flow (if the IN pin is low impedance) and faster ramp times upon power-up. In addition, for V_{IN} ramp times slower than a few milliseconds, the output may overshoot upon power-up.

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Dropout Voltage

The TPS737xx uses an NMOS pass transistor to achieve extremely low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the NMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS, ON}$ of the NMOS pass element.

For large step changes in load current, the TPS737xx requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the dc dropout. Values of V_{IN} – V_{OUT} above this line ensure normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions [full-scale instantaneous load change with (V_{IN} – V_{OUT}) close to dc dropout levels], the TPS737xx can take a couple of hundred microseconds to return to the specified regulation accuracy.

Transient Response

The low open-loop output impedance provided by the NMOS pass element in a voltage follower configuration allows operation without a 1.0-µF output capacitor. As with any regulator, the addition of additional capacitance from the OUT pin to ground reduces undershoot magnitude but increases its duration. In the adjustable version, the addition of a capacitor, C_{FB}, from the OUT pin to the FB pin will also improve the transient response.

The TPS737xx does not have active pulldown when the output is overvoltage. This architecture allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This architecture also results in an output overshoot of several percent if the load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal/external load resistance. The rate of decay is given by Equation 4 and Equation 5.

(Fixed voltage version)

$$\frac{dV}{dT} = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel R_{LOAD}} \quad (4)$$

(Adjustable voltage version)

$$\frac{dV}{dT} = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel (R_1 + R_2) \parallel R_{LOAD}} \quad (5)$$

Reverse Current

The NMOS pass element of the TPS737xx provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To ensure that all charge is removed from the gate of the pass element, the EN pin must be driven low before the input voltage is removed. If this is not done, the pass element may be left on because of stored charge on the gate.

After the EN pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Note that reverse current is specified as the current flowing out of the IN pin because of voltage applied on the OUT pin. There will be additional current flowing into the OUT pin as a result of the 80-kΩ internal resistor divider to ground (see Figure 1 and Figure 2).

For the TPS73701, reverse current may flow when V_{FB} is more than 1.0V above V_{IN}.

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Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS737xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS737xx into thermal shutdown degrades device reliability.

Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are shown in the Power Dissipation Ratings table. Using heavier copper will increase the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

Package Mounting

Solder pad footprint recommendations for the TPS737xx are presented in Application Bulletin *Solder Pad Recommendations for Surface-Mount Devices* (SBFA015), available from the Texas Instruments web site at www.ti.com.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS73719QDRBRQ1	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS73733QDRBRQ1	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF TPS73733-Q1 :
- Catalog: TPS73733

NOTE: Qualified Version Definitions:
- Catalog - TI's standard catalog product

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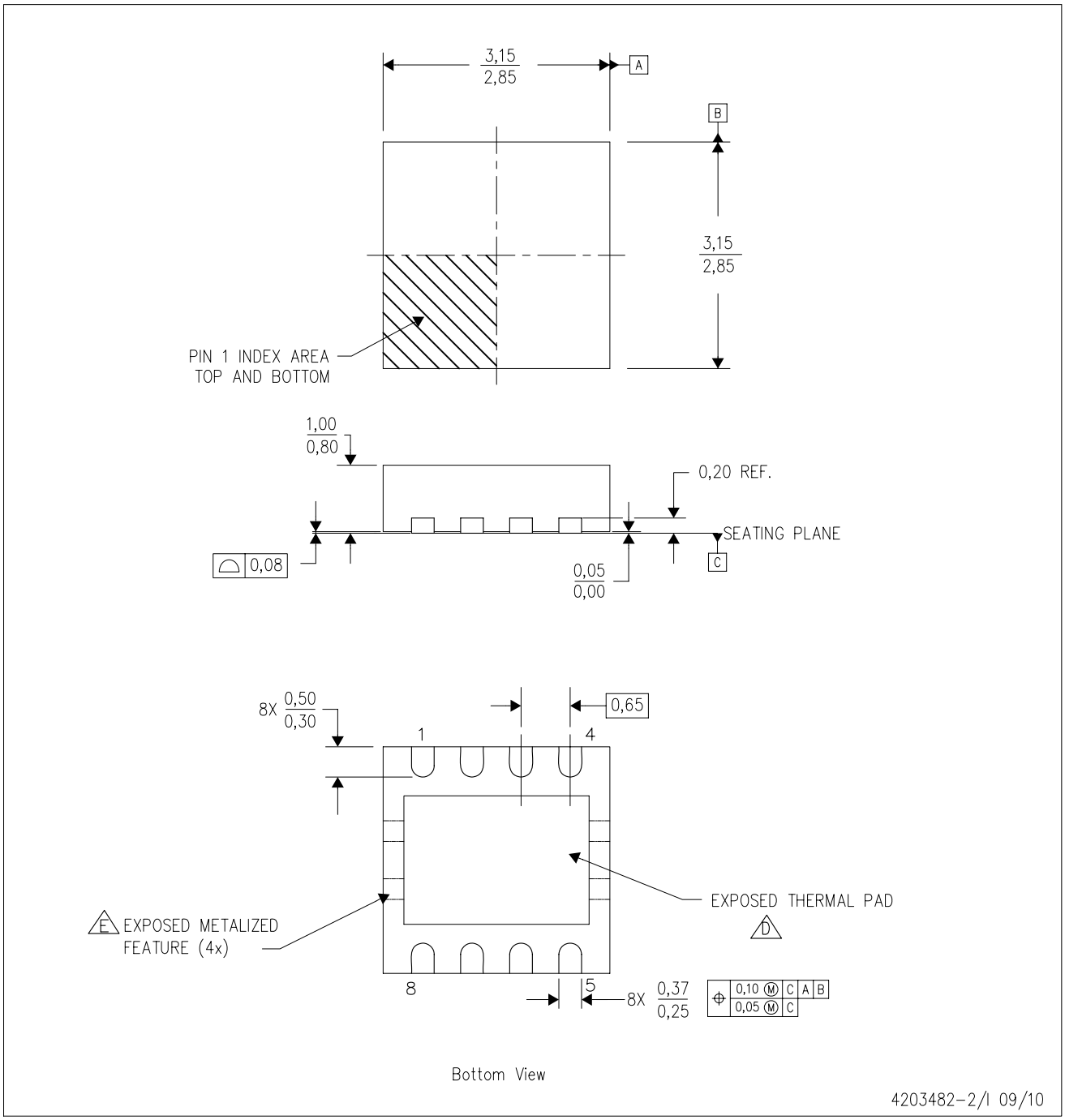
DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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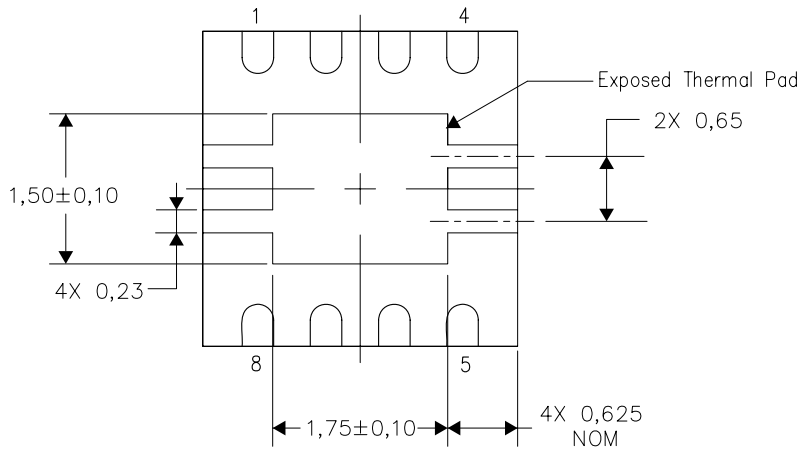
DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206340–2/K 11/10

NOTE: A. All linear dimensions are in millimeters

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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps

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