Power MOSFET, 40 A

SOT-227

FEATURES

- Low gate charge Q_g results in simple drive requirement
- Improved gate, avalanche and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Low $R_{DS(on)}$
- Fully insulated package
- UL pending
- Compliant to RoHS directive 2002/95/EC
- Designed and qualified for industrial level

Pb-free
RoHS COMPLIANT

APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- High speed power switching
- Hard switched and high frequency circuits

PRODUCT SUMMARY	
V_{DSS}	500 V
$R_{DS(on)}$ (typical)	0.084 Ω
I_D	40 A
Type	Modules - MOSFET
Package	SOT-227

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Continuous drain current, V_{GS} at 10 V	I_D	T_C = 25 °C	40	A
		T_C = 100 °C	26	
Pulsed drain current	I_{DM} (1)		160	
Power dissipation	P_D	T_C = 25 °C	430	W
Linear derating factor			3.45	W/°C
Gate to source voltage	V_{GS}		± 30	V
Peak diode recovery dV/dt	dV/dt (2)		9.0	V/ns
Operating junction and storage temperature range	T_J, T_{Stg}		- 55 to + 150	°C

Notes

(1) Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

(2) I_{SD} ≤ 40 A, dI/dt ≤ 150 A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 150 °C

AVALANCHE CHARACTERISTICS

PARAMETER	SYMBOL	TYP.	MAX.	UNITS
Single pulse avalanche energy	E_{AS} (1)	-	1240	mJ
Avalanche current	I_{AR} (2)	-	40	A
Repetitive avalanche energy	E_{AR} (2)	-	43	mJ

Notes

(1) Starting T_J = 25 °C, L = 1.55 mH, R_g = 25 Ω, I_{AS} = 40 A, dV/dt = 5.5 V/ns (see fig. 12a)

(2) Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

THERMAL RESISTANCE				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNITS**
Junction to case	R_{thJC}	-	0.29	°C/W
Case to sink, flat, greased surface	R_{thCS}	0.05	-	

STATIC CHARACTERISTICS (T_J = 25 °C unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Drain to source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	500	-	-	V
Breakdown voltage temperature coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to 25 °C, I_D = 1 mA	-	0.60	-	V/°C
Static drain to source on-resistance	$R_{DS(on)}$ (1)	V_{GS} = 10 V, I_D = 24 A	-	0.084	0.10	Ω
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	3.0	-	5.0	V
Drain to source leakage current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V	-	-	50	µA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C	-	-	250	
Gate to source forward leakage	I_{GSS}	V_{GS} = 30 V	-	-	250	nA
Gate to source reverse leakage		V_{GS} = - 30 V	-	-	- 250	

Note

(1) Pulse width ≤ 300 µs; duty cycle ≤ 2 %

DYNAMIC CHARACTERISTICS (T_J = 25 °C unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Forward transconductance	g_{fs}	V_{DS} = 50 V, I_D = 28 A	23	-	-	S
Total gate charge	Q_g (1)	I_D = 40 A V_{DS} = 400 V V_{GS} = 10 V; see fig. 6 and 13	-	-	270	nC
Gate to source charge	Q_{gs} (1)		-	-	84	
Gate to drain ("Miller") charge	Q_{gd} (1)		-	-	130	
Turn-on delay time	$t_{d(on)}$ (1)	V_{DD} = 250 V I_D = 40 A R_g = 1.0 Ω V_{GS} = 10 V, see fig. 10	-	25	-	ns
Rise time	t_r (1)		-	140	-	
Turn-off delay time	$t_{d(off)}$ (1)		-	55	-	
Fall time	t_f (1)		-	74	-	
Input capacitance	C_{iss}	V_{GS} = 0 V V_{DS} = 25 V f = 1.0 MHz, see fig. 5	-	8310	-	pF
Output capacitance	C_{oss}		-	960	-	
Reverse transfer capacitance	C_{rss}		-	120	-	
Output capacitance	C_{oss}	V_{GS} = 0 V, V_{DS} = 1.0 V, f = 1.0 MHz	-	10 170	-	
		V_{GS} = 0 V, V_{DS} = 480 V, f = 1.0 MHz	-	240	-	
Effective output capacitance	C_{oss} eff. (2)	V_{GS} = 0 V, V_{DS} = 0 V to 480 V	-	440	-	

Notes

(1) Pulse width ≤ 300 µs; duty cycle ≤ 2 %

(2) C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DSS}

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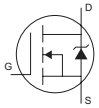
DIODE CHARACTERISTICS						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Continuous source current (body diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode 	-	-	40	A
Pulsed source current (body diode)	I_{SM} (1)		-	-	160	
Diode forward voltage	V_{SD} (2)	T_J = 25 °C, I_S = 40 A, V_{GS} = 0 V	-	-	1	V
Reverse recovery time	t_{rr} (2)	T_J = 25 °C, I_F = 47 A; dI/dt = 100 A/µs	-	620	940	ns
Reverse recovery charge	Q_{rr}		-	14	21	µC
Reverse recovery current	I_{RRM}	T_J = 25 °C	-	38	-	A
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S + L_D)				

Notes

(1) Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

(2) Pulse width ≤ 300 µs; duty cycle ≤ 2 %

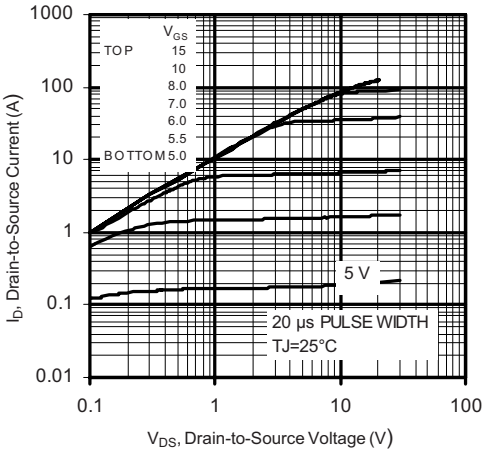


Fig. 1 - Typical Output Characteristics

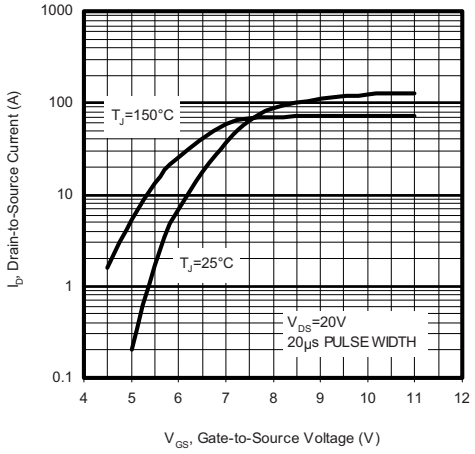


Fig. 3 - Typical Transfer Characteristics

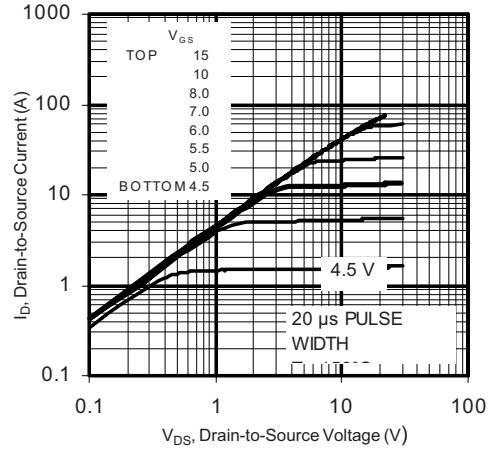


Fig. 2 - Typical Output Characteristics

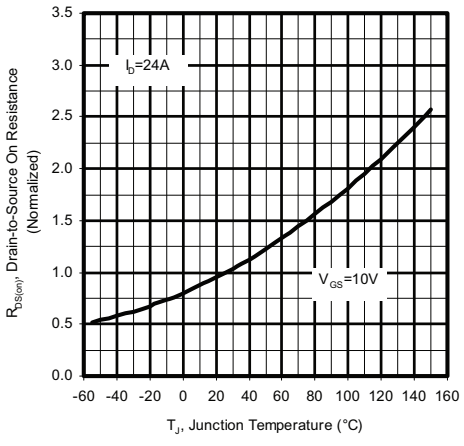


Fig. 4 - Normalized On-Resistance vs. Temperature

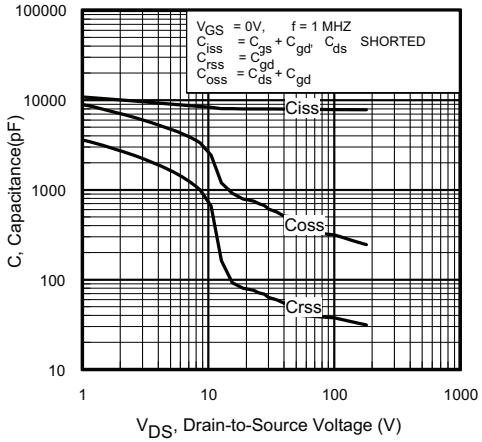


Fig. 5 - Typical Capacitance vs. Drain to Source Voltage

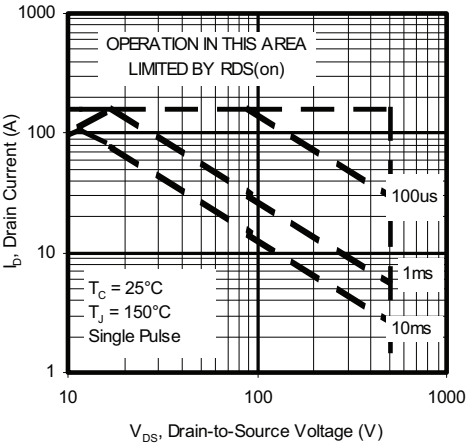


Fig. 8 - Maximum Safe Operating Area

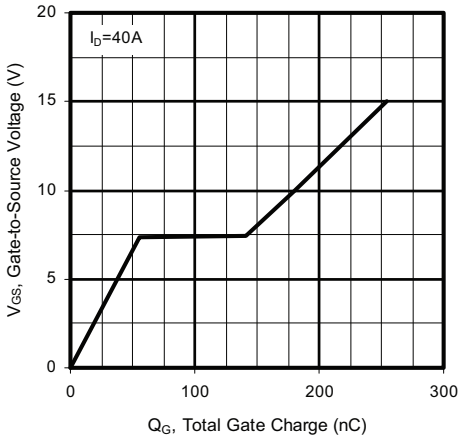


Fig. 6 - Typical Gate Charge vs. Gate to Source Voltage

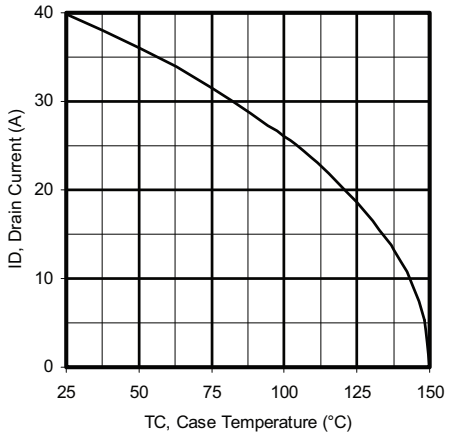


Fig. 9 - Maximum Drain Current vs. Case Temperature

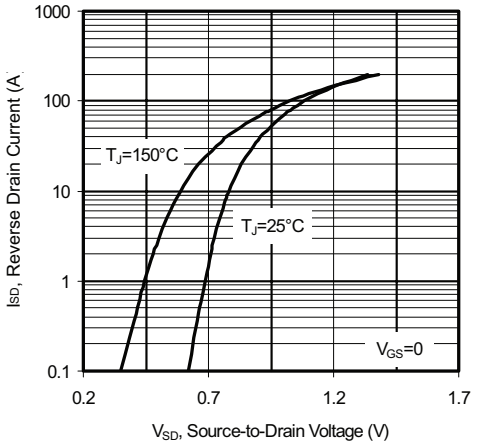


Fig. 7 - Typical Source Drain Diode Forward Voltage

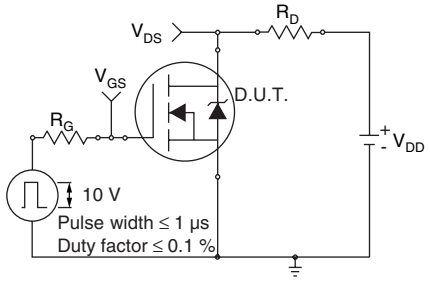


Fig. 10a - Switching Time Test Circuit

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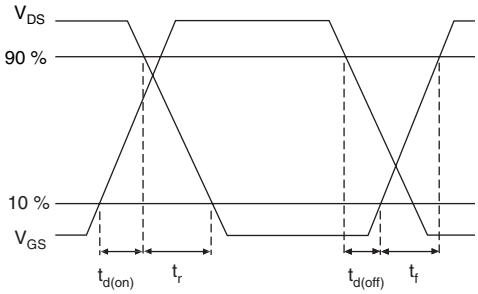

Fig. 10b - Switching Time Waveforms

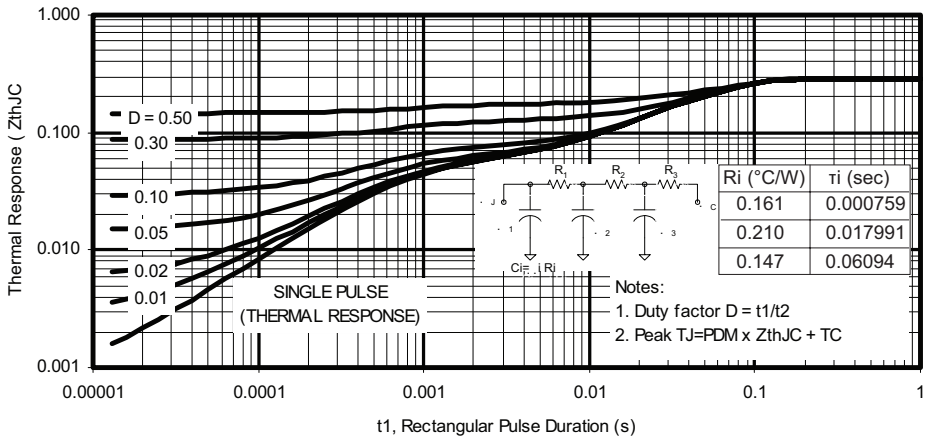

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction to Case

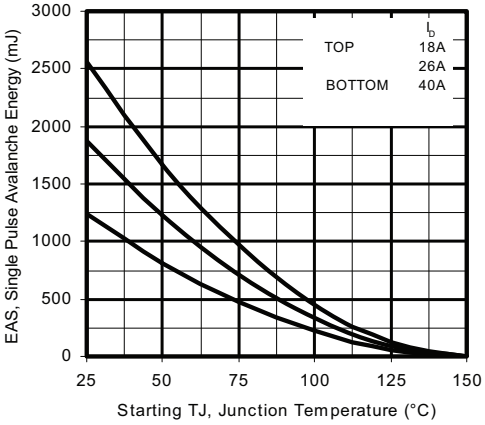

Fig. 12a - Maximum Avalanche Energy vs. Drain Current

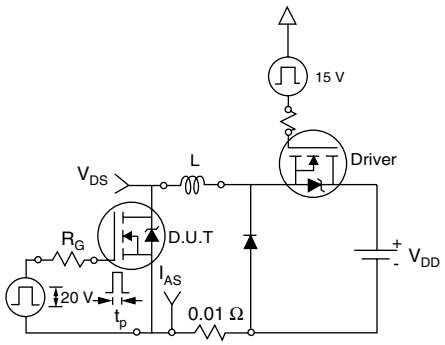

Fig. 12b - Unclamped Inductive Test Circuit

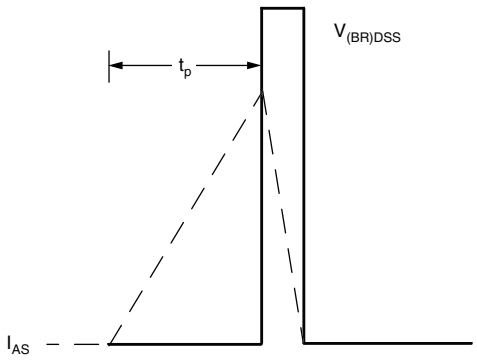

Fig. 12c - Unclamped Inductive Waveforms

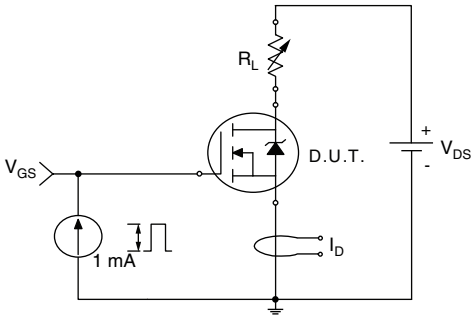

Fig. 13a - Gate Charge Test Circuit

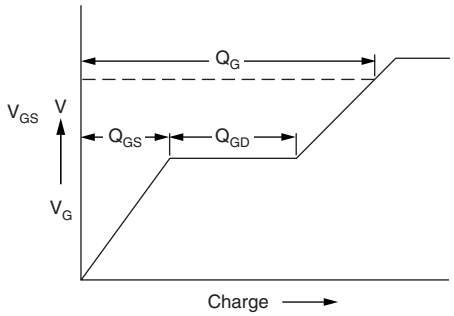

Fig. 13b - Basic Gate Charge Waveform

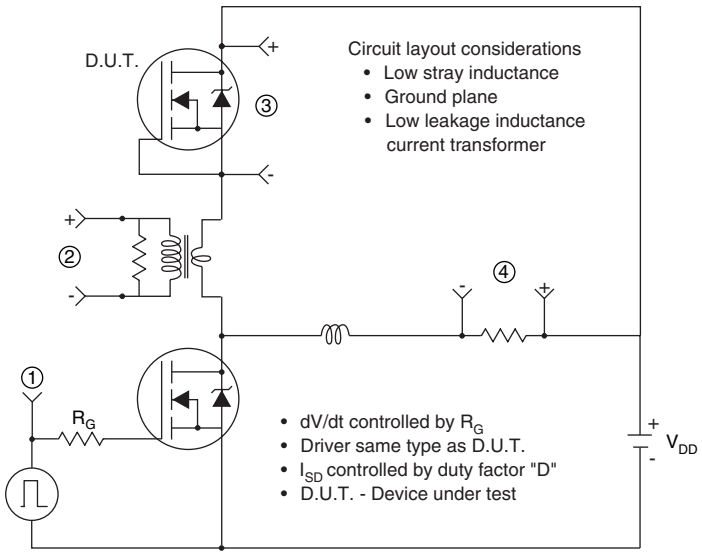

Fig. 13c - Peak Diode Recovery dV/dt Test Circuit

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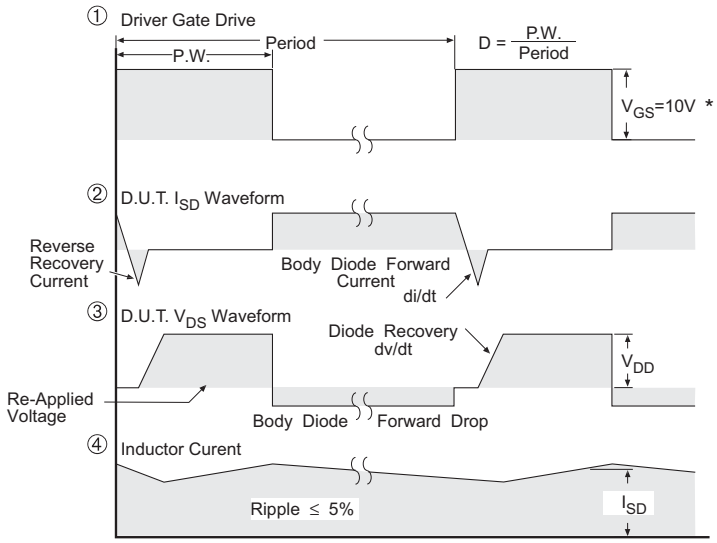


* V_{GS} = 5V for Logic Level Devices

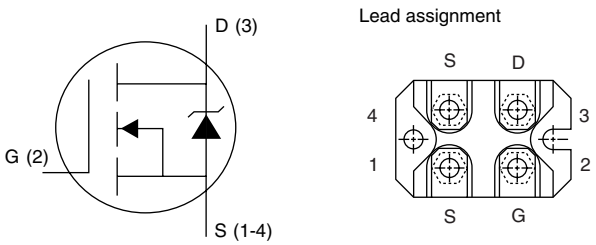
Fig. 14 - For N-Channel Power MOSFETs

ORDERING INFORMATION TABLE

Device code

F	C	40	S	A	50	FK	P
1	2	3	4	5	6	7	8

- 1 - Power MOSFET
- 2 - Generation 6.2/6.3 MOSFET silicon DBC construction
- 3 - Current rating (40 = 40 A)
- 4 - Single switch (see Circuit Configuration table)
- 5 - SOT-227
- 6 - Voltage rating (50 = 500 V)
- 7 - MOSFET K speed
- 8 - • None = Standard production
  • P = Lead (Pb)-free

CIRCUIT CONFIGURATION		
CIRCUIT	**CIRCUIT CONFIGURATION CODE**	**CIRCUIT DRAWING**
Single switch no diode	S	

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95036
Packaging information	www.vishay.com/doc?95037

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