



October 1987
Revised January 1999

CD4029BC Presettable Binary/Decade Up/Down Counter

General Description

The CD4029BC is a presettable up/down counter which counts in either binary or decade mode depending on the voltage level applied at binary/decade input. When binary/decade is at logical "1", the counter counts in binary, otherwise it counts in decade. Similarly, the counter counts up when the up/down input is at logical "1" and vice versa.

A logical "1" preset enable signal allows information at the "jam" inputs to preset the counter to any state asynchronously with the clock. The counter is advanced one count at the positive-going edge of the clock if the carry in and preset enable inputs are at logical "0". Advancement is inhibited when either or both of these two inputs is at logical "1". The carry out signal is normally at logical "1" state and goes to logical "0" state when the counter reaches its

maximum count in the "up" mode or the minimum count in the "down" mode provided the carry input is at logical "0" state.

All inputs are protected against static discharge by diode clamps to both V_{DD} and V_{SS} .

Features

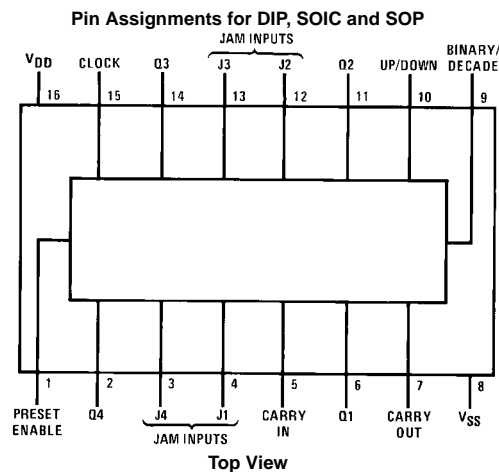
- Wide supply voltage range: 3V to 15V
- High noise immunity: $0.45 V_{DD}$ (typ.)
- Low power TTL compatibility: fan out of 2 driving 74L or 1 driving 74LS
- Parallel jam inputs
- Binary or BCD decade up/down counting

Ordering Code:

Order Number	Package Number	Package Description
CD4029BCWM	M16B	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide body
CD4029BCSJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4029BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

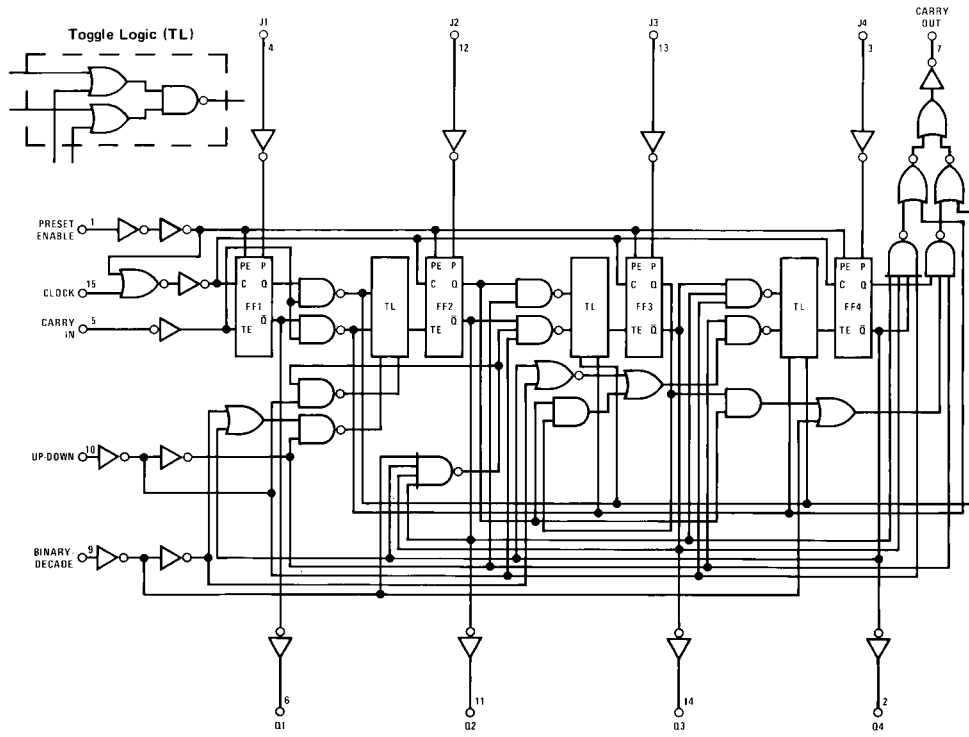
Connection Diagram



CD4029BC Presettable Binary/Decade Up/Down Counter

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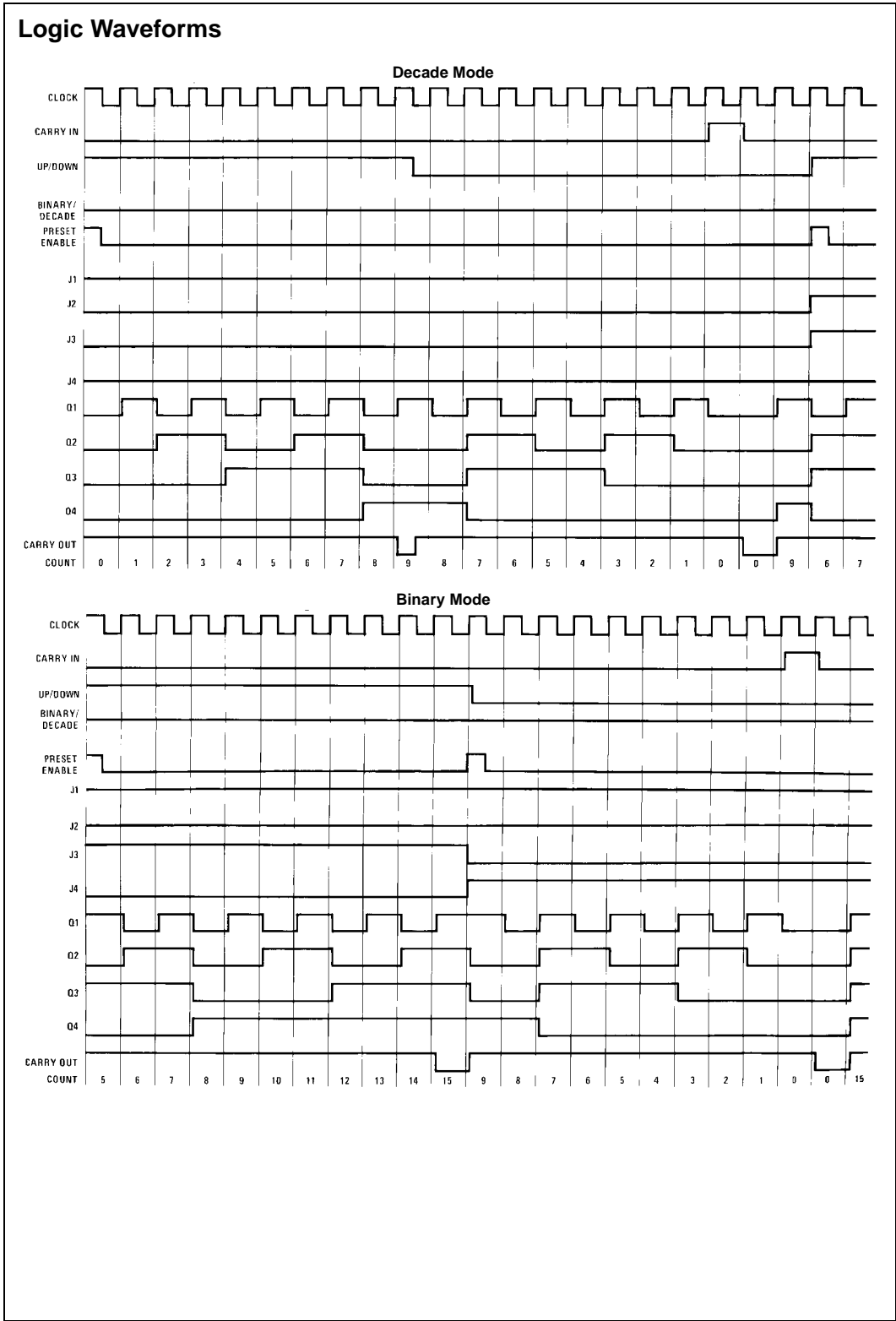
Logic Diagram



Absolute Maximum Ratings (Note 1)			Recommended Operating Conditions (Note 2)							
(Note 2)										
DC Supply Voltage (V_{DD})		-0.5V to +18 V_{DC}	DC Supply Voltage (V_{DD})	3V to 15 V_{DC}						
Input Voltage (V_{IN})		-0.5V to $V_{DD} + 0.5 V_{DC}$	Input Voltage (V_{IN})	0V to $V_{DD} V_{DC}$						
Storage Temperature Range (T_S)		-65°C to +150°C	Operating Temperature Range (T_A)	-40°C to +85°C						
Power Dissipation (P_D)			Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.							
Dual-In-Line		700 mW	Note 2: $V_{SS} = 0V$ unless otherwise specified.							
Small Outline		500 mW								
Lead Temperature (T_L)										
(Soldering, 10 seconds)		260°C								
DC Electrical Characteristics (Note 2)										
Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		20			20		150	μA
		$V_{DD} = 10V$		40			40		300	μA
		$V_{DD} = 15V$		80			80		600	μA
V_{OL}	LOW Level Output Voltage	$ I_O < 1 \mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	HIGH Level Output Voltage	$ I_O < 1 \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	LOW Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V		1.5			1.5		1.5	V
		$V_{DD} = 10V, V_O = 1V$ or 9V		3.0			3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or 13.5V		4.0			4.0		4.0	V
V_{IH}	HIGH Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V	3.5		3.5			3.5		V
		$V_{DD} = 10V, V_O = 1V$ or 9V	7.0		7.0			7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or 13.5V	11.0		11.0			11.0		V
I_{OL}	LOW Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	HIGH Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	-0.52		-0.44	-0.88		-0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	-1.3		-1.1	-2.25		-0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	-3.6		-3.0	-8.8		-2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.3		-10^{-5}	-0.3		-1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA
Note 3: I_{OH} and I_{OL} are tested one output at a time.										

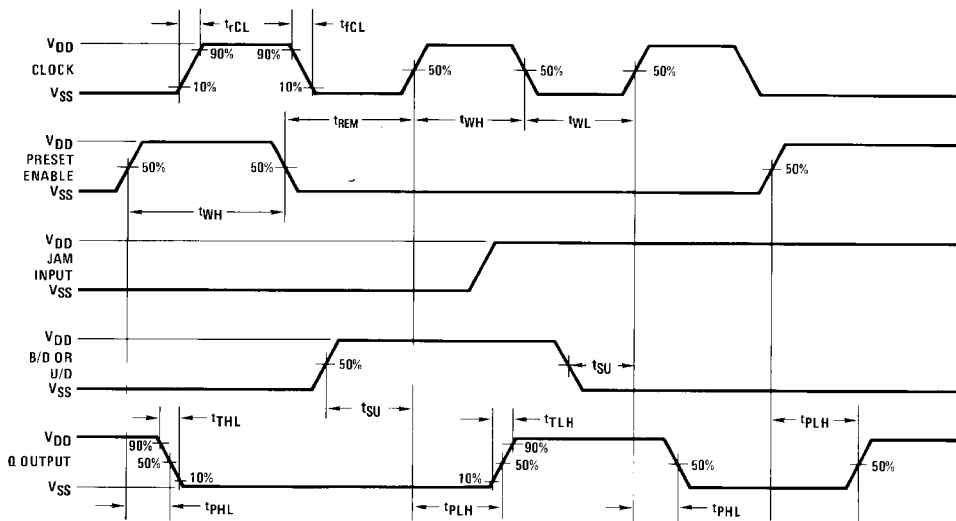
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AC Electrical Characteristics (Note 4)						
T _A = 25°C, C _L = 50 pF, R _L = 200k, Input t _{rCL} = t _{fCL} = 20 ns, unless otherwise specified						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
CLOCKED OPERATION						
t _{PHL} or t _{PLH}	Propagation Delay Time to Q Outputs	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		200 85 70	400 170 140	ns ns ns
t _{PHL} or t _{PLH}	Propagation Delay Time to Carry Output	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		320 135 110	640 270 220	ns ns ns
t _{PHL} or t _{PLH}	Propagation Delay Time to Carry Output	C _L = 15 pF V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		285 120 95	570 240 190	ns ns ns
t _{THL} or t _{TLH}	Transition Time/Q or Carry Output	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		100 50 40	200 100 80	ns ns ns
t _{WH} or t _{WL}	Minimum Clock Pulse Width	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		160 70 55	320 135 110	ns ns ns
t _{rCL} or t _{fCL}	Maximum Clock Rise and Fall Time	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V	15 10 5			μs μs μs
t _{SU}	Minimum Set-Up Time	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		180 70 55	360 140 110	ns ns ns
f _{CL}	Maximum Clock Frequency	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V	1.5 3.7 4.5	3.1 7.4 9		MHz MHz MHz
C _{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C _{PD}	Power Dissipation Capacitance	Per Package (Note 5)		65		pF
PRESET ENABLE OPERATION						
t _{PHL} or t _{PLH}	Propagation Delay Time to Q output	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		285 115 95	570 230 195	ns ns ns
t _{PHL} or t _{PLH}	Propagation Delay Time to Carry Output	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		400 165 135	800 330 260	ns ns ns
t _{WH}	Minimum Preset Enable Pulse Width	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		80 30 25	160 60 50	ns ns ns
t _{REM}	Minimum Preset Enable Removal Time	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		150 60 50	300 120 100	ns ns ns
CARRY INPUT OPERATION						
t _{PHL} or t _{PLH}	Propagation Delay Time to Carry Output	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		265 110 90	530 220 180	ns ns ns
t _{PHL} , t _{PLH}	Propagation Delay Time to Carry Output	C _L = 15 pF V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		200 85 70	400 170 140	ns ns ns
<p>Note 4: *AC Parameters are guaranteed by DC correlated testing.</p> <p>Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 74C Family Characteristics application note, AN-90.</p>						

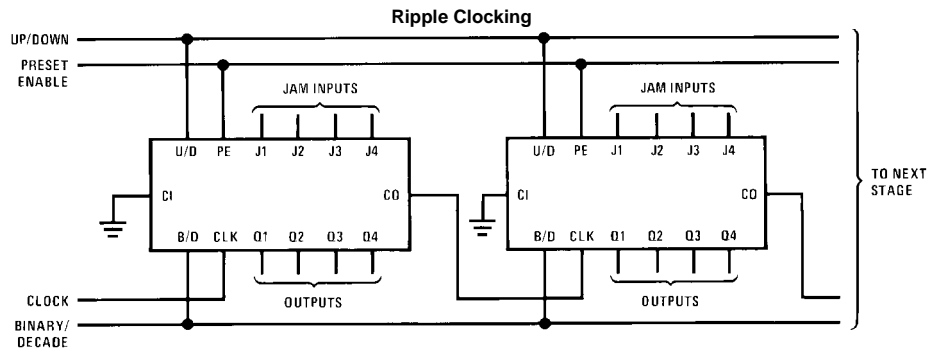
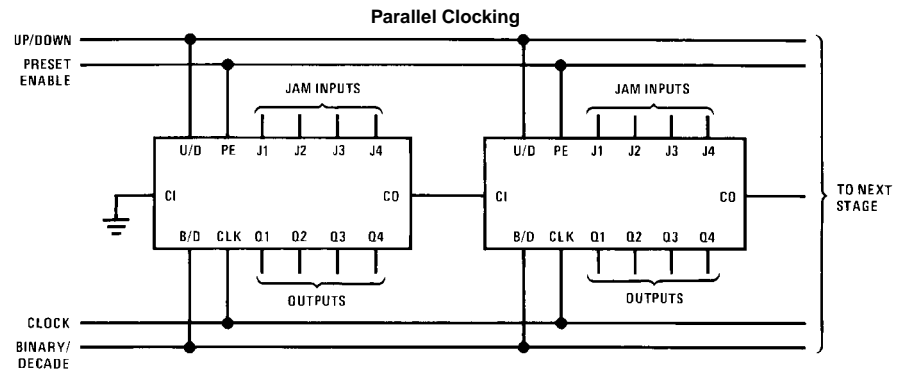


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Switching Time Waveforms

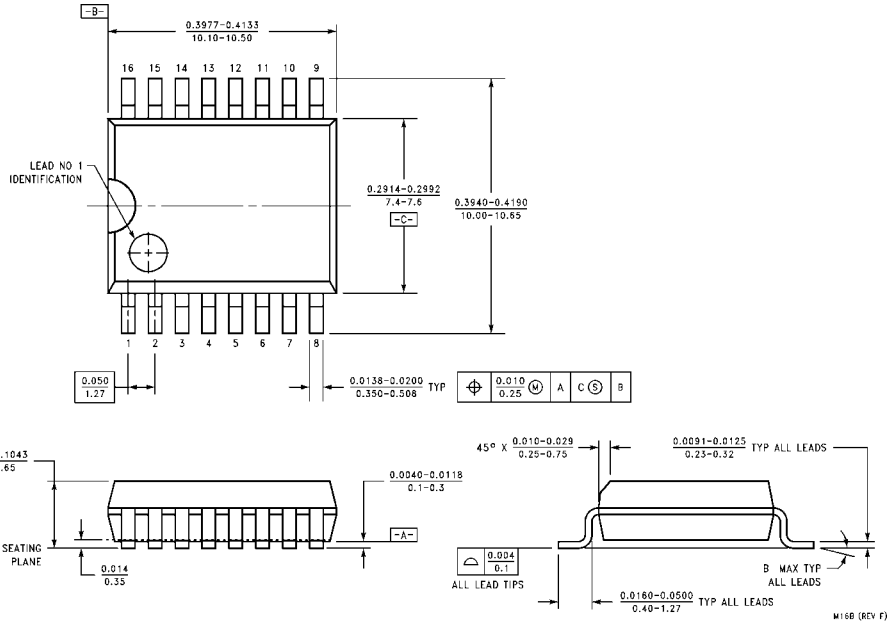


Cascading Packages

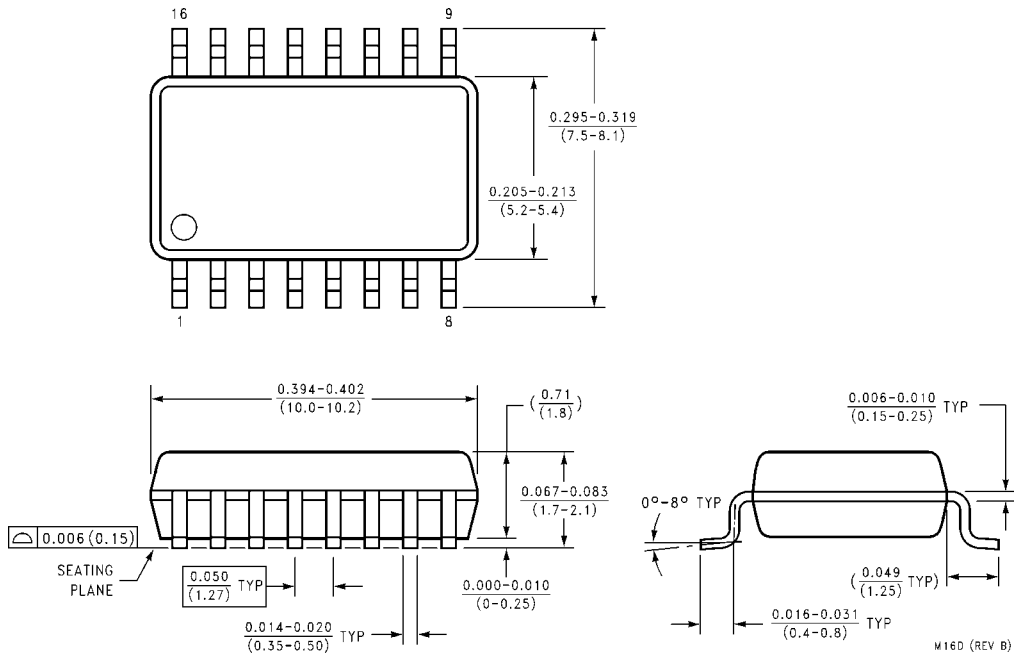


Carry out lines at the 2nd or later stages may have a negative-going spike due to differential internal delays. These spikes do not affect counter operation, but if the carry out is used to trigger external circuitry the carry out should be gated with the clock.

Physical Dimensions inches (millimeters) unless otherwise noted

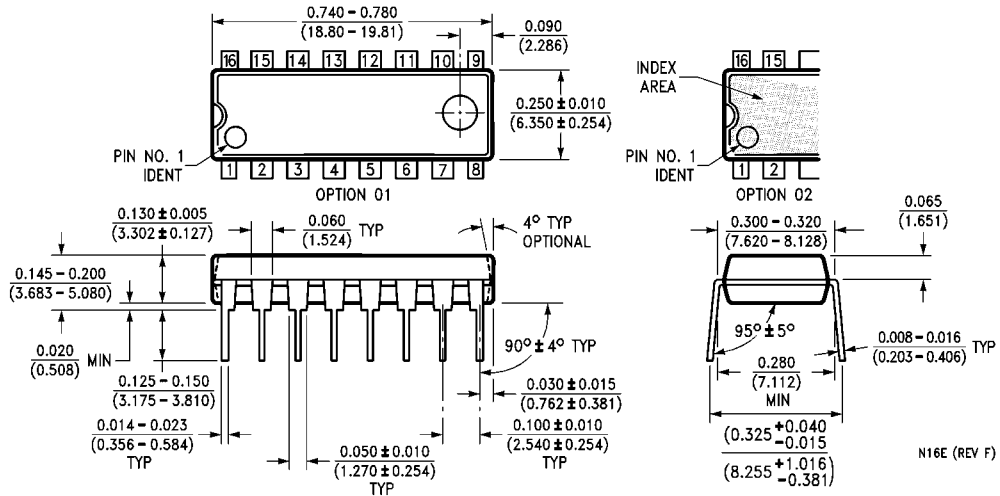


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
Package Number M16B**



**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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