

200 mA Low-Noise, High-PSRR Negative Output Low-Dropout Linear Regulators

Check for Samples: [TPS72325-Q1](#)

FEATURES

- **Ultralow Noise:** $60\mu\text{V}_{\text{RMS}}$ Typical
- **High PSRR:** 65dB Typical at 1kHz
- **Low Dropout Voltage:** 280mV Typical at 200mA, 2.5V
- **Available in –2.5V and Adjustable (–1.2V to –10V) Versions**
- **Stable With a $2.2\mu\text{F}$ Ceramic Output Capacitor**
- **Less Than $2\mu\text{A}$ Typical Quiescent Current in Shutdown Mode**
- **2% Overall Accuracy (Line, Load, Temperature)**
- **Thermal and Over-Current Protection**
- **SOT23-5 (DBV) Package**
- **Operating Junction Temperature Range:** -40°C to $+125^{\circ}\text{C}$

APPLICATIONS

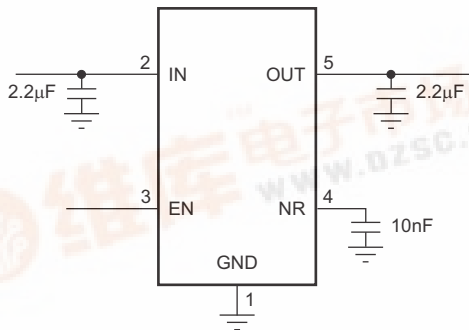
- Optical Drives
- Optical Networking
- Noise Sensitive Circuitry
- GaAs FET Gate Bias
- Video Amplifiers

DESCRIPTION

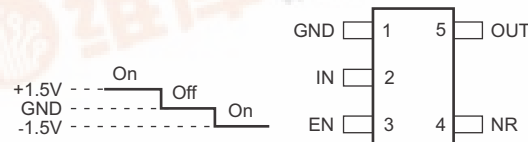
The TPS72325-Q1 low-dropout (LDO) negative voltage regulator offers an ideal combination of features to support low noise applications. This device is capable of operating with input voltages from -10V to -2.7V , and support outputs from -10V to -1.2V . The TPS72325-Q1 regulator is stable with small, low-cost ceramic capacitors, and include enable (EN) and noise reduction (NR) functions. Thermal short-circuit and over-current protections are provided by internal detection and shutdown logic. High PSRR (65dB at 1kHz) and low noise ($60\mu\text{V}_{\text{RMS}}$) make the TPS72325-Q1 ideal for low-noise applications.

The TPS72325-Q1 uses a precision voltage reference to achieve 2% overall accuracy over load, line, and temperature variations. Available in a small SOT23-5 package, the TPS72325-Q1 is fully specified over a temperature range of -40°C to $+125^{\circ}\text{C}$.

Typical Application Circuit



DBV PACKAGE
(TOP VIEW)



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TPS72325-Q1

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 1. ORDERING INFORMATION⁽¹⁾

PRODUCT	V _{OUT} ⁽²⁾
TPS72325QDBVRQ1	nominal output voltage = 2.5V

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Output voltages from –1.2V to –9V in 100mV increments are available. Minimum order quantities apply; contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS^{(1) (2)}

Over operating temperature range, unless otherwise noted.

	VALUE	UNITS
Input voltage range, V _{IN}	–11 to +0.3	V
Noise reduction pin voltage range, V _{NR}	–11 to +5.5	V
Enable voltage range, V _{EN}	–V _{IN} to +5.5	V
Output voltage range, V _{OUT}	–11 to +0.3	V
Output current, I _{OUT}	Internally limited	
Output short-circuit duration	Indefinite	
Continuous total power dissipation, P _D	See Power Dissipation Ratings table	
Junction temperature range, T _J	–55 to +150	°C
Storage temperature range, T _{stg}	–65 to +150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

POWER DISSIPATION RATINGS

BOARD	PACKAGE	R _{θJC}	R _{θJA}	DERATING FACTOR ABOVE T _A = +25°C	T _A ≤ +25°C POWER RATING	T _A = +70°C POWER RATING	T _A = +85°C POWER RATING
Low-K ⁽¹⁾	DBV	64°C/W	255°C/W	3.9mW/°C	390mW	215mW	155mW
High-K ⁽²⁾	DBV	64°C/W	180°C/W	5.6mW/°C	560mW	310mW	225mW

- (1) The JEDEC Low-K (1s) board design used to derive this data was a 3 inch × 3 inch, two-layer board with 2-ounce copper traces on top of the board.
- (2) The JEDEC High-K (2s2p) board design used to derive this data was a 3 inch × 3 inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on the top and bottom of the board.

ELECTRICAL CHARACTERISTICS

Over operating junction temperature range, $V_{IN} = V_{OUT(nom)} - 0.5V$, $I_{OUT} = 1mA$, $V_{EN} = 1.5V$, $C_{OUT} = 2.2\mu F$, and $C_{NR} = 0.01\mu F$, unless otherwise noted. Typical values are at $T_J = +25^\circ C$.

PARAMETER			TEST CONDITIONS	TPS72325-Q1			UNITS
				MIN	TYP	MAX	
V_{IN}	Input voltage range ⁽¹⁾			-10		-2.7	V
V_{FB}	Feedback reference voltage		$T_J = +25^\circ C$	-1.210	-1.186	-1.162	V
V_{OUT}	Accuracy	Nominal	$T_J = +25^\circ C$	-1		1	%
		TPS72325-Q1 vs $V_{IN}/I_{OUT}/T$	$-10V \leq V_{IN} \leq V_{OUT} - 0.5V$, $10\mu A \leq I_{OUT} \leq 200mA$	-2	± 1	2	%
V_{OUT}/V_{IN}	Line regulation		$-10V \leq V_{IN} \leq V_{OUT(nom)} - 0.5V$		0.04		%/V
V_{OUT}/I_{OUT}	Load regulation		$0mA \leq I_{OUT} \leq 200mA$		0.002		%/mA
V_{DO}	Dropout voltage at $V_{OUT} = 0.96 \times V_{OUT(nom)}$		$I_{OUT} = 200mA$		280	500	mV
I_{CL}	Current limit		$V_{OUT} = 0.85 \times V_{OUT(nom)}$	300	550	800	mA
I_{GND}	Ground pin current		$I_{OUT} = 0mA (I_Q)$, $-10V \leq V_{IN} \leq V_{OUT} - 0.5V$		130	200	μA
			$I_{OUT} = 200mA$, $-10V \leq V_{IN} \leq V_{OUT} - 0.5V$		350	500	
I_{SHDN}	Shutdown ground pin current		$-0.4V \leq V_{EN} \leq 0.4V$, $-10V \leq V_{IN} \leq V_{OUT} - 0.5V$		0.1	2.0	μA
I_{FB}	Feedback pin current		$-10V \leq V_{IN} \leq V_{OUT} - 0.5V$		0.05	1.0	μA
PSRR	Power-supply rejection ratio		$I_{OUT} = 200mA$, 1kHz, $C_{IN} = C_{OUT} = 10\mu F$		65		dB
			$I_{OUT} = 200mA$, 10kHz, $C_{IN} = C_{OUT} = 10\mu F$		48		
V_n	Output noise voltage		$C_{OUT} = 10\mu F$, 10Hz to 100kHz, $I_{OUT} = 200mA$		60		μV_{RMS}
t_{STR}	Startup time		$V_{OUT} = -2.5V$, $C_{OUT} = 1\mu F$, $R_L = 25\Omega$		1		ms
$V_{EN(HI)}$	Enable threshold positive			1.5			V
$V_{EN(LO)}$	Enable threshold negative					-1.5	V
$V_{DIS(HI)}$	Disable threshold positive					0.4	V
$V_{DIS(LO)}$	Disable threshold negative			-0.4			V
I_{EN}	Enable pin current		$-10V \leq V_{IN} \leq V_{OUT} - 0.5V$, $-10V \leq V_{EN} \leq \pm 3.5V$		0.1	2.0	μA
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing		+165		$^\circ C$
			Reset, temperature decreasing		+145		
T_J	Operating junction temperature			-40		+125	$^\circ C$

(1) Maximum $V_{IN} = (V_{OUT} - V_{DO})$ or $-2.7V$, whichever is more negative.

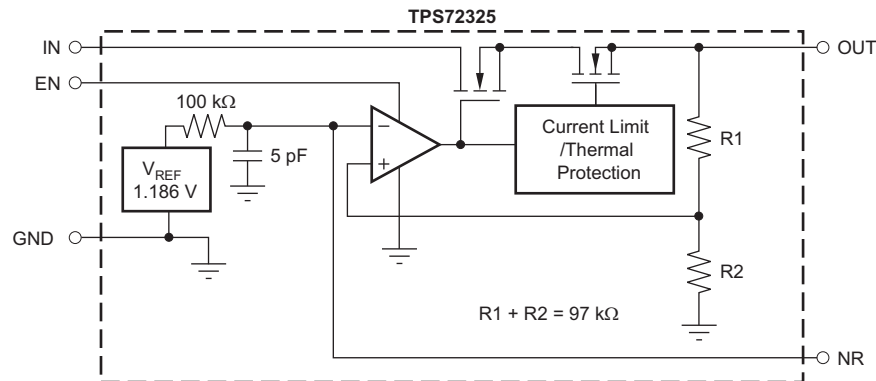
TPS72325-Q1

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FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
GND	1	Ground
IN	2	Input supply
EN	3	Bipolar enable pin. Driving this pin above the positive enable threshold or below the negative enable threshold turns on the regulator. Driving this pin below the positive disable threshold and above the negative disable threshold puts the regulator into shutdown mode.
NR	4	Fixed voltage versions only. Connecting an external capacitor between this pin and ground, bypasses noise generated by the internal bandgap. This configuration allows output noise to be reduced to very low levels.
FB	4	Adjustable voltage version only. This pin is the input to the control loop error amplifier. It is used to set the output voltage of the device.
OUT	5	Regulated output voltage. A small 2.2μF ceramic capacitor is needed from this pin to GND to ensure stability.

TYPICAL CHARACTERISTICS

TPS72325-Q1 at $V_{IN} = V_{OUTnom} - 0.5V$, $I_{OUT} = 1mA$, $V_{EN} = 1.5V$, $C_{OUT} = 2.2\mu F$, and $C_{NR} = 0.01\mu F$, unless otherwise noted.

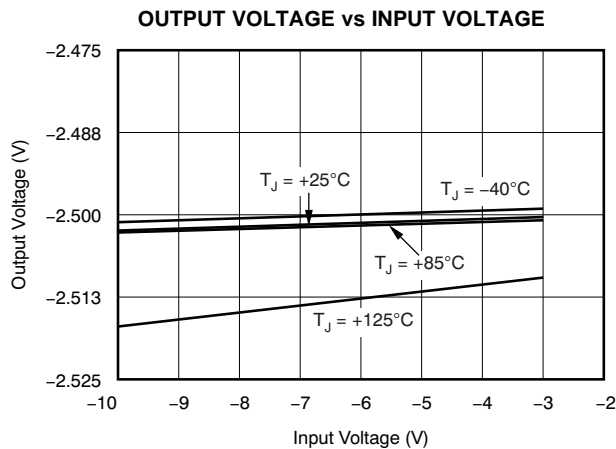


Figure 1.

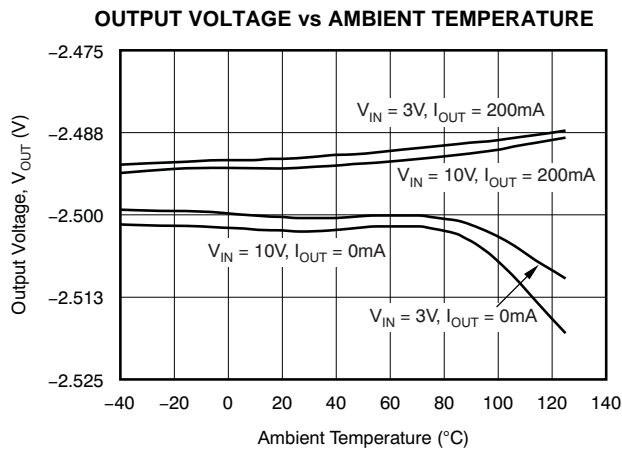


Figure 2.

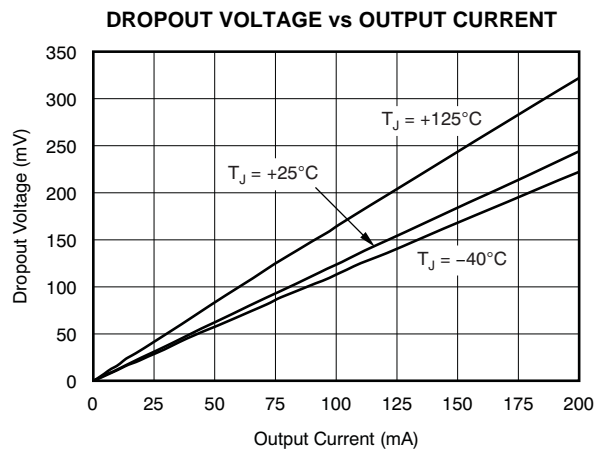


Figure 3.

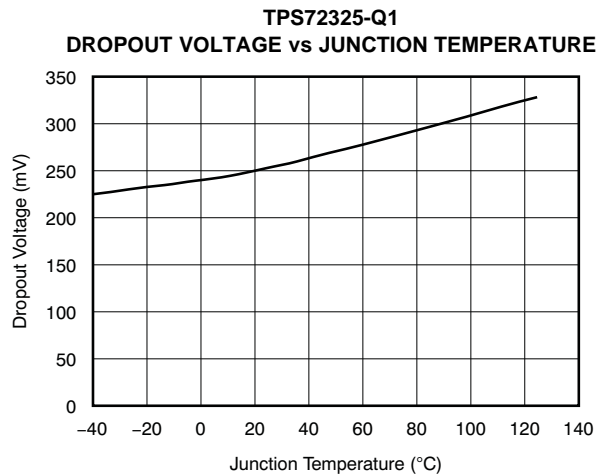


Figure 4.

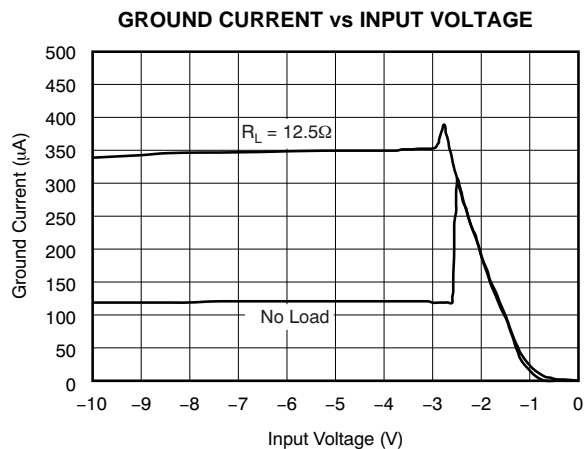


Figure 5.

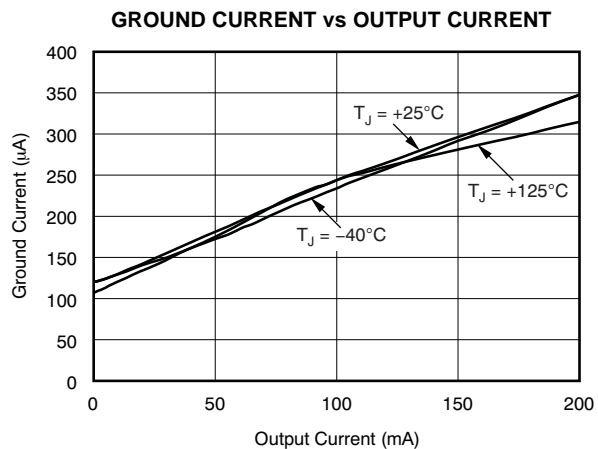


Figure 6.

TYPICAL CHARACTERISTICS (continued)

TPS72325-Q1 at $V_{IN} = V_{OUTnom} - 0.5V$, $I_{OUT} = 1mA$, $V_{EN} = 1.5V$, $C_{OUT} = 2.2\mu F$, and $C_{NR} = 0.01\mu F$, unless otherwise noted.

GROUND CURRENT vs JUNCTION TEMPERATURE

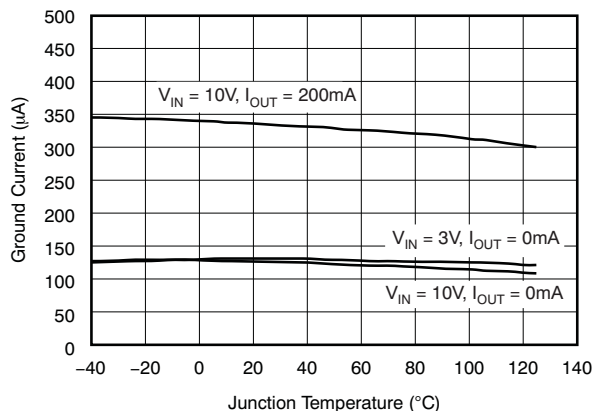


Figure 7.

CURRENT LIMIT vs JUNCTION TEMPERATURE

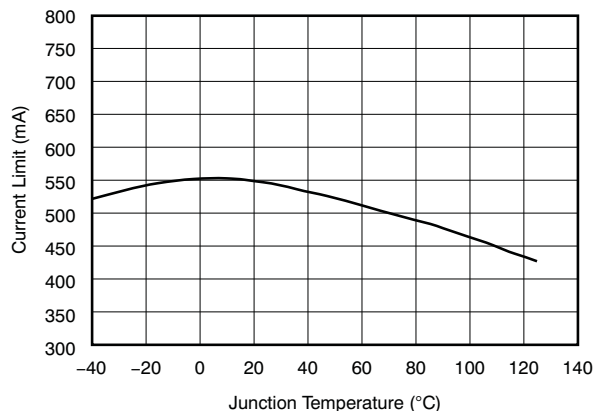


Figure 8.

STANDBY CURRENT vs JUNCTION TEMPERATURE

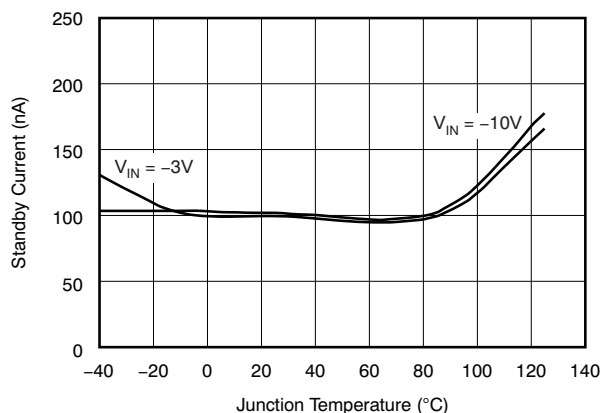


Figure 9.

ENABLE PIN CURRENT vs JUNCTION TEMPERATURE

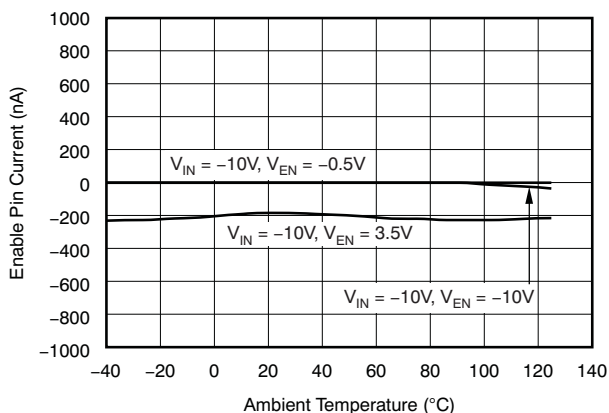


Figure 10.

LINE AND LOAD REGULATION vs JUNCTION TEMPERATURE

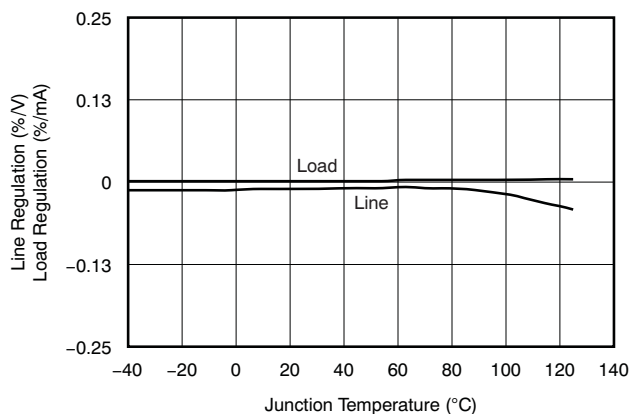


Figure 11.

LINE TRANSIENT RESPONSE

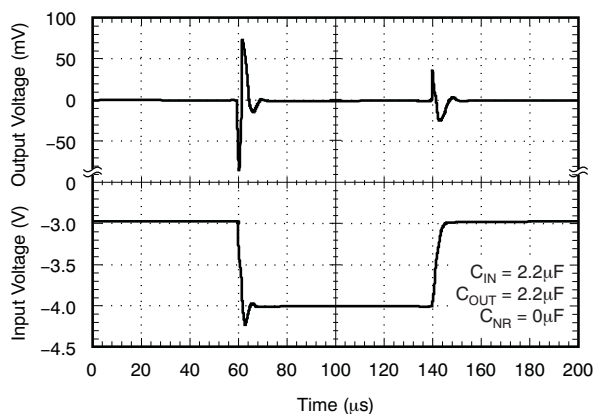


Figure 12.

TYPICAL CHARACTERISTICS (continued)

TPS72325-Q1 at $V_{IN} = V_{OUTnom} - 0.5V$, $I_{OUT} = 1mA$, $V_{EN} = 1.5V$, $C_{OUT} = 2.2\mu F$, and $C_{NR} = 0.01\mu F$, unless otherwise noted.

LOAD TRANSIENT RESPONSE

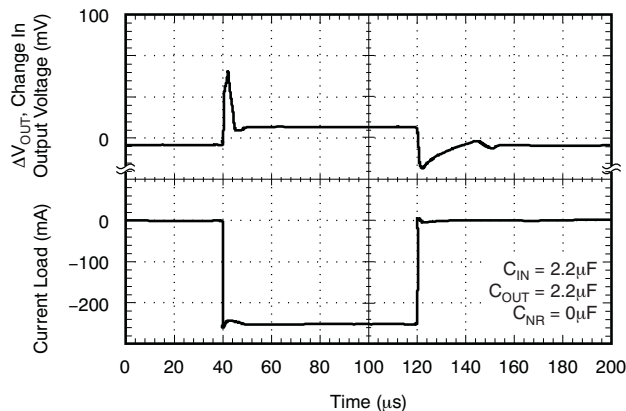


Figure 13.

LOAD TRANSIENT RESPONSE

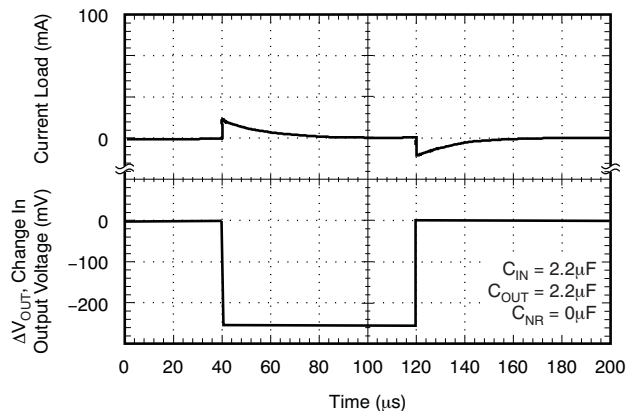


Figure 14.

START-UP RESPONSE

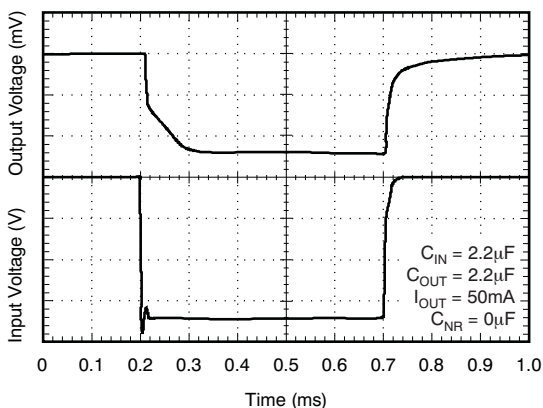


Figure 15.

START-UP RESPONSE

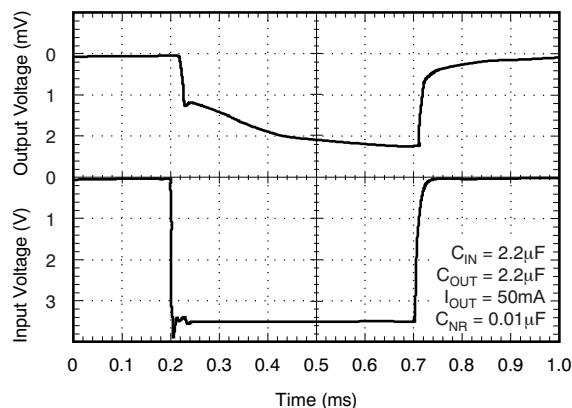


Figure 16.

POWER-UP/POWER-DOWN

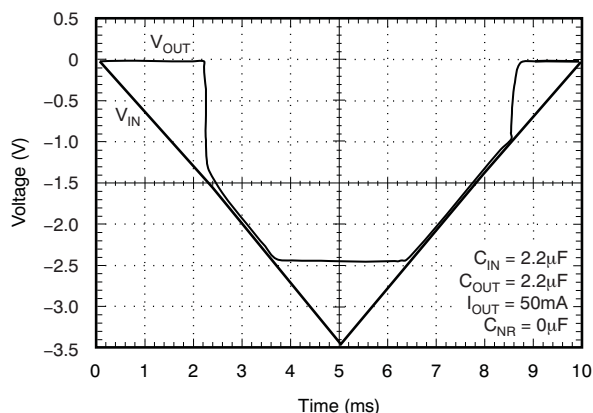


Figure 17.

TOTAL NOISE vs C_{NR}
(10Hz to 100kHz)

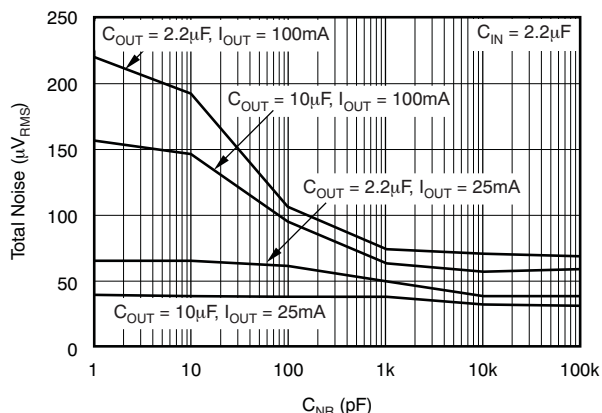


Figure 18.

TPS72325-Q1

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TYPICAL CHARACTERISTICS (continued)

TPS72325-Q1 at $V_{IN} = V_{OUTnom} - 0.5V$, $I_{OUT} = 1mA$, $V_{EN} = 1.5V$, $C_{OUT} = 2.2\mu F$, and $C_{NR} = 0.01\mu F$, unless otherwise noted.

OUTPUT NOISE vs TIME

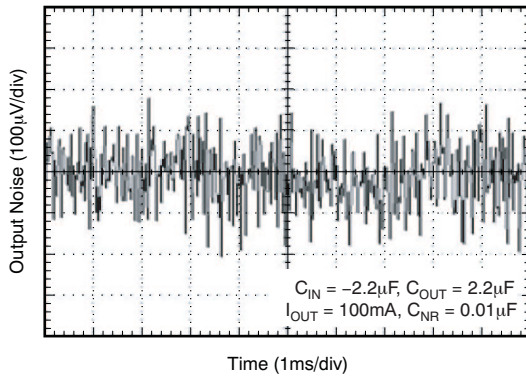


Figure 19.

NOISE SPECTRAL DENSITY vs FREQUENCY

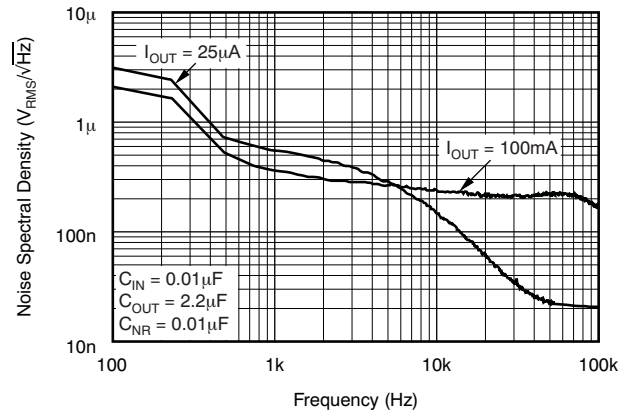


Figure 20.

NOISE SPECTRAL DENSITY vs FREQUENCY

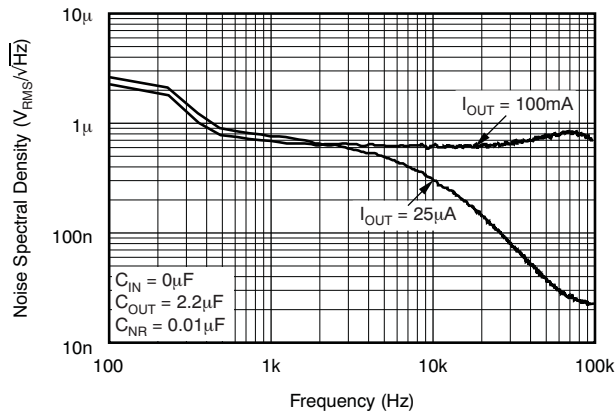


Figure 21.

PSRR vs FREQUENCY

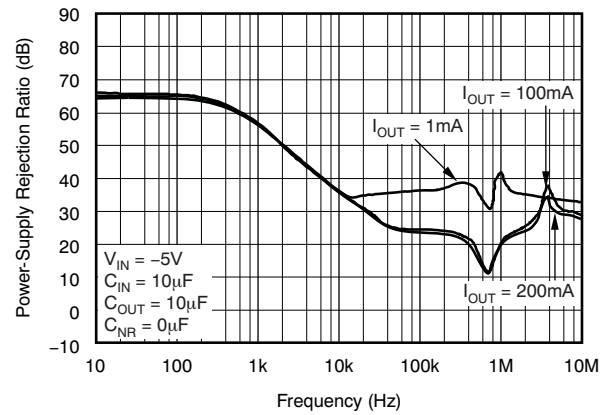


Figure 22.

PSRR vs FREQUENCY

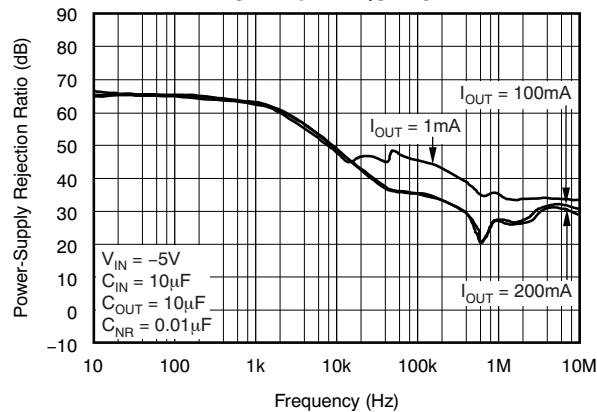


Figure 23.

APPLICATION INFORMATION

DEVICE OPERATION

The TPS72325-Q1 is a low-dropout negative linear voltage regulator with a rated current of 200mA. It is offered in trimmed output voltages between -1.5V and -5.2V and as an adjustable regulator from -1.2V to -10V . It features very low noise and high power-supply rejection ratio (PSRR), making it ideal for high-sensitivity analog and RF applications. A shutdown mode is available, reducing ground current to $2\mu\text{A}$ maximum over temperature and process. The TPS72325-Q1 is offered in a small SOT23 package and is specified over a -40°C to $+125^{\circ}\text{C}$ junction temperature range.

ENABLE

The enable pin is active above $+1.5\text{V}$ and below -1.5V , allowing it to be controlled by a standard TTL signal or by connection to V_i if not used. When driven to GND most internal circuitry is turned off, putting the TPS72325-Q1 into shutdown mode, drawing $2\mu\text{A}$ maximum ground current.

CAPACITOR SELECTION FOR STABILITY

Appropriate input and output capacitors should be used for the intended application. The TPS72325-Q1 only requires a $2.2\mu\text{F}$ ceramic output capacitor to be used for stable operation. Both the capacitor value and ESR affect stability, output noise, PSRR, and transient response. For typical applications, a $2.2\mu\text{F}$ ceramic output capacitor located close to the regulator is sufficient.

OUTPUT NOISE

Without external bypassing, output noise of the TPS72325-Q1 from 10Hz to 100kHz is $200\mu\text{V}_{\text{RMS}}$ typical. The dominant contributor to output noise is the internal bandgap reference. Adding an external $0.01\mu\text{F}$ capacitor to ground reduces noise to $60\mu\text{V}_{\text{RMS}}$. Best noise performance is achieved using appropriate low ESR capacitors for bypassing noise at the NR and OUT pins. See [Figure 18](#) in the [Typical Characteristics](#) section.

POWER-SUPPLY REJECTION

The TPS72325-Q1 offers a very high PSRR for applications with noisy input sources or highly sensitive output supply lines. For best PSRR, use high-quality input and output capacitors.

CURRENT LIMIT

The TPS72325-Q1 has internal circuitry that monitors and limits output current to protect the regulator from damage under all load conditions. When output current reaches the output current limit (550mA typical), protection circuitry turns on, reducing output voltage to ensure that current does not increase. See [Figure 8](#) in the [Typical Characteristics](#) section.

Do not drive the output more than 0.3V above the input. Doing so will bias the body diode in the pass FET, allowing current to flow from the output to the input. This current is not limited by the device. If this condition is expected, care should be taken to externally limit the reverse current.

THERMAL PROTECTION

As protection from damage due to excessive junction temperatures, the TPS72325-Q1 has internal protection circuitry. When junction temperature reaches approximately $+165^{\circ}\text{C}$, the output device is turned off. After the device has cooled by about 20°C , the output device is enabled, allowing normal operation. For reliable operation, design is for worst-case junction temperature of $\leq +125^{\circ}\text{C}$ taking into account worst-case ambient temperature and load conditions.



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PACKAG

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak
TPS72325QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com> for more information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in high temperature applications.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die attach between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (RoHS). All green components must pass the IEC 60755-2-2 test method.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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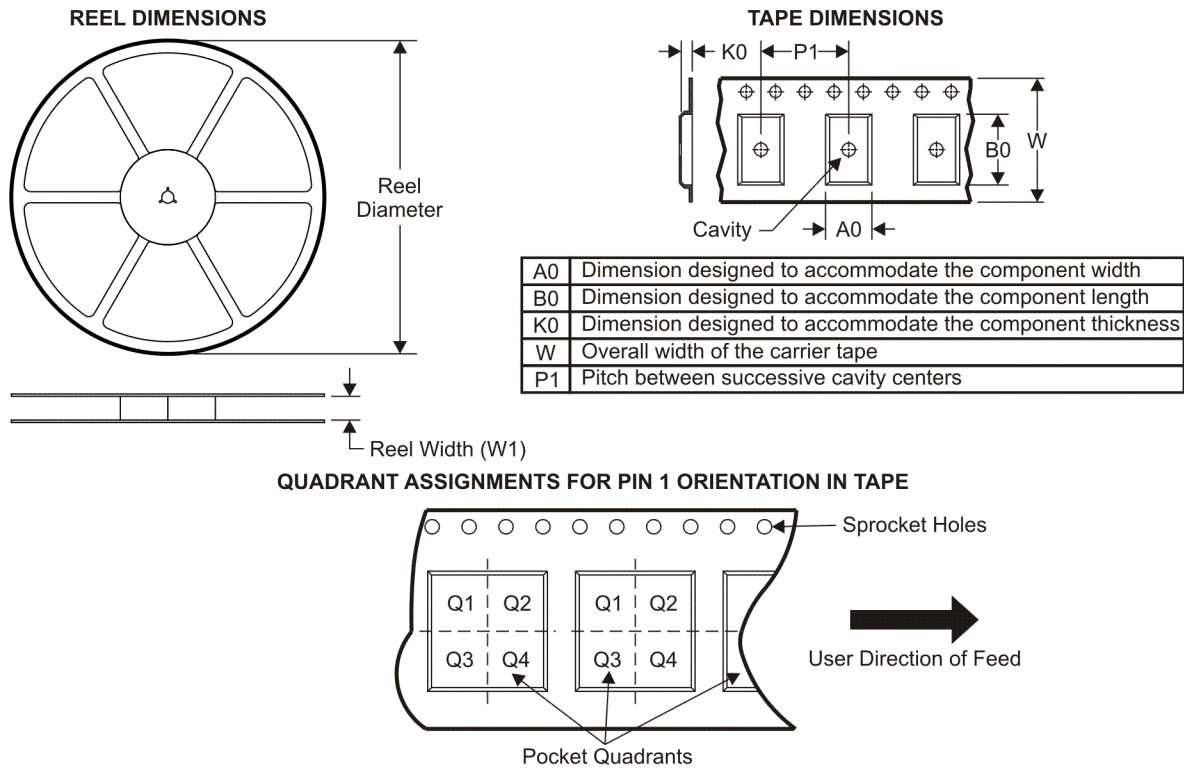
OTHER QUALIFIED VERSIONS OF TPS72325-Q1 :

- Catalog: [TPS72325](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS72325QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

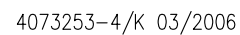
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS72325QDBVRQ1	SOT-23	DBV	5	3000	203.0	203.0	35.0

PLASTIC SMALL-OUTLINE PACKAGE



A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

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