NCP349

Positive Overvoltage Protection Controller with Internal Low R_{ON} NMOS FET

The NCP349 is able to disconnect the systems from its output pin in case wrong input operating conditions are detected. The system is positive overvoltage protected up to +28 V.

Due to this device using internal NMOS, no external device is necessary, reducing the system cost and the PCB area of the application board.

The NCP349 is able to instantaneously disconnect the output from the input, due to integrated Low R_{ON} Power NMOS (65 mΩ), if the input voltage exceeds the overvoltage threshold (OVLO) or undervoltage threshold (UVLO).

At powerup ($\overline{EN}$ pin = low level), the V_{out} turns on t_{on} time after the V_{in} exceeds the undervoltage threshold.

The NCP349 provides a negative going flag ($\overline{FLAG}$) output, which alerts the system that a fault has occurred.

In addition, the device has ESD−protected input (15 kV Air) when bypassed with a 1.0 μF or larger capacitor.

Features

- Overvoltage Protection up to 28 V
- On−Chip Low $R_{DS(on)}$ NMOS Transistor: 65 mΩ
- Internal Charge Pump
- Overvoltage Lockout (OVLO)
- Undervoltage Lockout (UVLO)
- Soft−Start
- Alert $\overline{FLAG}$ Output
- Shutdown $\overline{EN}$ Input
- Compliance to IEC61000−4−2 (Level 4)
  - 8.0 kV (Contact)
  - 15 kV (Air)
- ESD Ratings: Machine Model = B
  Human Body Model = 3
- DFN6 1.6x2 mm Package
- This is a Pb−Free Device

Applications

- Cell Phones
- Camera Phones
- Digital Still Cameras
- Personal Digital Applications
- MP3 Players

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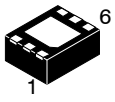
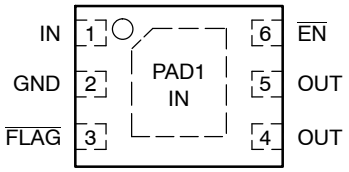


DFN6
MN SUFFIX
CASE 506BM

MARKING DIAGRAM

XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 11 of this data sheet.

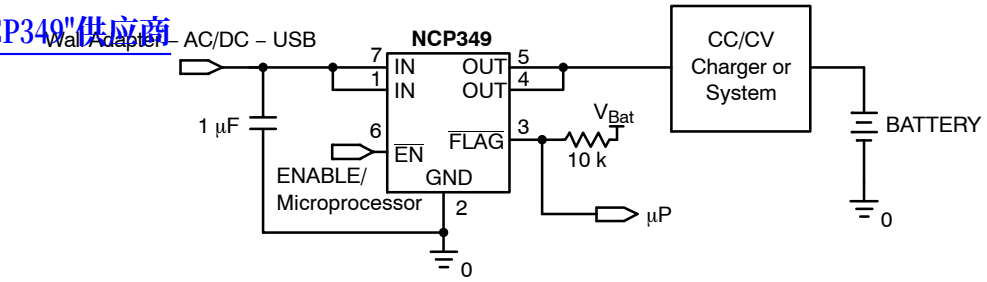


Figure 1. Typical Application Circuit

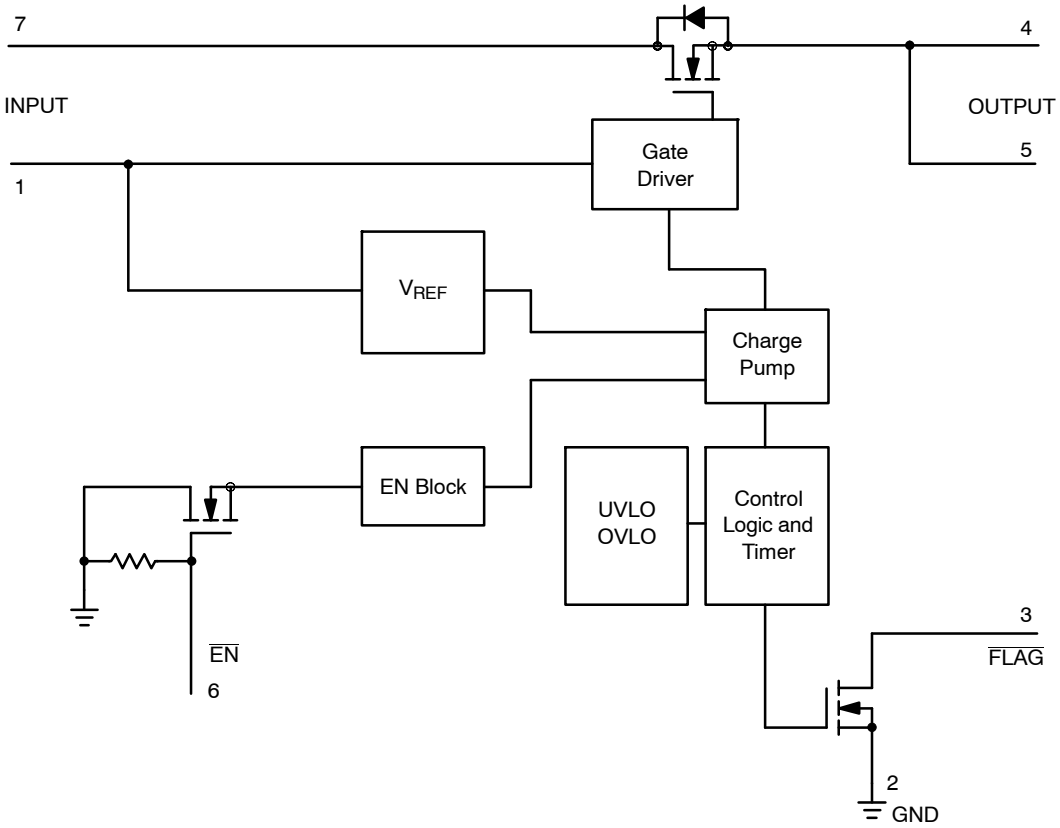


Figure 2. Functional Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Function	Description
1, 7	IN	INPUT	Input Voltage Pins. These pins are connected to the Wall Adapoter (AC−DC, Vbus ..). A 1 μF low ESR ceramic capacitor, or larger, must be connected between these pins and GND, as close as possible to the DUT. The two IN pins must be connected together to power supply. (See PCB recommendation for the pin7).
2	GND	POWER	Ground
3	$\overline{\text{FLAG}}$	OUTPUT	Fault Indication Pin. This pin allows an external system to detect a fault on the IN pins. The $\overline{\text{FLAG}}$ pin goes low when input voltage exceeds OVLO threshold or drops below UVLO threshold. Since the $\overline{\text{FLAG}}$ pin is open drain functionality, an external pull−up resistor to V_{CC} must be added. (Minimum 10 kΩ).
4, 5	OUT	OUTPUT	Output Voltage Pins. These pins follow IN pins when “no fault” is detected. The two OUT pins must be hardwired together.
6	$\overline{\text{EN}}$	INPUT	Enable Pin. The device enters in shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the input. To allow normal functionality, the $\overline{\text{EN}}$ pin shall be connected to GND to a pull down or to a I/O pin. This pin does not have an impact on the fault detection.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Minimum Voltage (IN to GND)	$Vmin_{in}$	−0.3	V
Minimum Voltage (All others to GND)	Vmin	−0.3	V
Maximum Voltage (IN to GND)	$Vmax_{in}$	30	V
Maximum Voltage (All others to GND)	Vmax	7.0	V
Maximum Current (UVLO<V_{IN}<OVLO)	Imax	2.0	A
Thermal Resistance, Junction−to−Air (Note 1)	$R_{\theta JA}$	180	°C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Operating Temperature	T_J	150	°C
ESD Withstand Voltage (IEC 61000−4−2) (input only) when bypassed with 1.0 μF capacitor Human Body Model (HBM), Model = 2 (Note 2) Machine Model (MM) Model = B (Note 3)	Vesd	15 Air, 8.0 Contact 2000 200	kV V V
Moisture Sensitivity	MSL	Level 1	−

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The $R_{\theta JA}$ is highly dependent on the PCB heat sink area (connected to pin 7).
2. Human Body Model, 100 pF discharged through a 1.5 kΩ resistor following specification JESD22/A114.
3. Machine Model, 200 pF discharged through all pins following specification JESD22/A115.

ELECTRICAL CHARACTERISTICS (Min/Max limits values (−40°C < T_A < +85°C) and V_{in} = +5.0 V. Typical values are T_A = +25°C, unless otherwise noted.)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{in}	–	1.2	–	28	V
Undervoltage Lockout Threshold (Note 4)	UVLO	V_{in} falls down UVLO threshold from 5 V to 2.7 V	2.8	2.95	3.1	V
Undervoltage Lockout Hysteresis	$UVLO_{hyst}$	V_{in} rises up UVLO + $UVLO_{hyst}$	30	60	90	mV
Overvoltage Lockout Threshold (Note 4) NCP349MNAE	OVLO	V_{in} rises up OVLO threshold	5.53	5.68	5.83	V
Overvoltage Lockout Hysteresis NCP349MNAE	$OVLO_{hyst}$	V_{in} falls down OVLO + $OVLO_{hyst}$	30	60	90	mV
V_{in} versus V_{out} Resistance	$R_{DS(on)}$	V_{in} = 5.0 V, $\overline{EN}$ = GND, Load connected to V_{out}	–	65	110	mΩ
Supply Quiescent Current	Idd	No load. $\overline{EN}$ = 5.0 V	–	70	150	μA
		No load. $\overline{EN}$ = Gnd	–	140	250	μA
UVLO Supply Current	Idd_{uvlo}	V_{IN} = 2.7 V	–	60	–	μA
$\overline{FLAG}$ Output Low Voltage	Vol_{flag}	1.2 V < V_{IN} < UVLO Sink 50 μA on $\overline{FLAG}$ pin	–	20	400	mV
		V_{IN} > OVLO Sink 1.0 mA on $\overline{FLAG}$ pin	–	–	400	mV
$\overline{FLAG}$ Leakage Current	$\overline{FLAG}_{leak}$	$\overline{FLAG}$ level = 5.0 V	–	1.0	–	nA
$\overline{EN}$ Voltage High	Vih	–	1.2	–	–	V
$\overline{EN}$ Voltage Low	Vol	–	–	–	0.4	V
$\overline{EN}$ Leakage Current	$\overline{EN}_{leak}$	$\overline{EN}$ = 5.0 V or GND	–	1.0	–	nA
TIMINGS						
Startup Delay NCP349MNAE	ton	From V_{in} > UVLO to V_{out} = 0.3 V (See Figures 3 & 7)	6.0	10	14	ms
$\overline{FLAG}$ Going Up Delay NCP349MNAE	tstart	From V_{out} = 0.3 V to FLAG = 1.2 V (See Figures 3 & 9)	6.0	10	14	ms
Output Turn Off Time	toff	From V_{in} > OVLO to V_{out} < = 0.3 V (See Figures 4 & 8) V_{in} increasing from 5.0 V to 8.0 V at 3.0 V/μs Rload connected on V_{out}	–	1.5	5.0	μs
Alert Delay	tstop	From V_{in} > OVLO to $\overline{FLAG}$ < = 0.4 V (See Figures 4 & 10) V_{in} increasing from 5.0 V to 8.0 V at 3.0 V/μs Rload connected on V_{out}	–	1.0	–	μs
Disable Time	tdis	From $\overline{EN}$ > = 1.2 V to V_{out} < 0.3 V Rload = 5.0 Ω (See Figures 5 & 12)	–	1.0	5.0	μs

NOTE: Electrical parameters are guaranteed by correlation across the full range of temperature.

4. Additional UVLO and OVLO thresholds ranging from UVLO and from OVLO can be manufactured. Contact your ON Semiconductor representative for availability.

TIMING DIAGRAMS

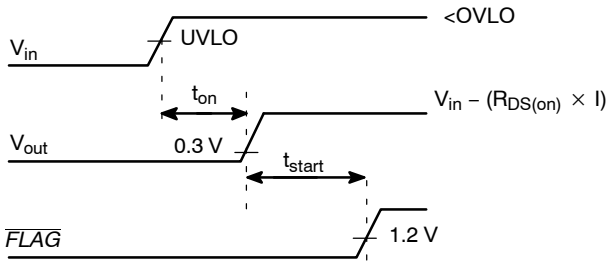


Figure 3. Startup

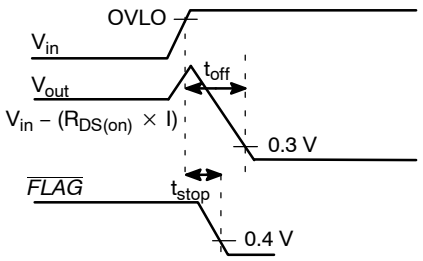


Figure 4. Shutdown on Overvoltage Detection

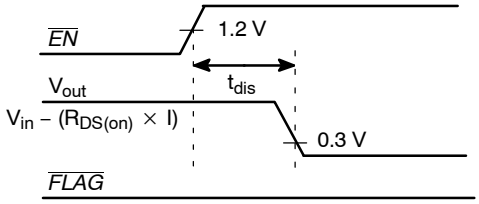


Figure 5. Disable on $\overline{EN}$ = 1

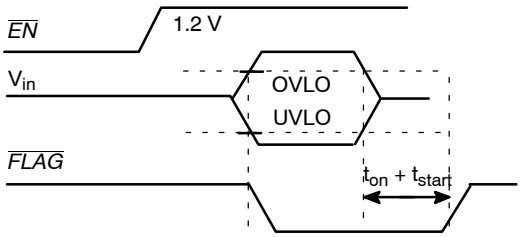


Figure 6. $\overline{FLAG}$ Response with $\overline{EN}$ = 1

TYPICAL OPERATING CHARACTERISTICS

50 ms t_{on} and t_{start} version

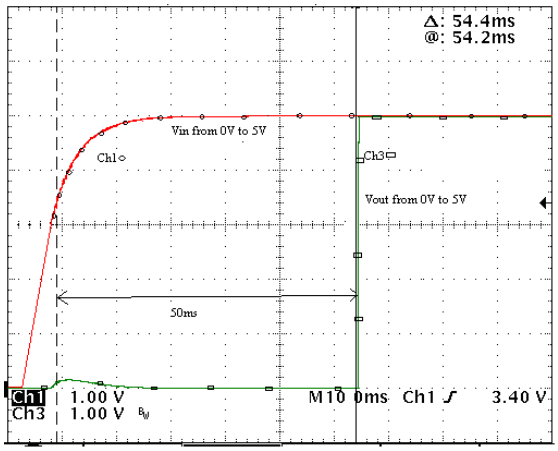


Figure 7. Startup
V_{in} = Ch1, V_{out} = Ch3

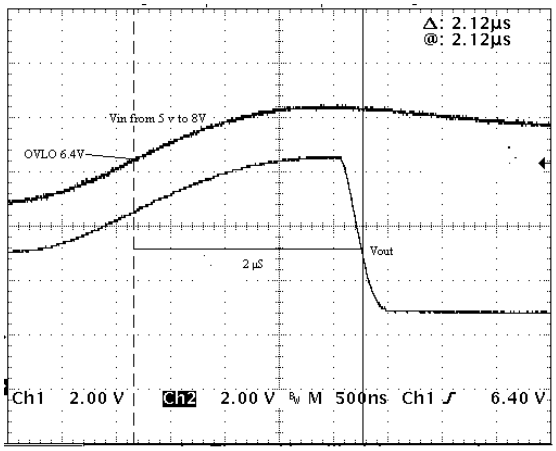


Figure 8. Output Turn Off Time
V_{in} = Ch1, V_{out} = Ch2

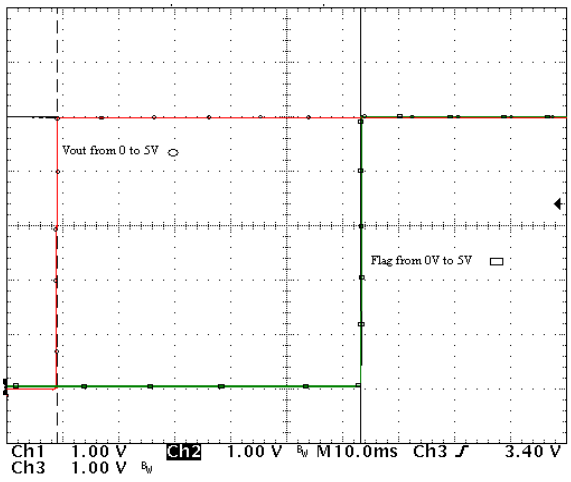


Figure 9. FLAG Going Up Delay
V_{out} = Ch3, FLAG = Ch2

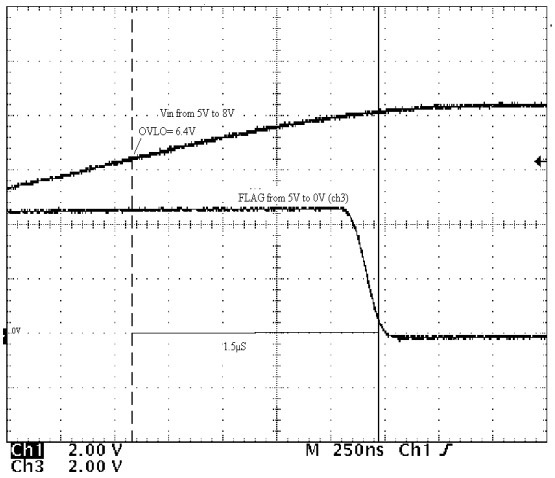


Figure 10. Alert Delay
V_{out} = Ch1, FLAG = Ch3

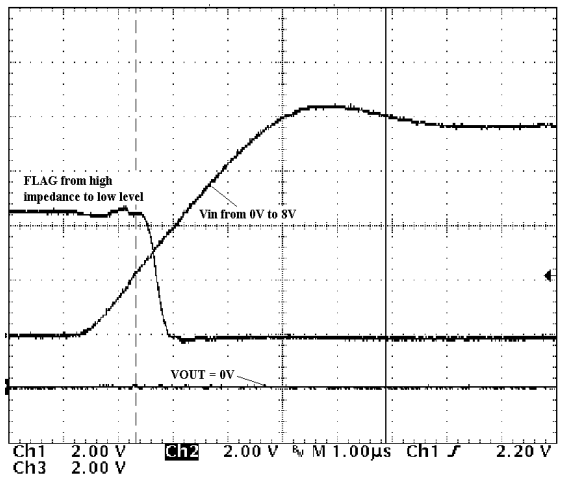


Figure 11. Initial Overvoltage Delay
V_{in} = Ch1, V_{out} = Ch2, FLAG = Ch3

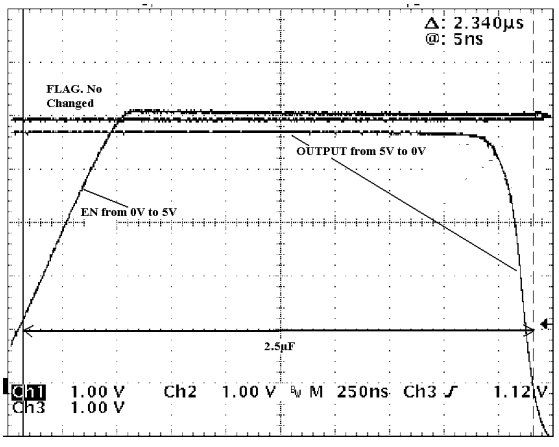


Figure 12. Disable Time
EN = Ch1, V_{out} = Ch2, FLAG = Ch3

TYPICAL OPERATING CHARACTERISTICS

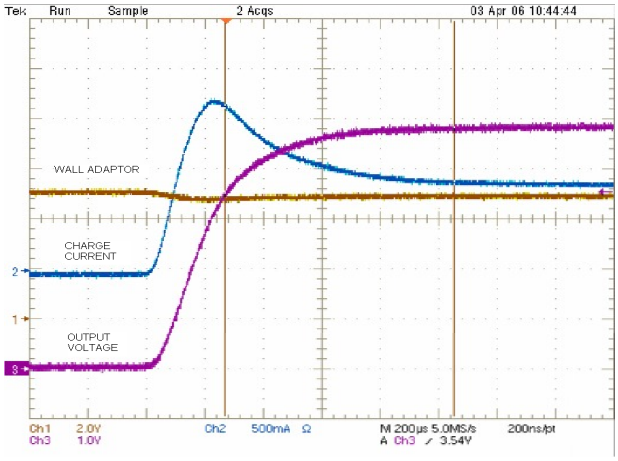


Figure 13. Inrush Current with C_{out} = 100 µF, I charge = 1 A, Output Wall Adaptor Inductance 1 µH

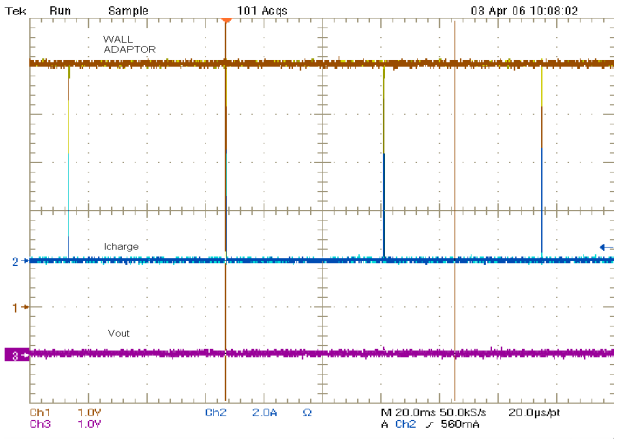


Figure 14. Output Short Circuit

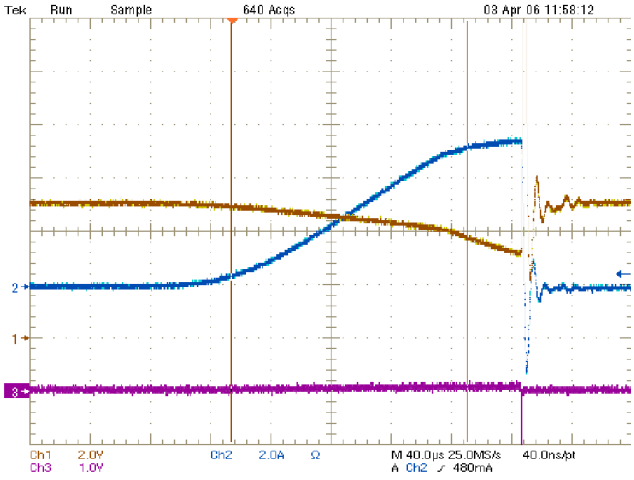


Figure 15. Output Short Circuit (Zoom Fig. 14)

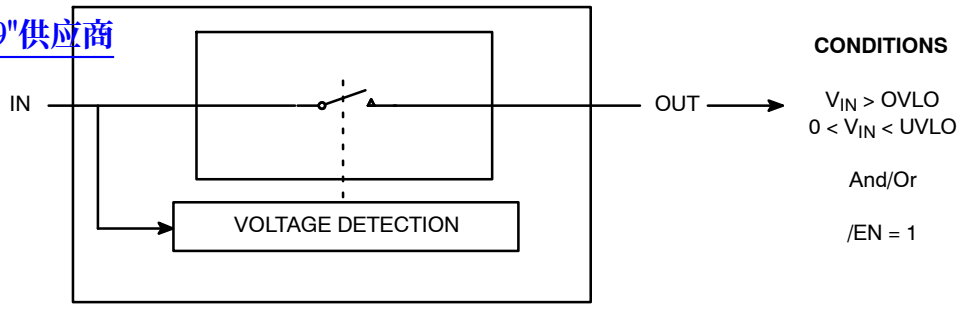


Figure 16. Simplified Diagram

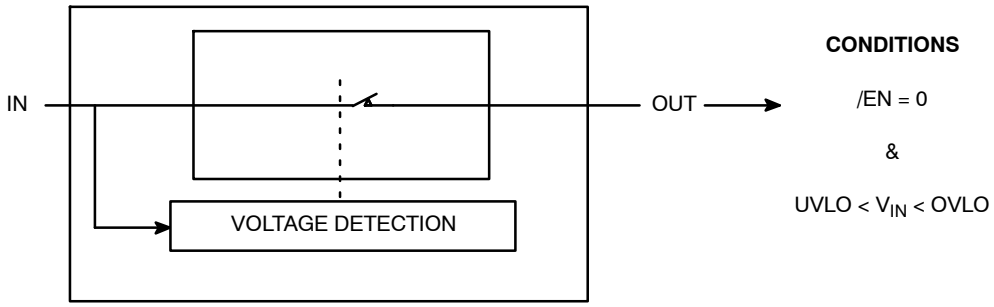


Figure 17. Simplified Diagram

Operation

The NCP349 provides overvoltage protection for positive voltage, up to 28 V. A low $R_{DS(on)}$ NMOSFET protects the systems (i.e.: charger) connected on the Vout pin, against positive overvoltage. At powerup, with $\overline{EN}$ pin = low, the output is rising up t_{on} soft−start after the input overtaking undervoltage UVLO (Figure 3). The NCP349 provides a $\overline{FLAG}$ output, which alerts the system that a fault has occurred. A t_{start} additional delay, regarding available output (Figure 3) is added between output signal rising up and to $\overline{FLAG}$ signal rising up. $\overline{FLAG}$ pin is an open drain output.

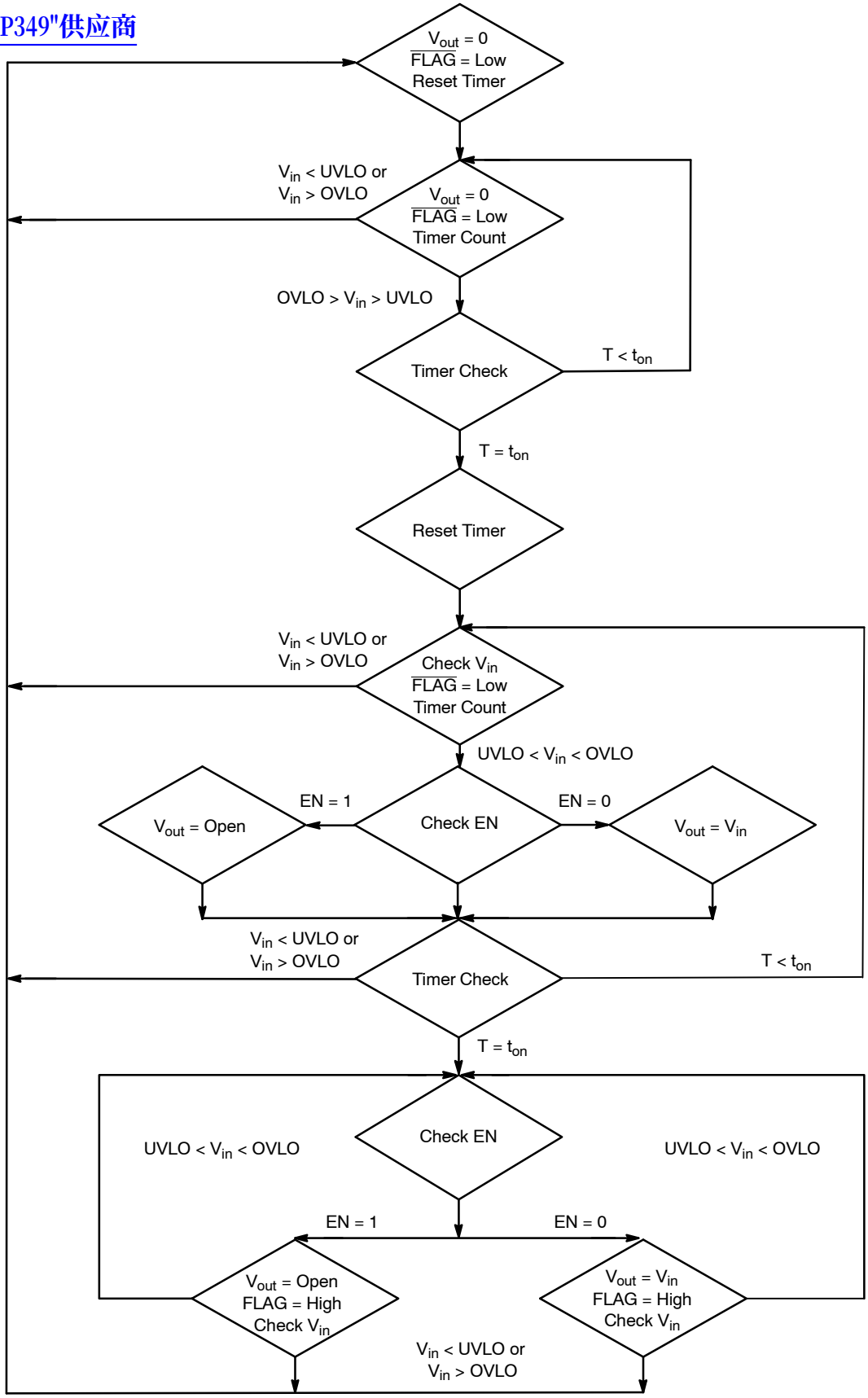


Figure 18. State Machine

Undervoltage Lockout (UVLO)

To ensure proper operation under any conditions, the device has a built−in undervoltage lockout (UVLO) circuit. During V_{in} positive going slope, the output remains disconnected from input until V_{in} voltage is below UVLO, plus hysteresis, nominal. The *FLAG* output is tied to low as long as V_{in} does not reach UVLO threshold. This circuit has a built−in hysteresis to provide noise immunity to transient condition. Additional UVLO thresholds ranging from UVLO can be manufactured. Contact your ON Semiconductor representative for availability.

Overvoltage Lockout (OVLO)

To protect connected systems on V_{out} pin from overvoltage, the device has a built−in overvoltage lockout (OVLO) circuit. During overvoltage condition, the output remains disabled as long as the input voltage exceeds typical OVLO. Additional OVLO thresholds ranging from OVLO can be manufactured. Contact your ON Semiconductor representative for availability.

FLAG output is tied to low until V_{in} is higher than OVLO. This circuit has a built−in hysteresis to provide noise immunity to transient conditions.

FLAG Output

The NCP349 provides a FLAG output, which alerts external systems that a fault has occurred.

This pin is tied to low as soon the OVLO threshold is exceeded or when the V_{in} level is below the UVLO threshold. When V_{in} level recovers normal condition, FLAG is held high, keeping in mind that an additional t_{start} delay has been added between available output and FLAG = high. The pin is an open drain output, thus a pull up resistor (typically 1 MΩ, minimum 10 kΩ) must be added to V_{bat}. Minimum V_{bat} supply must be 2.5 V. The FLAG level will always reflects V_{in} status, even if the device is turned off ($\overline{EN}$ = 1).

EN Input

To enable normal operation, the *EN* pin shall be forced to low or connected to ground. A high level on the pin, disconnects OUT pin from IN pin. *EN* does not overdrive an OVLO or UVLO fault.

Internal NMOS FET

The NCP349 includes an internal Low $R_{DS(on)}$ NMOS FET to protect the systems, connected on OUT pin, from positive overvoltage. Regarding electrical characteristics, the $R_{DS(on)}$, during normal operation, will create low losses on V_{out} pin.

As example: R_{load} = 8.0 Ω, V_{in} = 5.0 V
Typical $R_{DS(on)}$ = 65 mΩ, I_{out} = 618 mA

V_{out} = 8 x 0.618 = 4.95 V

NMOS losses = $R_{DS(on)}$ x $Iout^2$ = 0.065 x 0.618^2 = 25 mW

ESD Tests

The NCP349 input pin fully supports the IEC61000−4−2. 1.0 μF (minimum) must be connected between V_{in} and GND, close to the device.

That means, in Air condition, V_{in} has a ±15 kV ESD protected input. In Contact condition, V_{in} has ±8.0 kV ESD protected input.

Please refer to Figure 19 to see the IEC 61000−4−2 electrostatic discharge waveform.

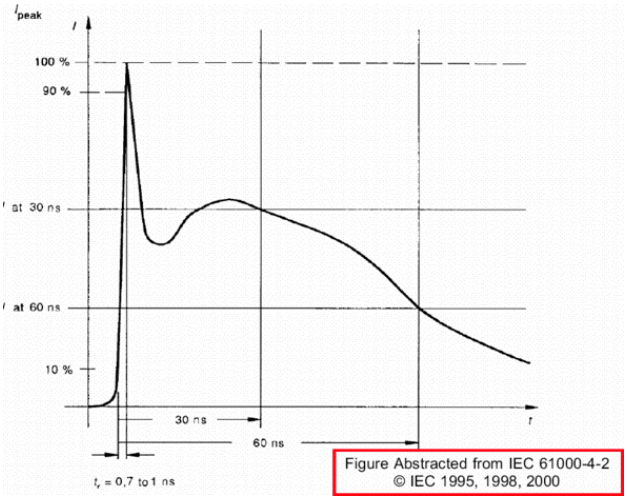


Figure 19. Electrostatic Discharge Waveform

PCB Recommendations

The NCP349 integrates a 2 A rated NMOSFET, and the PCB rules must be respected to properly evacuate the heat out of the silicon. The pin 7 (exposed pad) is internally connected to the internal NMOS Drain (Input). This exposed pad must be used to increase heat transfer and must be connected to Pin 1. Of course, in any case, this pad shall be not connected to any other potential.

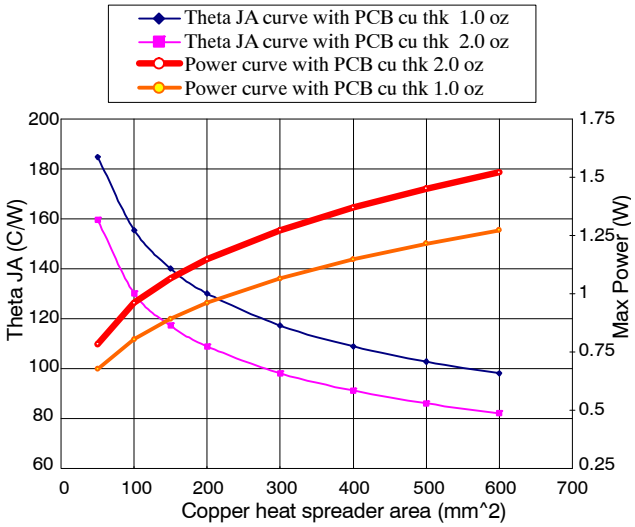


Figure 20.

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCP349MNAETBG	AE	DFN6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SELECTION GUIDE

The NCP349 can be available in several undervoltage and overvoltage thresholds versions. Part number is designated as follows:

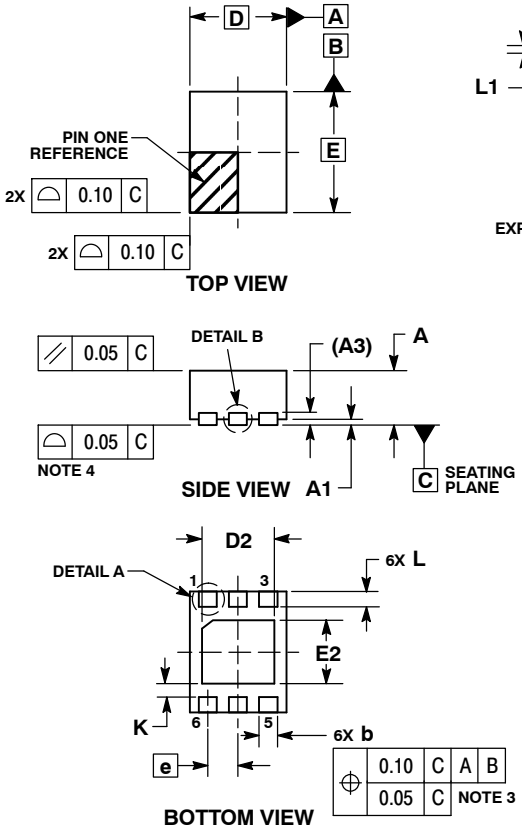
NCP349MNxxTxG

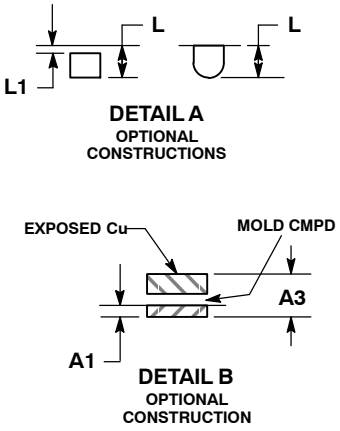
a b c

Code	Contents
a	UVLO Typical Threshold a: A = 2.95 V
b	OVLO Typical Threshold b: E = 5.68 V
c	Tape & Reel Type c: B = 3000

PACKAGE DIMENSIONS

DFN6, 1.6x2, 0.5P
CASE 506BM−01
ISSUE O

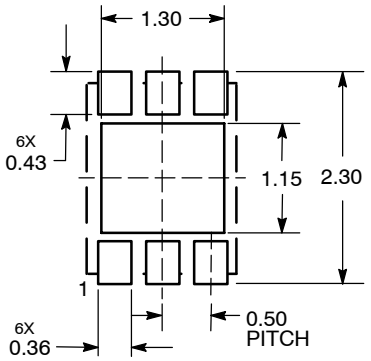




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.40
D	1.60 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.95	1.15
e	0.50 BSC	
K	0.20	---
L	0.15	0.35
L1	---	0.10

MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

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