

August 1998

## 54AC373 • 54ACT373 Octal Transparent Latch with TRI-STATE® Outputs

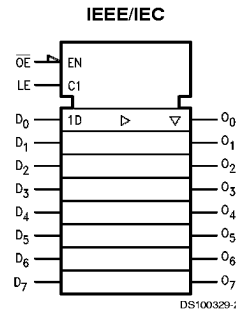
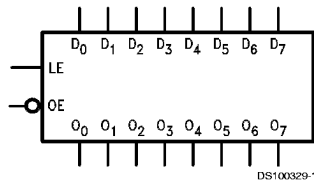
### General Description

The 'AC/'ACT373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ( $\overline{OE}$ ) is LOW. When  $\overline{OE}$  is HIGH, the bus output is in the high impedance state.

### Features

- $I_{CC}$  and  $I_{OZ}$  reduced by 50%
- Eight latches in a single package
- TRI-STATE outputs for bus interfacing
- Outputs source/sink 24 mA
- 'ACT373 has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD)
  - 'AC373: 5962-87555
  - 'ACT373: 5962-87556

### Logic Symbols

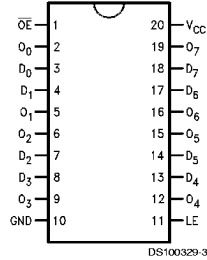


Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O <sub>0</sub> -O <sub>7</sub>	TRI-STATE Latch Outputs

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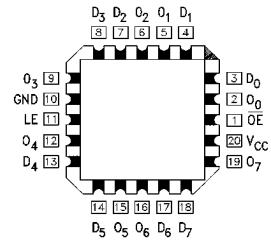
## Connection Diagrams

Pin Assignment for DIP and Flatpak



DS100329-3

Pin Assignment for LCC



DS100329-4

## Functional Description

The 'AC/ACT373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the standard outputs are in the 2-state mode. When  $\overline{OE}$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

## Truth Table

Inputs			Outputs
LE	$\overline{OE}$	$D_n$	$O_n$
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	$O_0$

H = HIGH Voltage Level

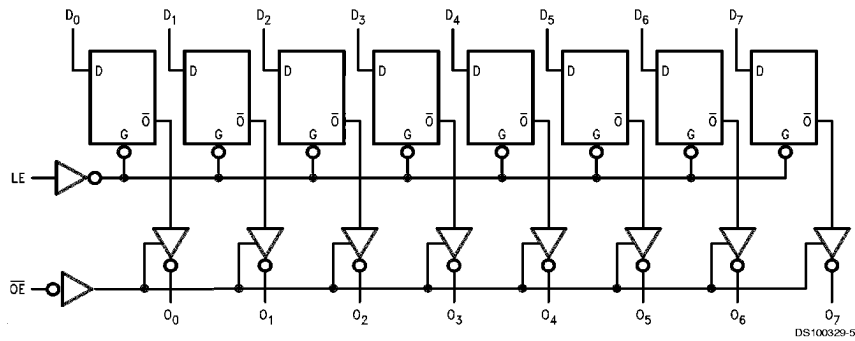
L = LOW Voltage Level

Z = High Impedance

X = Immaterial

$O_0$  = Previous  $O_0$  before HIGH to Low transition of Latch Enable

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)			Recommended Operating Conditions			
<p>If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.</p>			<p>Supply Voltage (<math>V_{CC}</math>)</p>			
Supply Voltage ( $V_{CC}$ )		-0.5V to +7.0V	'AC		2.0V to 6.0V	
DC Input Diode Current ( $I_{IK}$ )			'ACT		4.5V to 5.5V	
$V_I = -0.5V$		-20 mA	Input Voltage ( $V_I$ )		0V to $V_{CC}$	
$V_I = V_{CC} + 0.5V$		+20 mA	Output Voltage ( $V_O$ )		0V to $V_{CC}$	
DC Input Voltage ( $V_I$ )		-0.5V to $V_{CC} + 0.5V$	Operating Temperature ( $T_A$ )			
DC Output Diode Current ( $I_{OK}$ )			54AC/ACT		-55°C to +125°C	
$V_O = -0.5V$		-20 mA	Minimum Input Edge Rate ( $\Delta V/\Delta t$ )			
$V_O = V_{CC} + 0.5V$		+20 mA	'AC Devices			
DC Output Voltage ( $V_O$ )		-0.5V to $V_{CC} + 0.5V$	$V_{IN}$ from 30% to 70% of $V_{CC}$			
DC Output Source			$V_{CC}$ @ 3.3V, 4.5V, 5.5V		125 mV/ns	
or Sink Current ( $I_O$ )		$\pm 50$ mA	Minimum Input Edge Rate ( $\Delta V/\Delta t$ )			
DC $V_{CC}$ or Ground Current			'ACT Devices			
per Output Pin ( $I_{CC}$ or $I_{GND}$ )		$\pm 50$ mA	$V_{IN}$ from 0.8V to 2.0V			
Storage Temperature ( $T_{STG}$ )		-65°C to +150°C	$V_{CC}$ @ 4.5V, 5.5V		125 mV/ns	
Junction Temperature ( $T_J$ )			<b>Note 1:</b> Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.			
CDIP		175°C				
DC Characteristics for 'AC Family Devices						
Symbol	Parameter	$V_{CC}$ (V)	54AC	Units	Conditions	
			$T_A =$ -55°C to +125°C			
			<b>Guaranteed Limits</b>			
$V_{IH}$	Minimum High Level Input Voltage	3.0	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	3.15			
		5.5	3.85			
$V_{IL}$	Maximum Low Level Input Voltage	3.0	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	1.35			
		5.5	1.65			
$V_{OH}$	Minimum High Level Output Voltage	3.0	2.9	V	$I_{OUT} = -50 \mu A$	
		4.5	4.4			
		5.5	5.4			
		3.0	2.4	V	$V_{IN} = V_{IL}$ or $V_{IH}$	
		4.5	3.7		$I_{OH}$	-12 mA
		5.5	4.7		$I_{OH}$	-24 mA
$V_{OL}$	Maximum Low Level Output Voltage	3.0	0.1	V	$I_{OUT} = 50 \mu A$	
		4.5	0.1			
		5.5	0.1			
		3.0	0.50	V	$V_{IN} = V_{IL}$ or $V_{IH}$	
		4.5	0.50		$I_{OL}$	12 mA
		5.5	0.50		$I_{OL}$	24 mA
$I_{IN}$	Maximum Input Leakage Current	5.5	$\pm 1.0$	$\mu A$	$V_I = V_{CC}, GND$	

DC Characteristics for 'AC Family Devices (Continued)					
Symbol	Parameter	V <sub>CC</sub> (V)	54AC	Units	Conditions
			T <sub>A</sub> =		
			Guaranteed Limits		
I <sub>OZ</sub>	Maximum TRI-STATE Current	5.5	±5.0	µA	V <sub>I</sub> (OE) = V <sub>IL</sub> , V <sub>IH</sub> V <sub>I</sub> = V <sub>CC</sub> , GND V <sub>O</sub> = V <sub>CC</sub> , GND
I <sub>OLD</sub>	(Note 3) Minimum Dynamic Output Current	5.5	50	mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>	Output Current	5.5	-50	mA	V <sub>OHD</sub> = 3.85V Min
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	80.0	µA	V <sub>IN</sub> = V <sub>CC</sub> or GND
<p><b>Note 2:</b> All outputs loaded, thresholds on input associated with output under test.</p> <p><b>Note 3:</b> Maximum test duration 2.0 ms, one output loaded at a time.</p> <p><b>Note 4:</b> I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>. I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.</p>					
DC Characteristics for 'ACT Family Devices					
Symbol	Parameter	V <sub>CC</sub> (V)	54ACT	Units	Conditions
			T <sub>A</sub> =		
			Guaranteed Limits		
V <sub>IH</sub>	Minimum High Level Input Voltage	4.5 5.5	2.0 2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
V <sub>IL</sub>	Maximum Low Level Input Voltage	4.5 5.5	0.8 0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
V <sub>OH</sub>	Minimum High Level Output Voltage	4.5	4.4	V	I <sub>OUT</sub> = -50 µA
		5.5	5.4		
		4.5 5.5	3.70 4.70	V	(Note 5) V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> -24 mA -24 mA
V <sub>OL</sub>	Maximum Low Level Output Voltage	4.5	0.1	V	I <sub>OUT</sub> = 50 µA
		5.5	0.1		
		4.5 5.5	0.50 0.50	V	(Note 5) V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> 24 mA 24 mA
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	±1.0	µA	V <sub>I</sub> = V <sub>CC</sub> , GND
I <sub>OZ</sub>	Maximum TRI-STATE Current	5.5	±5.0	µA	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> V <sub>O</sub> = V <sub>CC</sub> , GND
I <sub>CC(T)</sub>	Maximum I <sub>CC</sub> /Input	5.5	1.6	mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V
I <sub>OLD</sub>	(Note 6) Minimum Dynamic Output Current	5.5	50	mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>	Output Current	5.5	-50	mA	V <sub>OHD</sub> = 3.85V Min
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	80.0	µA	V <sub>IN</sub> = V <sub>CC</sub> or GND
<p><b>Note 5:</b> All outputs loaded; thresholds on input associated with output under test.</p> <p><b>Note 6:</b> Maximum test duration 2.0 ms, one output loaded at a time.</p> <p><b>Note 7:</b> I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.</p>					

<b>AC Electrical Characteristics</b>						
Symbol	Parameter	V <sub>CC</sub> (V) (Note 8)	54AC		Units	
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Min	Max		
t <sub>PLH</sub>	Propagation Delay D <sub>n</sub> to O <sub>n</sub>	3.3	1.0	16.5	ns	
		5.0	1.5	11.5		
t <sub>PHL</sub>	Propagation Delay D <sub>n</sub> to O <sub>n</sub>	3.3	1.0	16.0	ns	
		5.0	1.5	11.5		
t <sub>PLH</sub>	Propagation Delay LE to O <sub>n</sub>	3.3	1.0	16.5	ns	
		5.0	1.5	12.0		
t <sub>PHL</sub>	Propagation Delay LE to O <sub>n</sub>	3.3	1.0	15.0	ns	
		5.0	1.5	11.0		
t <sub>PZH</sub>	Output Enable Time	3.3	1.0	14.0	ns	
		5.0	1.5	10.5		
t <sub>PZL</sub>	Output Enable Time	3.3	1.0	13.5	ns	
		5.0	1.5	10.0		
t <sub>PHZ</sub>	Output Disable Time	3.3	1.0	16.0	ns	
		5.0	1.5	13.5		
t <sub>PLZ</sub>	Output Disable Time	3.3	1.0	13.0	ns	
		5.0	1.5	10.5		
<p><b>Note 8:</b> Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V</p>						
<b>AC Operating Requirements</b>						
Symbol	Parameter	V <sub>CC</sub> (V) (Note 9)	54AC		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Guaranteed Minimum			
t <sub>s</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to LE	3.3	6.5		ns	
		5.0	5.0			
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to LE	3.3	1.0		ns	
		5.0	1.0			
t <sub>w</sub>	LE Pulse Width, HIGH	3.3	6.5		ns	
		5.0	5.0			
<p><b>Note 9:</b> Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V</p>						

<b>AC Electrical Characteristics</b>					
Symbol	Parameter	V <sub>CC</sub> (V) (Note 10)	54ACT		Units
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		
			Min	Max	
t <sub>PLH</sub>	Propagation Delay D <sub>n</sub> to O <sub>n</sub>	5.0	1.5	12.5	ns
t <sub>PHL</sub>	Propagation Delay D <sub>n</sub> to O <sub>n</sub>	5.0	1.5	12.5	ns
t <sub>PLH</sub>	Propagation Delay LE to O <sub>n</sub>	5.0	1.5	12.5	ns
t <sub>PHL</sub>	Propagation Delay LE to O <sub>n</sub>	5.0	1.5	11.5	ns
t <sub>PZH</sub>	Output Enable Time	5.0	1.5	11.5	ns
t <sub>PZL</sub>	Output Enable Time	5.0	1.5	11.0	ns
t <sub>PHZ</sub>	Output Disable Time	5.0	1.5	14.0	ns
t <sub>PLZ</sub>	Output Disable Time	5.0	1.5	11.0	ns

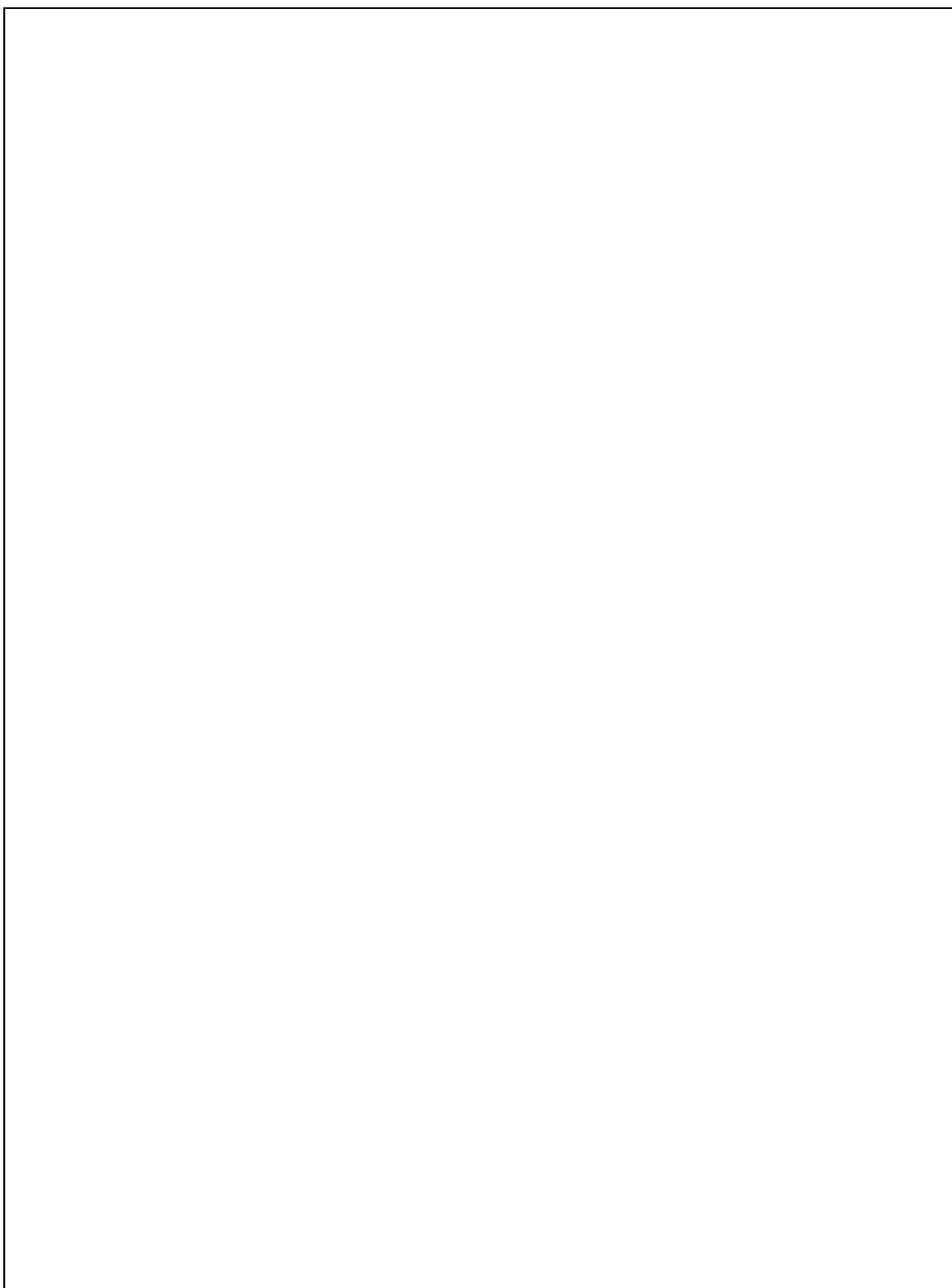
**Note 10:** Voltage Range 5.0 is 5.0V ±0.5V

<b>AC Operating Requirements</b>					
Symbol	Parameter	V <sub>CC</sub> (V) (Note 11)	54ACT		Units
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		
			Guaranteed Minimum		
t <sub>s</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to LE	5.0	8.5		ns
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to LE	5.0	1.0		ns
t <sub>w</sub>	LE Pulse Width, HIGH	5.0	8.5		ns

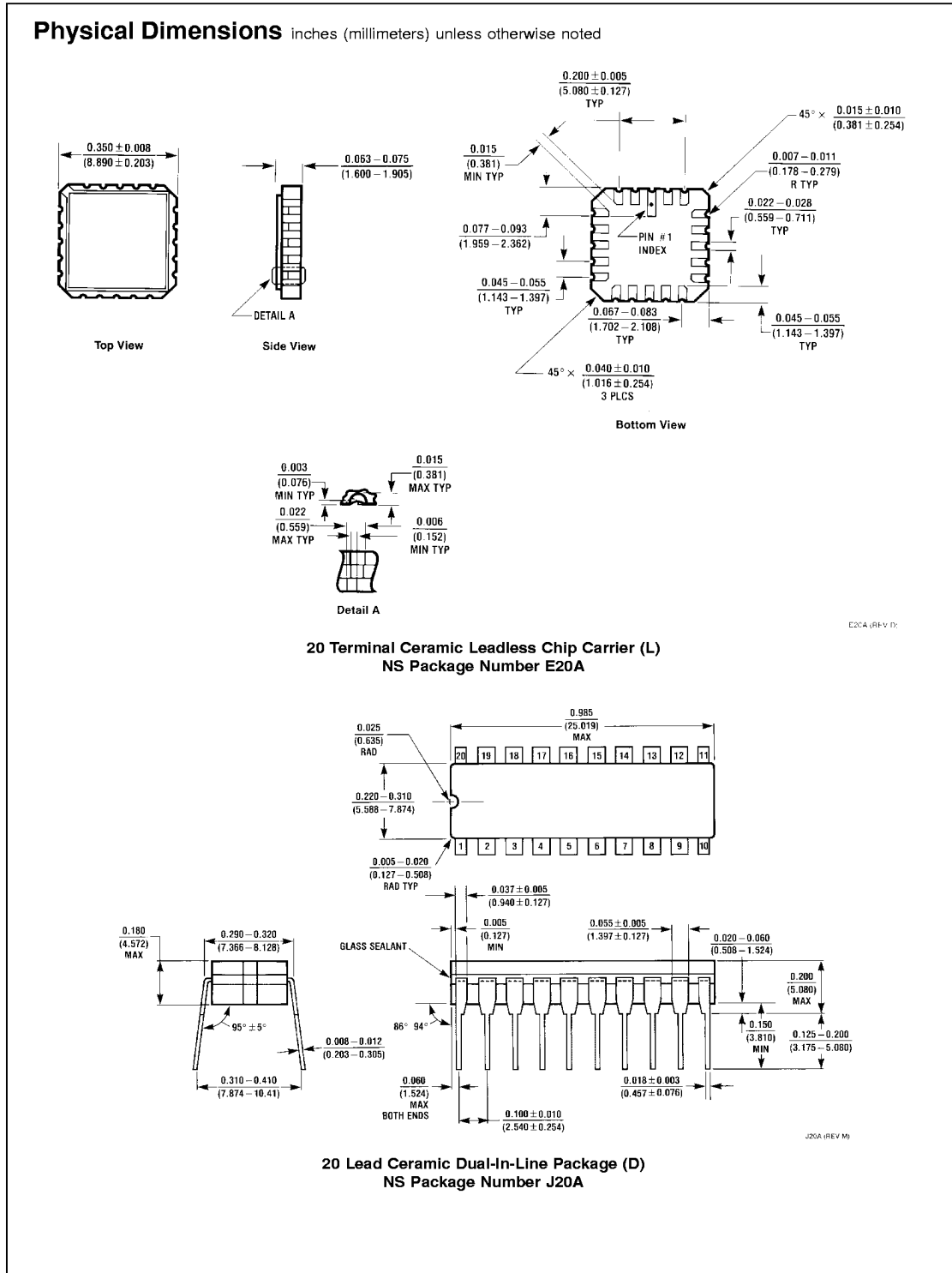
**Note 11:** Voltage Range 5.0 is 5.0V ±0.5V

<b>Capacitance</b>					
Symbol	Parameter	Typ	Units	Conditions	
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN	
C <sub>PD</sub>	Power Dissipation Capacitance	40.0	pF	V <sub>CC</sub> = 5.0V	

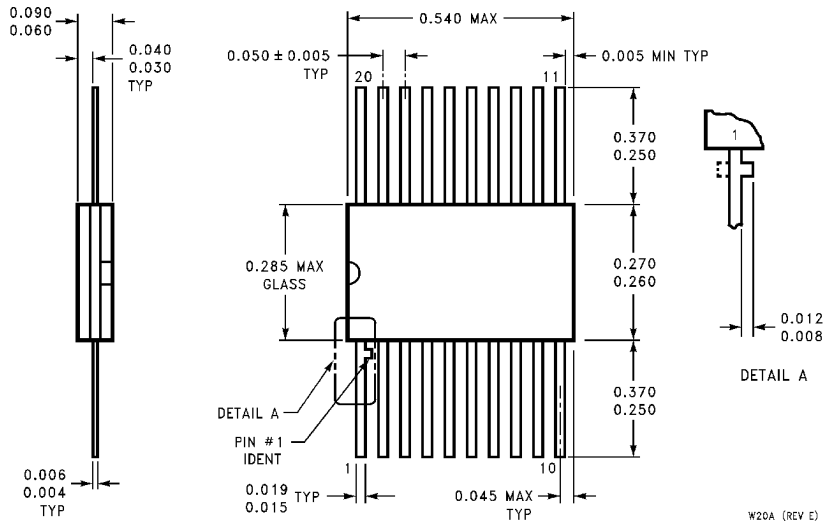
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**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**20-Lead Ceramic Flatpak (F)  
NS Package Number W20A**

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