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National Semiconductor

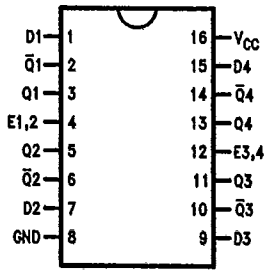
54LS375/DM74LS375 4-Bit Latch

General Description

The 'LS375 is a 4-bit D-type latch for use as temporary storage for binary information between processing units and input/output or indicator units. When its Enable (E) input is HIGH, a latch is transparent, i.e., the Q output will follow the D input each time it changes. When E is LOW a latch stores the last valid data present on the D input preceding the HIGH-to-LOW transition of E. The 'LS375 is functionally identical to the 'LS75 except for the corner power pins.

Connection Diagram

Dual-In-Line Package



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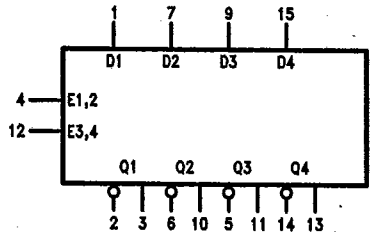
Order Number 54LS375DMQB, 54LS375FMQB, DM74LS375M or DM74LS375N
See NS Package Number J16A, M16A, N16E or W16A

Logic Symbol



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V_{CC} = Pin 16
GND = Pin 8

Pin Name	Description
D1–D4	Data Inputs
E1, 2	Latches 1, 2 Enable Inputs
E3, 4	Latches 3, 4 Enable Inputs
Q1–Q4	Latch Outputs
$\overline{Q}$1–Q4	Complementary Latch Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	10V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS375			DM74LS375			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to E_n	20			20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to E_n	0			0			ns
t_w (H)	E_n Pulse Width HIGH	20			15			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
			Enable Input			0.4	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
			Enable Input			80	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
			Enable Input			−1.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				12	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

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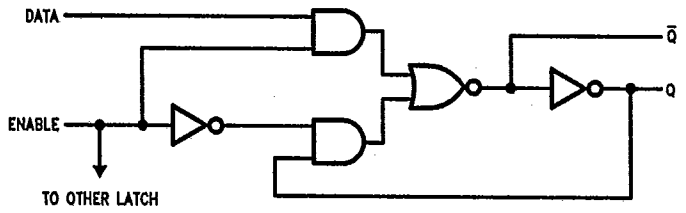
Symbol	Parameter	54LS/DM74LS C_L = 15 pF Min	54LS/DM74LS C_L = 15 pF Max	Units
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n		27 23	ns
t_{PLH} t_{PHL}	Propagation Delay D_n to $\overline{Q}_n$		20 15	ns
t_{PLH} t_{PHL}	Propagation Delay E_n to Q_n		27 25	ns
t_{PLH} t_{PHL}	Propagation Delay E_n to $\overline{Q}_n$		30 18	ns

Truth Table (Each Latch)

t_n	$t_n + 1$
D	Q
H	H
L	L

t_n = Bit time before Enable negative going transition.
t_{n+1} = Bit time after Enable negative going transition.
H = HIGH Voltage Level
L = LOW Voltage Level

Logic Diagram (1/4 of diagram shown)



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