Power Management Unit for Imaging Modules

ADP5020

FEATURES

- Input voltage range: 2.4 V to 5.5 V
- Low standby current: 1 µA
- Switching frequency: 3 MHz
- I²C interface
- Synchronous Buck 1 regulator: 600 mA
- Synchronous Buck 2 regulator: 250 mA
- Low dropout regulator (LDO): 150 mA
- Internal compensation
- Internal soft start
- Thermal shutdown
- 20-lead 4 mm × 4 mm LFCSP

APPLICATIONS

- Digital cameras, handsets
- Mobile TVs

TYPICAL APPLICATIONS CIRCUIT

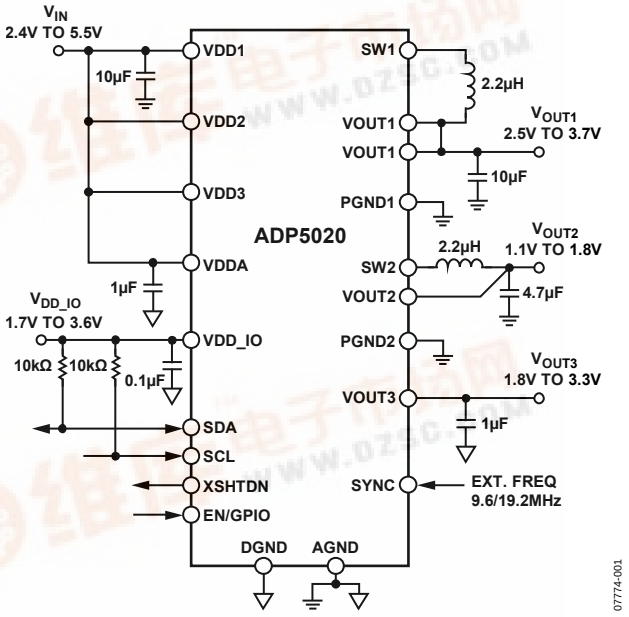

Figure 1.

GENERAL DESCRIPTION

The ADP5020 provides a highly integrated power solution that includes all of the power circuits necessary for a digital imaging module. It comprises two step-down dc-to-dc converters, one LDO, and a power sequence controller. All dc-to-dc converters integrate power pMOSFETs and nMOSFETs, making the system simpler and more compact and reducing the cost. The ADP5020 has digitally programmed output voltages and buck converters that can source up to 600 mA. A fixed frequency operation of 3 MHz enables the use of tiny inductors and capacitors. The buck converters use a voltage mode, constant-frequency PWM control scheme, and the synchronous rectification is implemented to reduce the power loss. The Buck 1 regulator operates at up to 93% efficiency.

The ADP5020 provides high performance, reduces component count and size, and is lower in cost when compared to conventional designs.

The ADP5020 runs on input voltage from 2.4 V to 5.5 V and supports one-cell lithium-ion (Li+) batteries. The high performance LDO maximizes noise suppression. The ADP5020 can be activated via an I²C® interface or through a dedicated enable input. During logic-controlled shutdown, the input is disconnected from the output source, and the part draws 1 µA typical from the input source. Other key features include undervoltage lockout to prevent deep-battery discharge and soft start to prevent input current overshoot at startup. The ADP5020 is available in a 20-lead LFCSP.

Rev. 0

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REVISION HISTORY

4/09—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

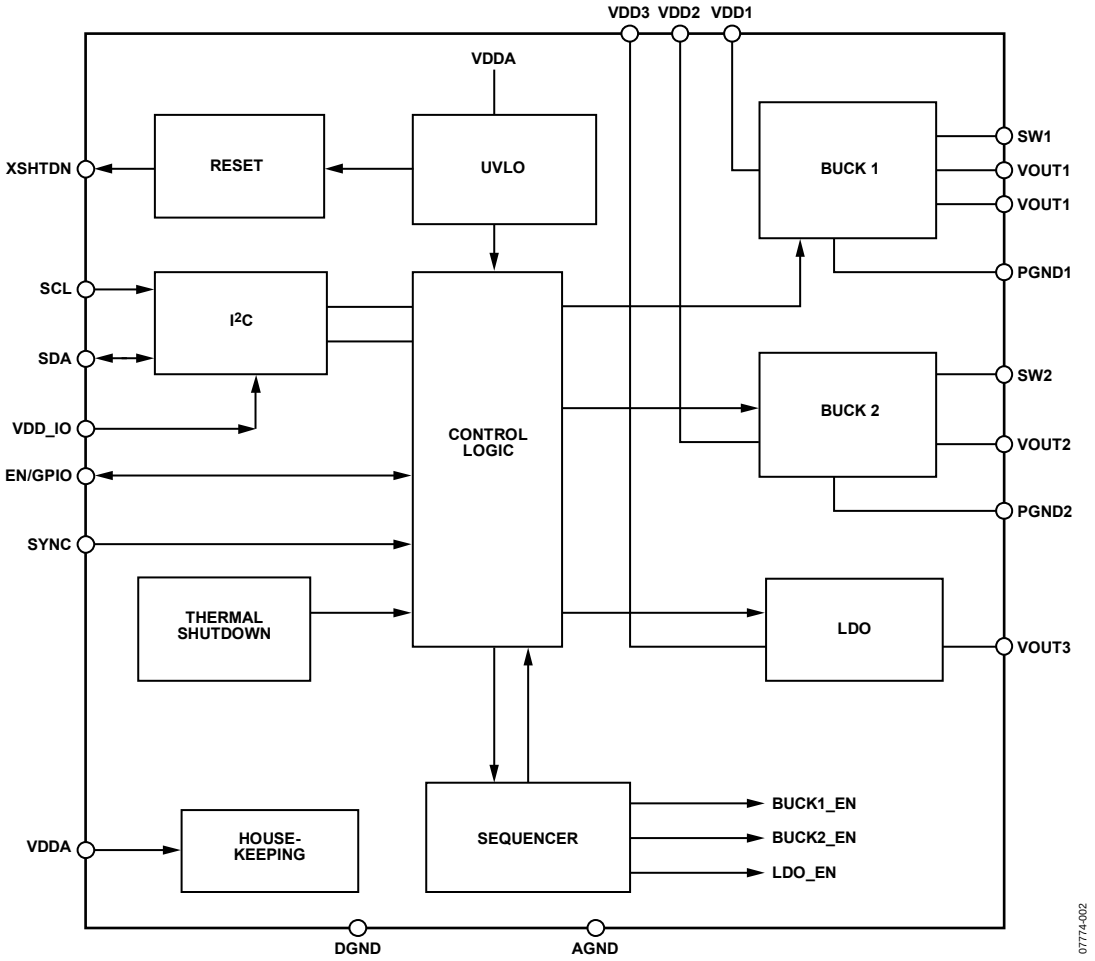

Figure 2.

SPECIFICATIONS

T_J = −40°C to +125°C, V_{DDx} = 3.6 V, V_{DD_IO} = 1.8 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OPERATING RANGE						
VDDx Operating Voltage Range	V_{DD}		2.4		5.5	V
Logic I/O Operating Voltage Range[1]	V_{DD_IO}		1.7		3.6	V
EN, SDA, SCL CHARACTERISTICS						
Low Level Input Voltage	V_{IL}				$0.3 \times V_{DD\_IO}$	V
High Level Input Voltage	V_{IH}		$0.7 \times V_{DD\_IO}$			V
INPUT LOGIC CURRENT	I_{LK}	Internal pull-down, 1 MΩ	−1		+6	µA
XSHTDN, EN/GPIO						
Low Level Output Voltage	V_{OL}	I_{RST} = +3 mA			$0.2 \times V_{DD\_IO}$	V
High Level Output Voltage	V_{OH}	I_{RST} = −3 mA	$0.8 \times V_{DD\_IO}$			V
OUTPUT LOGIC LEAKAGE CURRENT	I_{LK}				1	µA
UNDERVOLTAGE LOCKOUT THRESHOLD						
Falling	V_{UVLOF}	Referenced to V_{DDA}	1.8	2.0		V
Rising	V_{UVLOR}	Referenced to V_{DDA}		2.2	2.4	V
POWER-ON RESET THRESHOLD						
Falling	V_{PORF}	Referenced to V_{DDA}	1.0	1.4		V
Rising	V_{PORR}	Referenced to V_{DDA}		1.6	1.7	V
UVLO GLITCH DEBOUNCE TIME		V_{DD} > POR levels		50		µs
SHUTDOWN OUTPUT DURATION[2]	t_{XSHTDN}	XSHTDN line driven low		1		ms
POWER GOOD (POK) ACTIVATION DELAY TIME[3]						
EN to First Regulator	t_{REG1}			5		ms
First to Second Regulator	t_{REG2}			5		ms
Second to Third Regulator	t_{REG3}			5		ms
NO LOAD CURRENT CHARACTERISTICS						
Standby Current	$I_{Q(STNBY)}$	EN = 0		1	5	µA
Lockout Current	I_{LOCK}	EN = 0, $V_{DDA} < V_{UVLOF}$		1	1	µA
Operating Quiescent Current, Switching[4]	I_Q	I_{LOAD} = 0 mA		10	15	mA
THERMAL CHARACTERISTICS						
Thermal Shutdown, T_J Rising	T_{SD}			150		°C
Thermal Shutdown Hysteresis				30		°C
HOUSEKEEPING BLOCK						
Power Good Threshold	V_{PG}		70	80	90	%

[1] The V_{DD_IO} voltage must be less than or equal to the level on the V_{DDx} supply lines.
[2] Shutdown output duration is automatic when using the EN pin. To get this delay when using I²C, FORCE_XS must be set to 1.
[3] Activation delays apply only when the device is activated through the EN pin or the EN_ALL bit (Address 0x03[4]); the sequencer controls the turning on of the regulators.
[4] The quiescent current is calculated as though all regulators are powered up.

SWITCHING SPECIFICATIONS

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SWITCHING FREQUENCY						
CH1	f_{SW1}	Sync disabled	2.5	3	3.6	MHz
CH2	f_{SW2}	Sync disabled	2.5	3	3.6	MHz
SYNC CLOCK DIVIDER RATIO						
	$RATIO_{DIV}$	SYNC_9P6 = 1		3		
	$RATIO_{DIV}$	SYNC_19P2 = 1		6		
SYNC CHARACTERISTICS						
Frequency Range						
	f_{SYNC1}			9.6		MHz
	f_{SYNC2}			19.2		MHz
Frequency Duty Cycle	$f_{SYNCDUTY}$		40	50	60	%
Signal						
DC Coupling Level						
Low Level Input Voltage	V_{IL}				$0.3 \times V_{DD\_IO}$	V
High Level Input Voltage	V_{IH}		$0.7 \times V_{DD\_IO}$			V
DC Coupling	V_{SYNC}		0		V_{DD_IO}	V
AC Coupling Level	V_{CAC-PP}	Sine wave, peak-to-peak	0.5	1.0	V_{DD_IO}	V
AC Coupling Capacitor				10		nF
Input Current	I_{SYNC}	SYNC_9P6 = 1, or SYNC_19P2 = 1		50		µA

DC-TO-DC CONVERSION SPECIFICATIONS, BUCK 1 REGULATOR

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE						
Range[1]	V_{OUT1}	3-bit range	2.5		3.7	V
Initial Accuracy		T_A = 25°C, V_{DD1}[2], V_{OUT1} = 3.3 V, I_{LOAD} = 20 mA	−1		+1	%
Total Accuracy		V_{DD1}[3], I_{LOAD} = 50 mA to 600 mA	−5		+4	%
VOUT1 REGULATION						
Load Regulation		I_{LOAD} = 20 mA to 600 mA		0.2		%
Line Regulation		V_{DDA} = 1.8 V, V_{DD1}[2,3]		0.15		%
CURRENT						
Maximum Output Current	I_{BK1MAX}	V_{DD1}[3], V_{OUT1} = 2.5 V to 3.7 V			600	mA
Quiescent Current	I_{QBK1}	I_{LOAD} = 0 mA		4	6	mA
POWER						
Low-Side Power nMOSFET	R_{DSON1}	I_D = 400 mA		175	250	mΩ
High-Side Power pMOSFET	R_{DSON1}	I_D = 400 mA		250	400	mΩ
SWITCH CURRENT LIMIT	I_{CL1}		0.8	1.2	1.6	A
MINIMUM ON TIME	t_{MIN1}			55		ns
MAXIMUM DUTY CYCLE	D_{MAX1}			88	95	%
SOFT START TIME	t_{SS1}			1.4		ms
C_{OUT} DISCHARGE SWITCH ON RESISTANCE	R_{DIS1}		0.7	1	1.3	kΩ

[1] See Table 13 (the BUCK1_VSEL register, Address 0x01) for details.
[2] V_{DD1} = 3.1 V to 5.5 V, I_{LOAD} is less than 200 mA. For tight regulation, the supply voltage must be 0.6 V higher than the output voltage.
[3] V_{DD1} = 3.7 V to 5.5 V, I_{LOAD} is more than 200 mA. For tight regulation, the supply voltage must be 1.2 V higher than the output voltage.

DC-TO-DC CONVERSION SPECIFICATIONS, BUCK 2 REGULATOR

Table 4.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE						
Adjustable Range[1]	V_{OUT2}	4-bit range	1.1		1.8	V
Initial Accuracy		T_A = 25°C, V_{DD2} = 3.6 V, V_{OUT2} = 1.2 V, I_{LOAD} = 20 mA	−1		+1	%
Total Accuracy		V_{DD2} = 2.5 V to 5 V, I_{LOAD} = 10 mA to 250 mA	−5		+4	%
Load Regulation		I_{LOAD} = 10 mA to 250 mA		0.2		%
Line Regulation		V_{DDA} = 1.8 V, V_{DD2} = 2.5 V to 5 V		0.15		%
CURRENT						
Maximum Output Current	I_{BK2MAX}				250	mA
Quiescent Current	I_{QBK2}	I_{LOAD} = 0 mA		4	6.5	mA
POWER						
Low-Side Power nMOSFET	R_{DSON2}	I_D = 200 mA		240	330	mΩ
High-Side Power pMOSFET	R_{DSON2}	I_D = 200 mA		300	450	mΩ
SWITCH CURRENT LIMIT	I_{CL2}		360	630	850	mA
MINIMUM ON TIME	t_{MIN2}			55		ns
MAXIMUM DUTY CYCLE	D_{MAX2}			87.5	90	%
SOFT START TIME	t_{SS2}			900		µs
C_{OUT} DISCHARGE SWITCH ON RESISTANCE	R_{DIS2}		0.7	1	1.3	kΩ

[1] See Table 14 (the BUCK2_LDO_VSEL register, Address 0x02) for details.

VOUT3 SPECIFICATIONS, LOW DROPOUT (LDO) REGULATOR

Table 5.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE						
Adjustable Range[1]	V_{OUT3}	100 mV step, 4-bit range	1.8		3.3	V
Initial Accuracy		T_A = 25°C, V_{DD3} = 3.6 V, V_{OUT3} = 1.8 V, I_{LOAD} = 10 mA	−1.5		+1.5	%
Total Accuracy		V_{DD3} = 2.5 V to 5 V, I_{LOAD} = 0 mA to 150 mA	−5		+4	%
Load Regulation		I_{LOAD} = 10 mA to 100 mA		0.45	0.75	%
Line Regulation		I_{LOAD} = 100 mA[2]		0.15	0.30	%
CURRENT						
Maximum Output Current	I_{LDOMAX}				150	mA
Dropout Voltage	$V_{LDODROP}$	At 100 mA, V_{OUT3} = 3.3 V		70	100	mV
Quiescent Current	I_Q	I_{LOAD} = 0 mA		45	85	µA
Short-Circuit Current Limit			200	400	600	mA
Power Supply Rejection Ratio	PSRR					
		f = 1 kHz, V_{DD3} = 5 V, V_{OUT3} = 3.3 V, I_{LOAD} = 50 mA		47		dB
		f = 10 kHz, V_{DD3} = 5 V, V_{OUT3} = 3.3 V, I_{LOAD} = 50 mA		44		dB
SOFT START TIME	t_{SS2}			70		µs
C_{OUT} DISCHARGE SWITCH ON RESISTANCE	R_{DIS8}		0.7	1	1.3	kΩ

[1] See Table 14 (the BUCK_LDO_VSEL register, Address 0x02) for details.
[2] $V_{DD3} > V_{OUT3} + L_{DODROP}$.

I²C TIMING SPECIFICATIONS

Table 6.

Parameter	Min	Max	Unit	Description
f_{SCL}		400	kHz	SCL clock frequency
t_{HIGH}	0.6		µs	SCL high time
t_{LOW}	1.3		µs	SCL low time
$t_{SU,DAT}$	100		ns	Data setup time
$t_{HD,DAT}$ [1]	0	0.9	µs	Data hold time
$t_{SU,STA}$	0.6		µs	Setup time for repeated start
$t_{HD,STA}$	0.6		µs	Hold time for start/repeated start
t_{BUF}	1.3		µs	Bus free time between a stop condition and a start condition
$t_{SU,STO}$	0.6		µs	Setup time for stop condition
t_{RISE}	$20 + 0.1C_B$	300	ns	Rise time of SCL/SDA
t_{FALL}	$20 + 0.1C_B$	300	ns	Fall time of SCL/SDA
t_{SP}	0	50	ns	Pulse width of suppressed spike
C_B [2]		400	pF	Capacitive load for each bus line

[1] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the SCL falling edge.
[2] C_B is the total capacitance of one bus line in picofarads (pF).

Timing Diagram

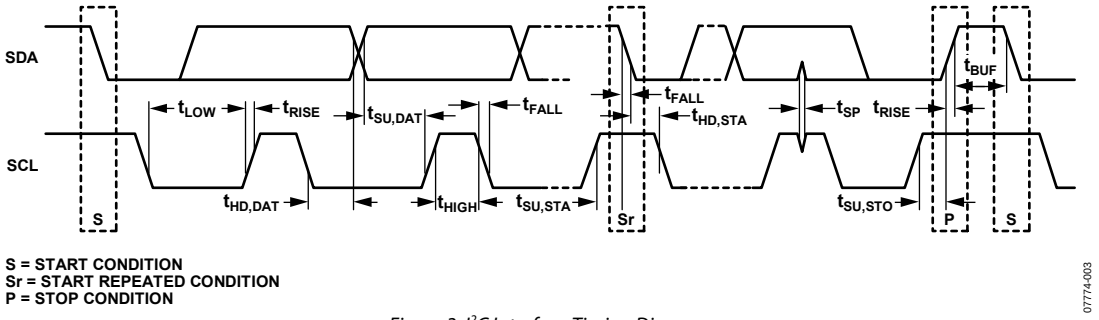

Figure 3. I²C Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
VDD1, VDD2, VDD3	−0.3 V to +6 V
SW1, SW2	−0.3 V to +6 V
VOUT1, VOUT2, VOUT3	−0.3 V to +6 V
VDD_IO	−0.3V to +3.6 V
EN, SCL, SDA, SYNC, XSHTDN	−0.3 V to V_{DD_IO} + 0.3 V
Operating Temperature Range	
Ambient	−40°C to +85°C
Junction	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	260°C
Soldering (10 sec)	260°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
V_{ESD}	
Machine Model Range	−200 V to +200 V
Human Body Model Range	−2000 V to +2000 V
Charged Device Model	±750 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

The ADP5020 can be damaged when the junction temperature (T_J) limits are exceeded. Monitoring the ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated. In applications having moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The T_J of the device is dependent on the ambient temperature (T_A), the power dissipation (PD) of the device, and the junction-to-ambient thermal resistance of the package (θ_{JA}). Maximum T_J is calculated from T_A and PD using the following formula:

$$T_J = T_A + (PD \times \theta_{JA})$$

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
20-Lead LFCSP (CP-20-4)	47.4	4.3	°C/W

Thermal Data

Junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified value of θ_{JA} is based on a 4-layer, 4 in × 3 in, 2 1/2 oz copper board, as per JEDEC standards. For more information, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

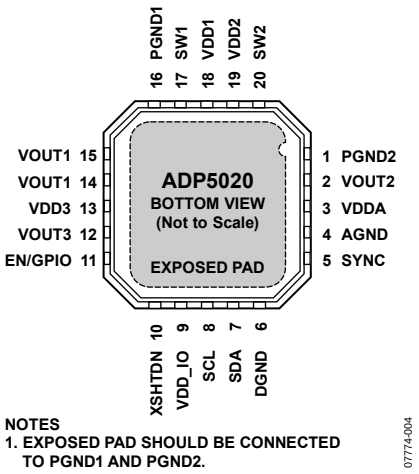

Figure 4. Pin Configuration (Bottom View)

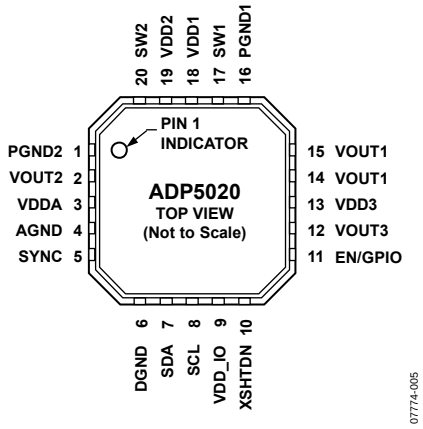

Figure 5. Pin Configuration (Top View)

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PGND2	Power Ground Buck 2.
2	VOUT2	Feedback Buck 2.
3	VDDA	Supply Voltage Internal Analog Circuit.
4	AGND	Analog Ground.
5	SYNC	Frequency Synchronization. Connect to an external 19.2 MHz or 9.6 MHz clock signal to synchronize the internal oscillator.
6	DGND	Digital Ground.
7	SDA	I^2C Data.
8	SCL	I^2C Clock.
9	VDD_IO	Supply Voltage for Internal Logic Inputs/Outputs.
10	XSHTDN	Shutdown Output, Active Low.
11	EN/GPIO	After power-on reset, this pin is defined as enable (EN). To enable active high, the I^2C command can program this pin to be an output (GPIO). A weak pull-down resistor is enabled when the pin operates as EN.
12	VOUT3	Regulated Output Voltage from LDO.
13	VDD3	Supply Voltage LDO.
14, 15	VOUT1	Feedback/Driver Buck 1 Output.
16	PGND1	Power Ground Buck 1.
17	SW1	Switch Pin Buck 1.
18	VDD1	Supply Voltage Buck 1.
19	VDD2	Supply Voltage Buck 2.
20	SW2	Switch Pin Buck 2.
EPAD	Exposed paddle	Exposed pad should be connected to PGND1 and PGND2.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 4.5 V, V_{OUT1} = 2.8 V, V_{OUT2} = V_{OUT3} = 1.8 V, I_{OUT} = 100 mA, C_4 = C_1 = 10 µF, C_2 = 4.7 µF, C_3 = 1 µF, T_J = 25°C, unless otherwise noted.

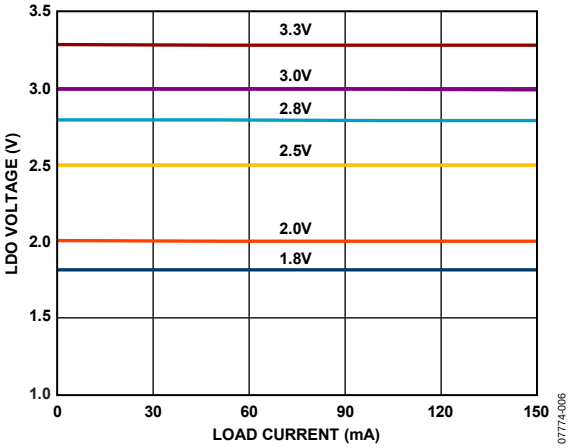

Figure 6. LDO Load Regulation

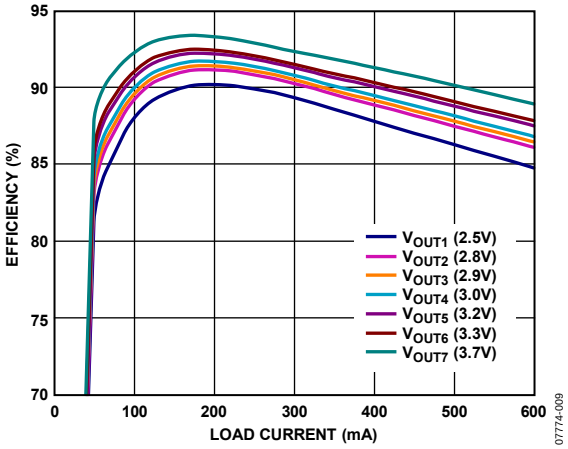

Figure 9. Buck 1, Efficiency vs. Load Current

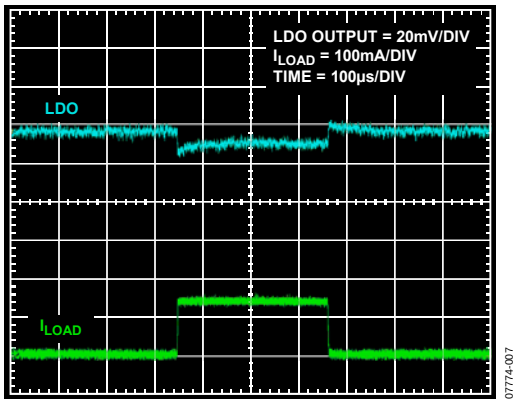

Figure 7. LDO Load Transient

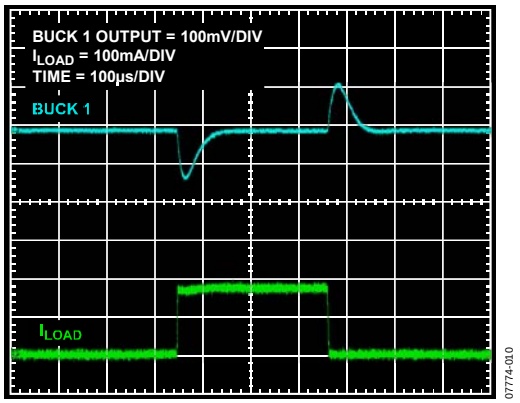

Figure 10. Buck 1 Load Transient Response

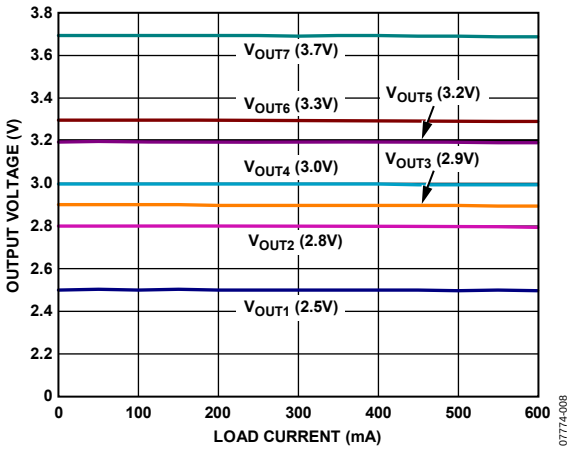

Figure 8. Buck 1 Load Regulation

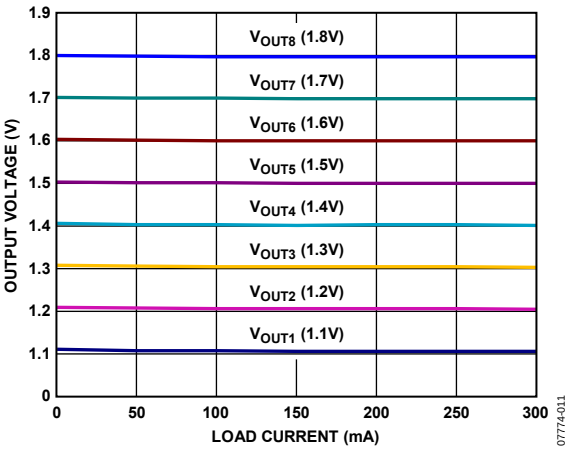

Figure 11. Buck 2 Load Regulation

V_{IN} = 4.5 V, V_{OUT1} = 2.8 V, V_{OUT2} = V_{OUT3} = 1.8 V, I_{OUT} = 100 mA, C_4 = C_1 = 10 µF, C_2 = 4.7 µF, C_3 = 1 µF, T_J = 25°C, unless otherwise noted.

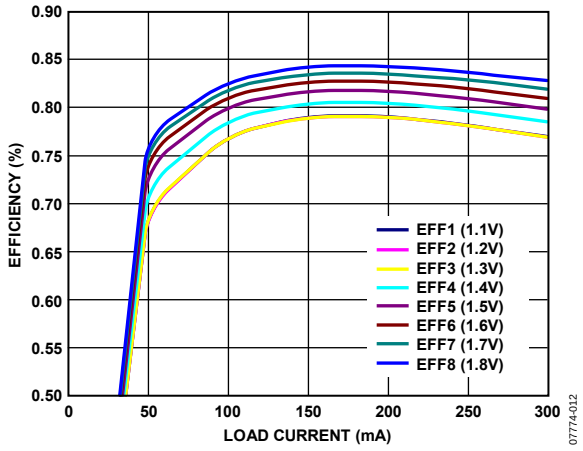

Figure 12. Buck 2 Efficiency vs. Load Current

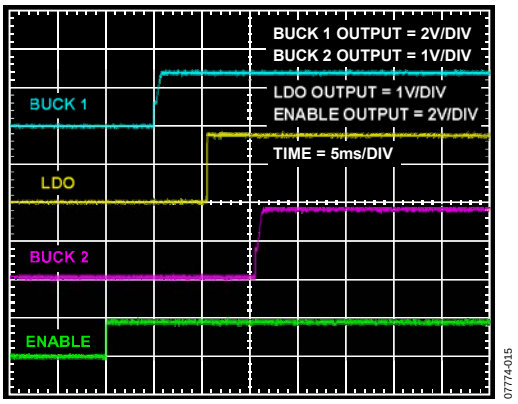

Figure 15. Startup Sequence of the Three Regulators, Set by Default

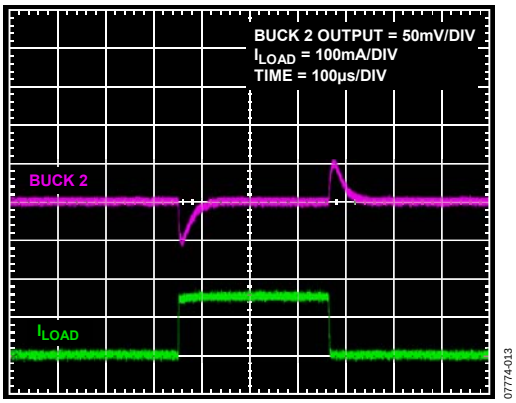

Figure 13. Buck 2 Load Transient Response

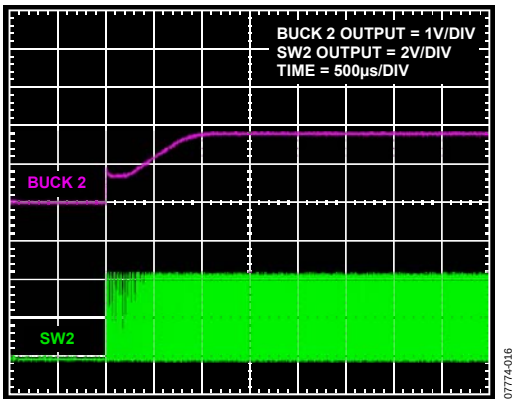

Figure 16. Buck 2 Enable Startup

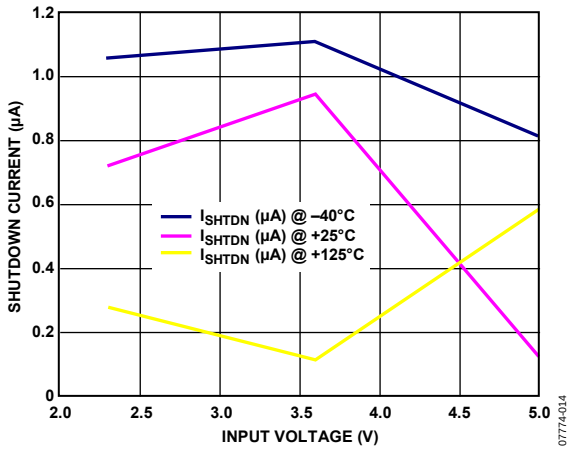

Figure 14. Shutdown Current vs. Input Voltage

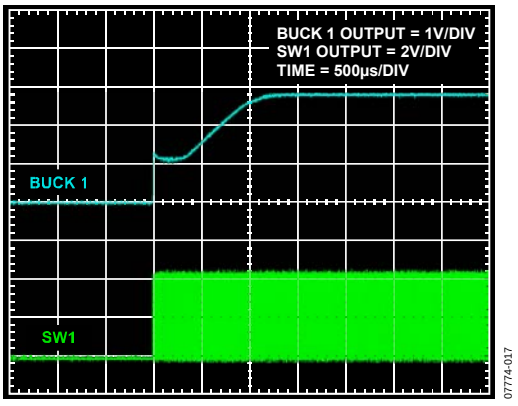

Figure 17. Buck 1 Enable Startup

V_{IN} = 4.5 V, V_{OUT1} = 2.8 V, V_{OUT2} = V_{OUT3} = 1.8 V, I_{OUT} = 100 mA, C_4 = C_1 = 10 µF, C_2 =4.7 µF, C_3 = 1 µF, T_J = 25°C, unless otherwise noted.

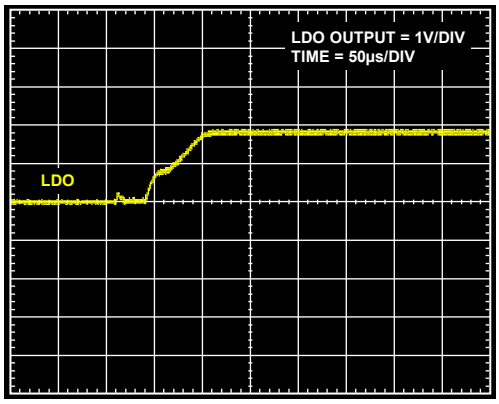

Figure 18. LDO Startup

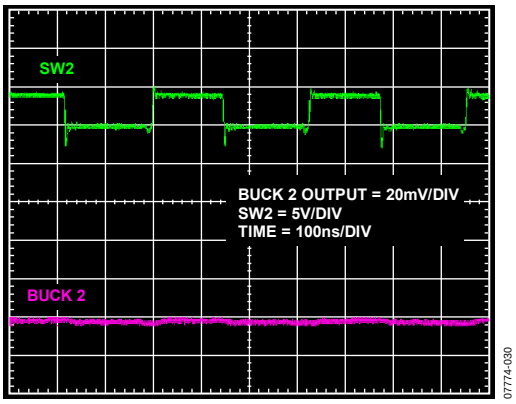

Figure 20. Buck 2 Switching Node Voltage and Output Ripple Voltage

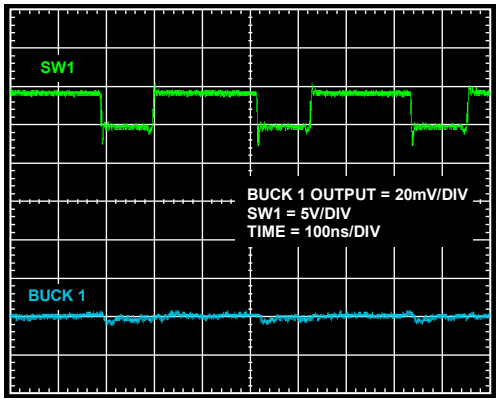

Figure 19. Buck 1 Switching Node Voltage and Output Ripple Voltage

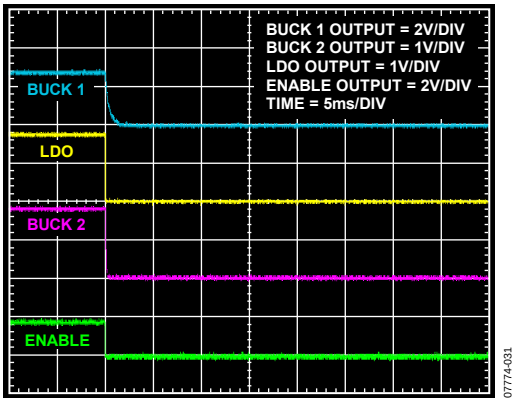

Figure 21. Three Regulators Turned Off by Sequencer

THEORY OF OPERATION

CIRCUIT OPERATION

The buck converters use pMOSFET as the upper switch and nMOSFET as a synchronous rectifier. This synchronous rectification maintains high efficiency for a wide input and output voltage range. The voltage mode control architecture, which features a high frequency bandwidth, provides a fast load and line transient response. The Buck 1 regulator can deliver up to 600 mA with very tight regulation. To minimize cross conduction and maximize efficiency, an antishoot-through circuit is implemented in the gate driver. The two switching regulators operate out of phase, reducing input ripple voltage and current.

INTERNAL COMPENSATION

The ADP5020 contains an internal compensation network. The compensation circuit is designed to make the synchronous buck converter stable over the input line, output load, and temperature with specified output capacitors and inductors. In addition, the high bandwidth control loop design allows for fast load and line transient response.

CURRENT LIMITING AND SHORT-CIRCUIT PROTECTION

Both buck converters and the LDO have a current limit feature that allows the ADP5020 to protect itself and any external components during overload and short-circuit conditions. The upper switch pMOSFET turns off if peak current exceeds the limit. The nMOSFET is turned on for a longer period until inductor current drops to 0 A to prevent thermal runaway.

SYNCHRONIZATION

The device has several methods of synchronizing an external clock with the switching regulators. If the external clock is 9.6 MHz, Bit 6 (SYNC_9P6) in the OPERATIONAL_CONTROL register (Address 0x04) must be set to 1, and Bit 5 (SYNC_19P2) must be set to 0. This operation divides the external clock by 3 before it is applied to the switching regulator clock. If the external clock is 19.2 MHz, Bit 5 (SYNC_19P2) in Address 0x04 must be set to 1, and Bit 6 (SYNC_9P6) must be set to 0. This opera-tion divides the external clock by 6 before it is applied to the switching regulator clock. The synchronous clock can be dc- or ac-coupled onto the SYNC pin. For ac coupling, Bit 4 (SYNC_AC) in Address 0x04 is set to 1; for dc coupling, Bit 4 is set to 0. Operational control is performed by I²C writing to Register 0x04.

I²C INTERFACE

An internal register can be accessed using a synchronous serial interface that implements the standard I²C interface. The ADP5020 behaves as a slave device, communicating at normal speed (100 kHz) or fast speed (400 kHz).

The I²C timing specifications are shown in Table 6, and the I²C interface timing diagram is shown in Figure 3. The 7-bit slave address of the ADP5020 is shown in Table 10.

UNDERVOLTAGE LOCKOUT

The undervoltage lockout block contains the UVLO detector circuits for the battery voltage level. It also contains the status registers that are required to allow the external application processor to determine the status of the power supplies. The most important function of the UVLO circuit is to prevent converter operation if the supply voltage is too low. The UVLO falling condition (when the battery voltage decreases from the operating range level) is set to a typical value of 2.0 V, whereas the UVLO rising condition (when the supply voltage increases from zero) is typically 2.2 V.

THERMAL SHUTDOWN

The thermal shutdown block (TSD) prevents device damage if the die temperature reaches a level greater than 150°C. When the thermal shutdown limit is reached, the regulator disables the outputs, while waiting for the die to cool down (typically, to 30°C below the thermal shutdown threshold). There are two distinct conditions to be considered when recovering from a thermal shutdown condition:

- The EN pin is low. If the EN pin is low and the device is operating in I²C command mode, the outputs remain disabled until the application processor initializes the parameters and performs the sequencing of the regulators. The application processor can sense a generic failure condition by detecting a missing acknowledge bit following an I²C command. When a thermal shutdown condition occurs, Bit 0 (TSD) in the OPERATIONAL_CONTROL register (Address 0x04) is latched to 1 so that the processor can recognize the origin of the failure when resuming from a fault condition. When the TSD bit is set, the application processor must clear this bit to activate the regulators. If the TSD bit is not cleared, writing to the regulator enable bits, Bits[7:4] (BK1_EN, BK2_EN, LDO_EN, and EN_ALL), in the REG_CONTROL_STATUS register (Address 0x03) has no effect. The application processor can also force Bit 0 (TSD) to 1. In this case, the operation proceeds as though a thermal shutdown condition has occurred.
- The EN pin is high. If the EN pin is high, the device resumes operation automatically from a thermal shutdown condition. The device resumes performing the predefined regulator sequence without processor intervention. Bit 0 (TSD) in the OPERATIONAL_CONTROL register (Address 0x04) is set to indicate that a thermal shutdown has occurred, and it is not possible to activate the regulators using an I²C command unless the host sets the TSD bit to 0.

CONTROL REGISTERS

DEVICE ADDRESS

Following a start condition, the bus master must send the address of the slave it is accessing. The slave address for the ADP5020 is shown in Table 10. The Bit 0 defines the operation to be performed. When this bit is set to Logic 1, a read operation is selected. When this bit is set to Logic 0, a write operation is selected.

Table 10. Slave Address

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	R/W
0	0	1	0	1	0	0	1 or 0

REGISTER MAP

Table 11.

Address	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0x00	Revision	MAJ[2:0]			MIN[2:0]			OPT[1:0]	
0x01	BUCK1_VSEL	Reserved[7:3]					BK1_VSEL[2:0]		
0x02	BUCK2_LDO_VSEL	BK2_VSEL[3:0]				LDO_VSEL[3:0]			
0x03	REG_CONTROL_STATUS	BK1_EN	BK2_EN	LDO_EN	EN_ALL	BK1_ PGOOD	BK2_ PGOOD	LDO_ PGOOD	FORCE_XS
0x04	OPERATIONAL_CONTROL	Reserved	SYNC_9P6	SYNC_19P2	SYNC_ AC	BK1_ XSHTDN	BK2_ XSHTDN	LDO_ XSHTDN	TSD
0x05	EN_CONTROL	Reserved[7:2]						ENO_HIZ_ BAR	ENO_DRV
0x06 to 0x0F	Reserved								

REGISTER DESCRIPTIONS

User Accessible Registers

Table 12. Revision Register, Address 0x00

Bit	Bit Name	Access	Default	Description
[7:5]	MAJ[2:0]	R	N/A	Major revision bits. Used to electronically ID the device version.
[4:2]	MIN[2:0]	R	N/A	Minor revision bits. Used to electronically ID the device version.
[1:0]	OPT[1:0]	R	N/A	Option bits. Used to electronically ID the option (multiple options on same device family).

Table 13. BUCK1_VSEL Register, Address 0x01

Bit	Bit Name	Access	Default	Description
[7:3]	Reserved	N/A	N/A	Reserved.
[2:0]	BK1_VSEL[2:0]	R/W	Fuse	Sets the voltage output level of the Buck 1 regulator. Preloads on power-up with values stored in fuses. Note that this value can be edited by the user in an application. 000 = 2.5 V. 001 = 2.8 V. 010 = 2.9 V. 011 = 3.0 V. 100 = 3.2 V. 101 = 3.3 V (default). 110 = 3.7 V. 111 = reserved.

Table 14. BUCK2_LDO_VSEL Register, Address 0x02

Bit	Bit Name	Access	Default	Description
[7:4]	BK2_VSEL[3:0]	R/W	Fuse	Sets the voltage output level of the Buck 2 regulator. Preloads on power-up with values stored in fuses. Note that this value can be edited by a user in an application. 0000 = 1.1 V. 0001 = 1.1 V. 0010 = 1.1 V. 0011 = 1.1 V. 0100 = 1.1 V. 0101 = 1.1 V. 0110 = 1.1 V. 0111 = 1.1 V. 1000 = 1.1 V. 1001 = 1.2 V (default). 1010 = 1.3 V. 1011 = 1.4 V. 1100 = 1.5 V. 1101 = 1.6 V. 1110 = 1.7 V. 1111 = 1.8 V.
[3:0]	LDO_VSEL[3:0]	R/W	Fuse	Sets the voltage output level of the LDO regulator. Preloads on power-up with values stored in fuses. Note that this value can be edited by the user in an application. 0000 = 1.8 V (default). 0001 = 1.9 V. 0010 = 2.0 V. 0011 = 2.1 V. 0100 = 2.2 V. 0101 = 2.3 V. 0110 = 2.4 V. 0111 = 2.5 V. 1000 = 2.6 V. 1001 = 2.7 V. 1010 = 2.8 V. 1011 = 2.9 V. 1100 = 3.0 V. 1101 = 3.1 V. 1110 = 3.2 V. 1111 = 3.3 V.

Table 15. REG_CONTROL_STATUS Register, Address 0x03

Bit	Bit Name	Access	Default	Description
7	BK1_EN	R/W	0	1 = turns on the Buck 1 regulator. If the EN pin is high, the sequencer is ignored.
6	BK2_EN	R/W	0	1 = turns on the Buck 2 regulator. If the EN pin is high, the sequencer is ignored.
5	LDO_EN	R/W	0	1 = turns on the LDO regulator. If the EN pin is high, the sequencer is ignored.
4	EN_ALL	R/W	0	1 = turns on all regulators, following sequencer programming. BK1_EN, BK2_EN, and LDO_EN must all be set to 0 for this bit to function.
3	BK1_PGOOD	R	0	Power good status for Buck 1. 1 = power good (POK). 0 = fail.
2	BK2_PGOOD	R	0	Power good status for Buck 2. 1 = power good (POK). 0 = fail.
1	LDO_PGOOD	R	0	Power good status for LDO. 1 = power good (POK). 0 = fail.
0	FORCE_XS	R/W	0	1 = the XSHTDN pin is controlled by the power good signals. 0 = the XSHTDN pin is held low unless the EN pin is high, regardless of regulator status. If EN is high, this bit is ignored in controlling the XSHTDN pin (acts as if FORCE_XS = 1).

Table 16. OPERATIONAL_CONTROL Register, Address 0x04

Bit	Bit Name	Access	Default	Description
7	Reserved	N/A	N/A	Reserved.
6	SYNC_9P6[1]	R/W	0	1 = a 9.6 MHz clock is on the SYNC pin. The SYNC frequency is divided by 3 and used as clock frequency for switching regulators.
5	SYNC_19P2[1]	R/W	0	1 = a 19.2 MHz clock is on the SYNC pin. The SYNC frequency is divided by 6 and used as clock frequency for switching regulators. 1 for both SYNC_9P6 and SYNC_19P2 = invalid setting. 0 for both SYNC_9P6 and SYNC_19P2 = clock synchronization is disabled, and the device operates with the 3 MHz internal clock.
4	SYNC_AC[1]	R/W	0	1 = the ac path is used for the SYNC input. 0 = the dc path is used (default).
3	BK1_XSHTDN	R/W	Fuse	0 = power good for Buck 1 must be high for XSHTDN to go high (default). 1 = Buck 1 power good is ignored.
2	BK2_XSHTDN	R/W	Fuse	0 = power good for Buck 2 must be high for XSHTDN to go high (default). 1 = Buck 2 power good is ignored.
1	LDO_XSHTDN	R/W	Fuse	0 = LDO power good must be high for XSHTDN to go high (default). 1 = LDO power good is ignored.
0	TSD	R/W	0	Shows a latched status of a thermal shutdown (TSD) event. 1 = TSD is active. Must be cleared to 0 by user program to enable the regulators. If this bit remains set to 1, regulator activation is inhibited, as in a thermal shutdown event.

[1] The SYNC selection bits (SYNC_AC, SYNC_9P6, and SYNC_19P2) cannot be changed while a switching regulator is running.

Table 17. EN_CONTROL Register, Address 0x05

Bit	Bit Name	Access	Default	Description
[7:2]	Reserved	N/A	N/A	Reserved.
1	ENO_HIZ_BAR	R/W	0	0 = the EN/GPIO pin is in high impedance, and the EN function is selected. 1 = GPIO output is selected, and the EN function is ignored.
0	ENO_DRV	R/W	0	Active only when ENO_HIZ_BAR = 1 (GPIO). 0 = GPIO output is set to low. 1 = GPIO output is set to high.

POWER-UP/POWER-DOWN SEQUENCE

SEQUENCER

The sequencer is enabled after a low-to-high transition of the enable pin (EN). When EN is low or programmed as an output, the sequencing is controlled and timed by the application processor via the I²C commands.

Each regulator inside the ADP5020 is controlled by the sequencer block. The sequencer is factory programmed with a default turn-on sequence that determines the activation order of the regulators. The default activation order is listed as follows:

1. Buck 1
2. LDO
3. Buck 2

A low-to-high transition of the EN pin, when programmed as an input, or an I²C command setting Bit 4 (EN_ALL) in the REG_CONTROL_STATUS register (Address 0x03), starts the sequencer.

The activation delay for the first regulator is determined by the turn-on delay of the band gap, oscillator, and other internal circuits. Therefore, the first regulator cannot be activated before a typical 5 ms delay time has elapsed. Delays between the first and second regulator and from the second to third regulator are hard coded to a specific time (t_{REG1}, t_{REG2}, and t_{REG3}). The delay time starts from the moment a regulator has reached the power good threshold (see Figure 22).

DEFAULT POWER-ON SEQUENCE WITH EN PIN

Figure 22 shows the default regulator sequencing after a low-to-high transition of the EN pin. The regulator order is factory programmed and can be changed for specific applications. The power good signal (POK) turns to high if the regulator voltage is ≥80% of the target voltage. The second regulator checks the POK signal of the first regulator and waits the preset delay time (t_{REG2}) before turning on. In addition to changing the regulator order, it is also possible to disable the unused regulator. Additional fuses allow disabling of the association between XSHTDN generation and the POK signal for a specific regulator. The power good signal of an unused regulator must be masked, via dedicated fuse and user registers, to prevent the XSHTDN output from being forced low. A host processor controller, connected to the I²C bus, can override the masking fuses by accessing the following bits in the OPERATIONAL_CONTROL register (Address 0x04): Bit 3 (BK1_XSHTDN, for Buck 1), Bit 2 (BK2_XSHTDN, for Buck 2), and Bit 3 (LDO_XSHTDN, for LDO). Writing 0 to these register bits requires that power good be true to release the XSHTDN pin to high. Writing 1 to these bits causes the regu-lator state to be ignored, and XSHTDN must depend on the active and unmasked regulators.

The regulators can also be activated individually via the I²C commands. The host specifies which regulator is to be turned on or off by setting or clearing the following selection bits in the REG_CONTROL_STATUS register (Address 0x03): Bit 7 (BK1_EN), Bit 6 (BK2_EN), or Bit 5 (LDO_EN). When the regulators are individually activated by I²C commands, the auto sequencing is disabled and the host controls the turn-on and turn-off timing (see Figure 26).

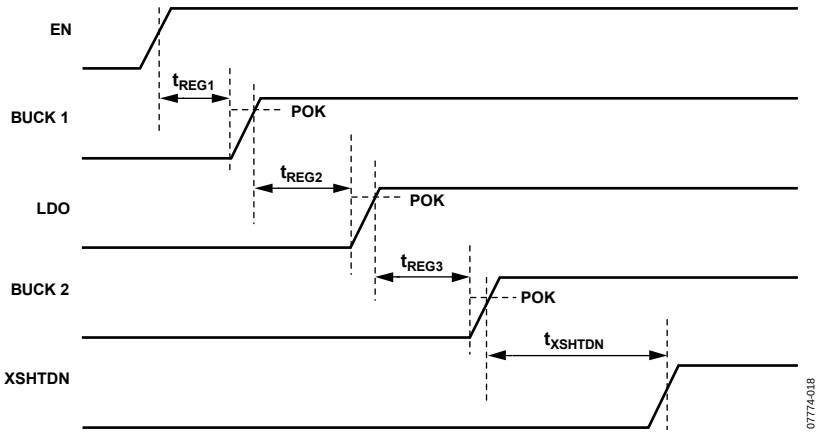

Figure 22. Automatic Sequencing with EN Low-to-High Transition

Activation Waveforms

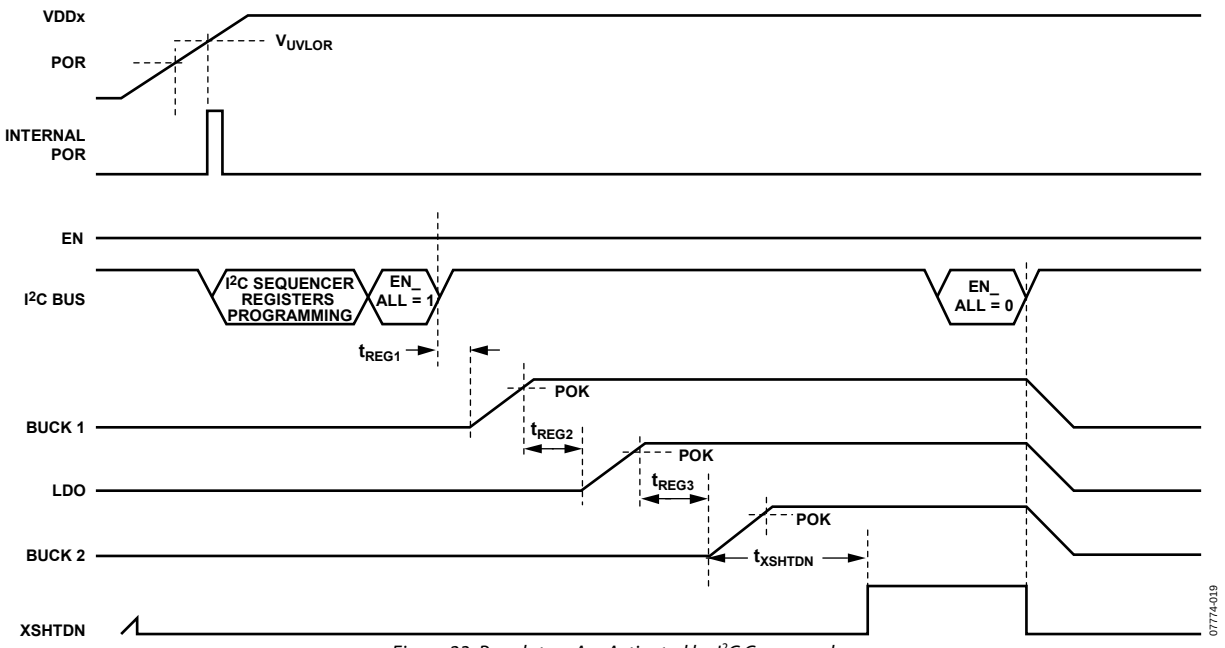

Figure 23. Regulators Are Activated by I²C Command

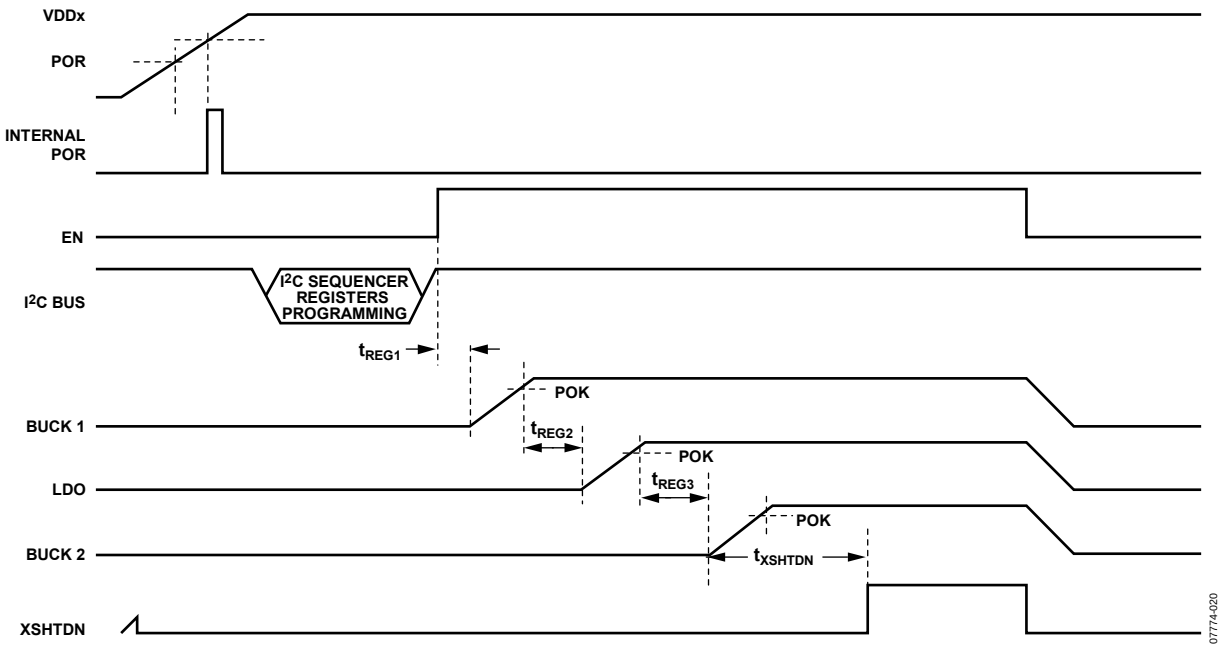

Figure 24. Activation Command Using the EN Pin

When activated through the EN pin, the sequencer is affected only by the I²C commands that set or clear the regulator power good masking bits: Bit 3 (BK1_XSHTDN), Bit 2 (BK2_XSHTDN), and Bit 1 (LDO_XSHTDN) in the OPERATIONAL_CONTROL register (Address 0x04). See the Default Power-On Sequence with EN Pin section for more information. The sequence order of the regulators is factory programmed through fuses, but the delays between the regulators (t_{REG1}, t_{REG2}, and t_{REG3}) are fixed and cannot be changed.

The EN_ALL bit (Bit 4) in the REG_CONTROL_STATUS regi-ster (Address 0x03) has the same functionality as the EN pin. The sequencer has an antiglitch function that allows it to ignore supply voltage dip if glitch time is less than 50 µs (see Figure 25).

POWER-ON SEQUENCE USING THE I²C INTERFACE

When the EN pin is low, the regulator sequence is controlled by the application processor sending I²C commands to control the activation. When Bit 4 (EN_ALL) in the REG_CONTROL_STATUS register (Address 0x03) is set to 1, the regulator sequence is as follows:

1. Buck 1
2. LDO
3. Buck 2

This sequence can be factory programmed through fuses. Unused regulators can also be fuse programmed to be turned off during sequencing.

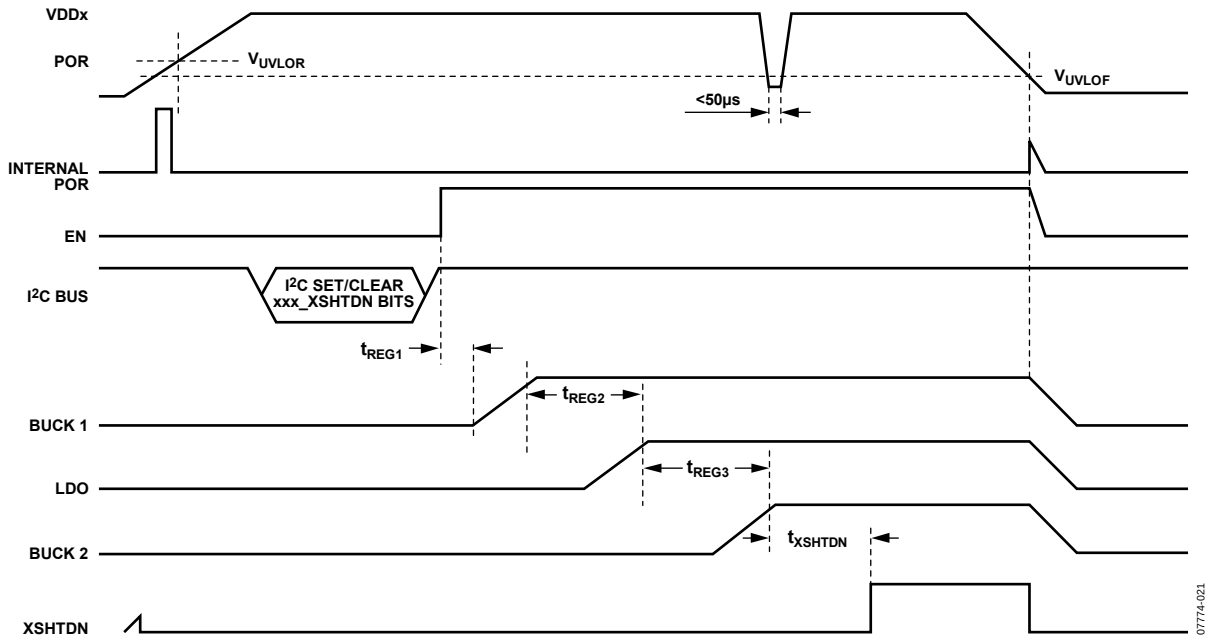

Figure 25. Activation and Power Failure Conditions

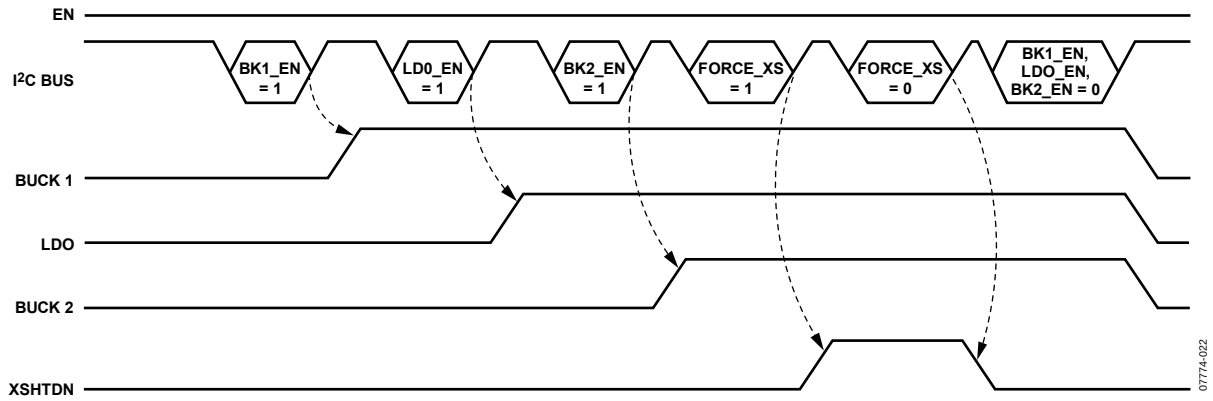

Figure 26. Individual Activation Through I²C Commands

The application processor, together with the regulator power good signal, controls the XSHTDN pin, as shown in Table 18. After a regulator is enabled and no failure condition is detected (power good = 1 in Bits[3:1] of the REG_CONTROL_STATUS register, Address 0x03), the level of the XSHTDN pin is controlled by Bit 0 (FORCE_XS) in the REG_CONTROL_STATUS register. Therefore, the application processor can write to this register to gain control over the XSHTDN pin. However, if the EN signal is high, the level on the XSHTDN pin depends on the power good condition of the regulator.

Table 18. Truth Table

EN Pin	I²C Regulator Enable	Power Good	FORCE_XS	XSHTDN Pin
0	0	0	X[1]	0
0	1	X[1]	0	0
0	1	0	1	0
0	1	1	1	1
1	X[1]	1	X[1]	1
1	X[1]	0	X[1]	0

[1] X = don't care.

POWER-UP/POWER-DOWN STATE FLOW

When the device is enabled, the UVLO circuit constantly monitors the supply voltage. If the supply voltage falls below the V_{UVLOF} threshold, typically 2.0 V, the regulators are immediately turned off. All the internal analog circuits are then disabled to save power, except the power-on reset (POR) circuit, which detects if the supply voltage is dropping. If the supply voltage is higher than the POR threshold, the POR circuit keeps the logic circuits operating properly and retains the internal values of the registers. This POR threshold is set to approximately 1.4 V.

If the supply voltage goes below the V_{UVLOR} threshold, but not below the POR threshold, the registers are preserved. If the supply voltage returns to the normal operating level (above V_{UVLOR}), a new activation does not require initialization of the registers. However, if the supply voltage goes below the POR level, the device is held in reset state. When the input voltage resumes the proper operating level, the host controller must reload the registers.

The additional current required to keep the POR monitoring circuits alive during UVLO is estimated to be approximately 1 µA.

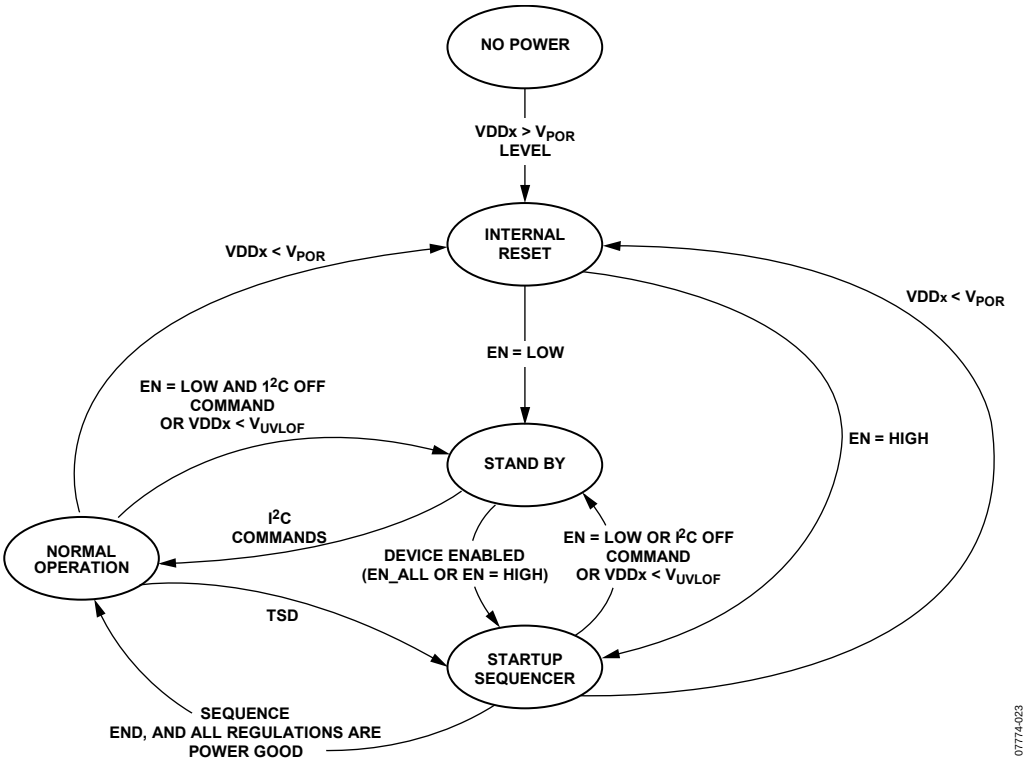

Figure 27. State Flow

APPLICATIONS INFORMATION

POWER GOOD STATUS

The ADP5020 constantly monitors the operating conditions. When a regulator is activated, it checks if the output voltage level is above 80% (the power good threshold) of the nominal level for that output. If the output voltage does not reach the power good threshold, one of the three power good status bits in the REG_CONTROL_STATUS register (Address 0x03) is cleared. If the output voltage reaches the power good threshold, one of the power good status bits in the REG_CONTROL_STATUS register is set to 1. The REG_CONTROL_STATUS register contains the following three power good bits: BK1_PGOOD for the Buck 1 output (Bit 3), BK2_PGOOD for the Buck 2 output (Bit 2), and LDO_PGOOD for the LDO output (Bit 1).

XSHTDN LOGIC

In addition to the power good information for each enabled regulator, an XSHTDN signal is generated, as shown in Table 18. If one or more regulators are unused in a specific application, the masking bits for the disabled regulator, which are fuse programmable and I²C programmable after device startup, must be set to 1 to mask the status of the power good signal. Besides having the masking bits predefined through factory-programmed fuses (necessary only for operation with the EN signal), the ADP5020 provides three masking bits that are accessible through the I²C interface. These bits are located in the OPERATIONAL_CONTROL register (Address 0x04), where the BK1_XSHTDN bit (Bit 3) is the mask (if set to 1) for Buck 1, the BK2_XSHTDN bit (Bit 2) is the mask (if set to 1) for Buck 2, and the LDO_XSHTDN bit (Bit 3) is the mask (if set to 1) for the LDO. Additional failures that are verified are the input (VDDA) undervoltage condition, as described in the Undervoltage Lockout section; and an overtemperature condition of the die, as described in the Thermal Shutdown section. As soon as one of these conditions occurs, the active regulators are immediately turned off, and the XSHTDN pin is set to 0.

COMPONENTS SELECTION

Buck Inductor

The buck inductor is chosen to meet output ripple current and ripple voltage requirements with minimum size. The fast load transient response and wide frequency bandwidth are also important factors for inductor selection. The minimum inductance of the buck converter is derived from the following equation:

$$L_{MINBUCK} = \frac{(V_{INMAX} - V_{OUT}) \times V_{OUT}}{V_{INMAX} \times f_{SW} \times r \times I_{OUT}} \quad (1)$$

where:

V_{INMAX} is the maximum input supply voltage.
V_{OUT} is the regulator output voltage in the buck converter.
f_{SW} is the converter switching frequency.
r is the inductor ripple factor, which is selected as 30%.

Peak inductor current is calculated in the following equation:

$$I_{LMAX} = I_{OUT} + 0.5 \times r \times I_{OUT} \quad (2)$$

The calculated minimum Buck 2 inductor value is 2.2 µH. The maximum peak inductor current is 325 mA. A ceramic inductor such as the Taiyo Yuden BRL2012T2R2M, with a 600 mA saturation current in a 2 mm × 1.2 mm × 1 mm package, can be used. For the Buck 1 converter, the calculated minimum inductance is 2.2 µH, with maximum peak current of 690 mA. A ceramic inductor such as the Taiyo Yuden BRL2518T2R2M, with a 1 A saturation current in a 2.5 mm × 1.8 mm × 1.2 mm package, is recommended.

Input Capacitor Selection

The input capacitors are used to decouple the parasitic inductance of input wires to the converters and to reduce the input ripple voltage and the switching ac current flow to the battery rail. The capacitors are selected to support the maximum input operating voltage and the maximum rms current. The capacitance must also be large enough to ensure input stability and suppress input ripple. ESR should as small as possible to decouple the noise. MLCC ceramic capacitors are a good choice for battery-powered applications because of their high capacitance, small size, and low ESR. A 10 µF ceramic capacitor (for example, the JMK107BJ106MA-T from Taiyo Yuden) is recommended.

Output Capacitor Selection

Output capacitor selection should be based on the following three factors:

- Maximizing the control loop bandwidth of the converter with the LC filter
- Minimizing the output voltage ripple
- Minimizing the size of the capacitor

Note that the output ripple is the combination of several factors, including the inductor ripple current (ΔI_L), the ESR and ESL output capacitors, and the capacitor impedance at the switching frequency.

In buck converters, the output ripple can be calculated as follows:

$$\Delta V_{OUTRIPPLE} = \Delta I_L \left(ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}} + 4 \times ESL \times f_{SW} \right)$$

$$\Delta I_L = r \times I_{OUT}$$

Capacitor manufacturer data sheets show the ESR and ESL value. In real-life applications, the ripple voltage may be higher because the equations provided in this data sheet do not consider parameters such as board/package parasitic inductance and capacitance. The minimum recommended capacitance is no less than 4.0 µF for Buck 1, 2.0 µF for Buck 2, and 0.4 µF for the LDO.

LDO INPUT FILTER

To improve the LDO input-to-output ripple suppression in the critical switching frequency range of the buck converters, it may be necessary to add an LC filter tuned to 1 MHz, as shown in Figure 28. Additional tests and simulation must be performed to assess if this filter is necessary.

The filter resonance frequency is determined by the following equation:

$$f_{LC} = \frac{1}{2 \times \pi \times \sqrt{L3 \times C8}} \quad (3)$$

where L3 = 250 nH, assuming that f_{LC} = 1 MHz and C8 = 100 nF. The inductor must be able to withstand the LDO load current, including the overload condition, which is limited to 400 mA.

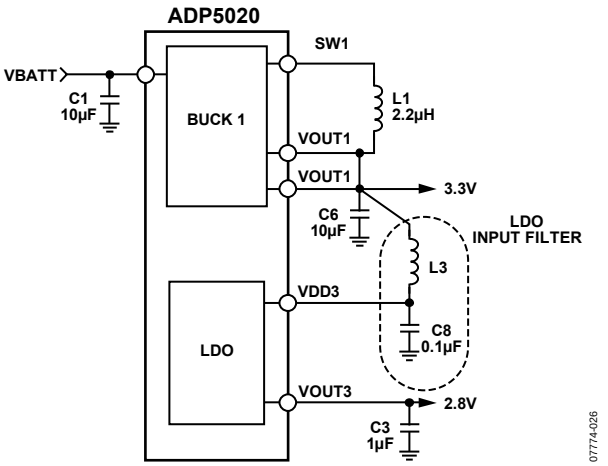

Figure 28. Optional LDO Input Filter

LAYOUT RECOMMENDATIONS

APPLICATIONS SCHEMATIC

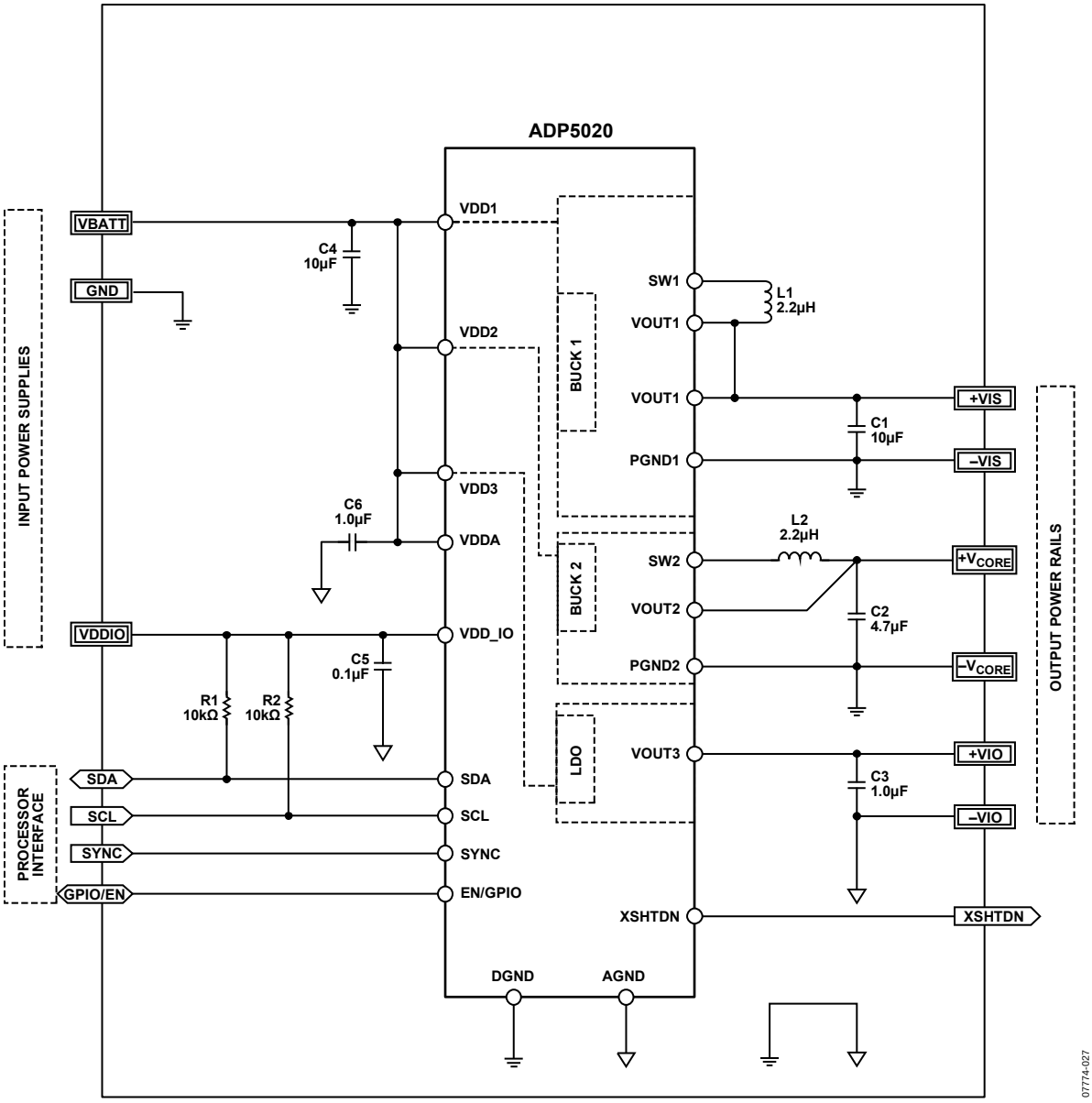

Figure 29. Schematic for Camera Module Applications

PCB BOARD LAYOUT RECOMMENDATIONS

- Place the input and output capacitors, C1, C2, C3, C4, and C5, as close as possible to the respective ADP5020 pin, and make the grounding connection to the ADP5020 ground pins as short as possible.
- Connect C3, C5, and C6 to the analog ground, and connect C1, C2, and C4 to the power ground.
- Place the L1 and L2 inductors as close as possible to the respective output pins.
- The power and analog ground planes are recommended to keep the noise low. Use one layer for power ground and one layer for analog ground. Tie the power and analog grounds at a single point.
- Use wide traces to connect the inductor and the input and output capacitors.
- Add the L3 inductor and the C8 capacitor, if needed, to improve the LDO noise rejection at the switching frequency of the Buck 1 regulator (3 MHz) because the LDO PSRR typically degrades at higher frequencies. If switching noise is not an issue, remove the L3 inductor.

EXTERNAL COMPONENT LIST

Table 19. Recommended External Components List

Reference Designator	Description	Size	Proposed Vendor	Vendor Part No.
C1, C4	10 µF, X5R, 6.3 V, ±20%	0603	Murata	GRM188R60J106M
C1, C4	10 µF, X5R, 6.3 V, ±20%	0603	Taiyo Yuden	JMK107BJ106MA
C2	4.7 µF, X5R, 6.3 V, ±10%	0603	Murata	GRM188R60J475K
C3	1.0 µF, X5R, 6.3 V, ±10%	0603	Murata	GRM155R60J105K
C5	0.1 µF, X5R, 10 V, ±10%	0402	Murata	GRM155R61A104K
C6	1.0 µF, X5R, 6.3 V, ±10%	0603	Murata	GRM155R60J105K
L1	2.2 µH, DCR = 0.13 Ω, IDC = 1 A	2.5 mm × 1.8 mm × 1.2 mm	Taiyo Yuden	BRL2518T2R2M
L2	2.2 µH, DCR = 0.23 Ω, IDC = 0.53 A	2.0 mm × 1.2 mm × 1.0 mm	Taiyo Yuden	BRL2012T2R2M
R1, R2	10 kΩ, 1%, thick film resistor	0402	KOA Speer Electronics	RK73H1ETTP1002F

OUTLINE DIMENSIONS

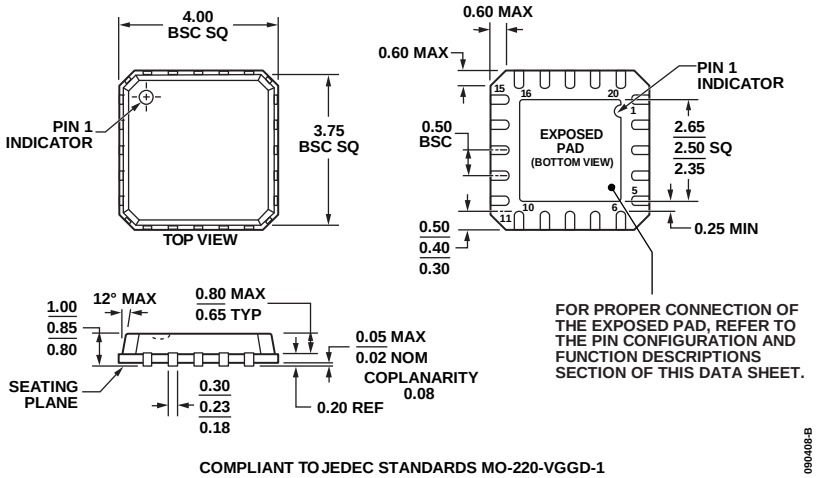

Figure 30. 20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-20-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADP5020ACPZ-R7[1]	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-20-4
ADP5020CP-EVALZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

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