



May 1993
Revised March 1999

74LVX74

Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop

General Description

The LVX74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, \bar{Q}) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

- LOW input to \bar{S}_D (Set) sets Q to HIGH level
- LOW input to \bar{C}_D (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on \bar{C}_D and \bar{S}_D makes both Q and \bar{Q} HIGH

Features

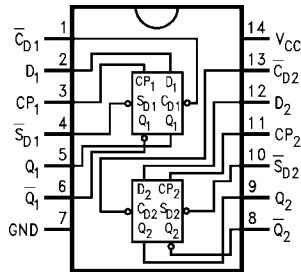
- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Ordering Code:

| Order Number | Package Number | Package Description |
|--------------|----------------|--|
| 74LVX74M | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow |
| 74LVX74SJ | M14D | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74LVX74MTC | MTC14 | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram



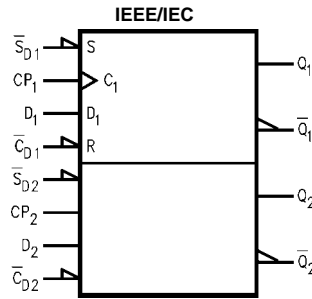
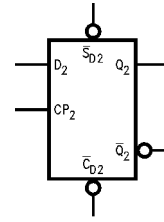
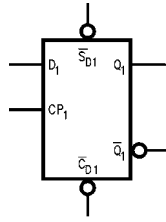
Pin Descriptions

| Pin Names | Description |
|---|---------------------|
| D ₁ , D ₂ | Data Inputs |
| CP ₁ , CP ₂ | Clock Pulse Inputs |
| \bar{C}_D1 , \bar{C}_D2 | Direct Clear Inputs |
| \bar{S}_D1 , \bar{S}_D2 | Direct Set Inputs |
| Q ₁ , \bar{Q}_1 , Q ₂ , \bar{Q}_2 | Outputs |

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Logic Symbols



Truth Table

(Each Half)

| Inputs | | | | Outputs | |
|------------------|------------------|----|---|---------|------------------|
| \overline{S}_D | \overline{C}_D | CP | D | Q | \overline{Q} |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H | H |
| H | H | ↗ | H | H | L |
| H | H | ↗ | L | L | H |
| H | H | L | X | Q_0 | \overline{Q}_0 |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 ↗ = LOW-to-HIGH Clock Transition
 $Q_0(\overline{Q}_0)$ = Previous Q(\overline{Q}) before LOW-to-HIGH Transition of Clock

Absolute Maximum Ratings(Note 1)

| | |
|--------------------------------------|--------------------------|
| Supply Voltage (V_{CC}) | -0.5V to +7.0V |
| DC Input Diode Current (I_{IK}) | |
| $V_I = -0.5V$ | -20 mA |
| DC Input Voltage (V_I) | -0.5V to 7V |
| DC Output Diode Current (I_{OK}) | |
| $V_O = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | +20 mA |
| DC Output Voltage (V_O) | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Source | |
| or Sink Current (I_O) | ± 25 mA |
| DC V_{CC} or Ground Current | |
| (I_{CC} or I_{GND}) | ± 50 mA |
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| Power Dissipation | 180 mW |

Recommended Operating Conditions (Note 2)

| | |
|--|--------------------|
| Supply Voltage (V_{CC}) | 2.0V to 3.6V |
| Input Voltage (V_I) | 0V to 5.5V |
| Output Voltage (V_O) | 0V to V_{CC} |
| Operating Temperature (T_A) | -40°C to +85°C |
| Input Rise and Fall Time ($\Delta t/\Delta V$) | 0 ns/V to 100 ns/V |

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

| Symbol | Parameter | V_{CC} | $T_A = +25^\circ C$ | | | $T_A = -40^\circ C$ to $+85^\circ C$ | | Units | Conditions |
|----------|------------------------------|----------|---------------------|-----|-----------|--------------------------------------|-----------|---------|---|
| | | | Min | Typ | Max | Min | Max | | |
| V_{IH} | HIGH Level Input Voltage | 2.0 | 1.5 | | | 1.5 | | V | |
| | | 3.0 | 2.0 | | | 2.0 | | | |
| | | 3.6 | 2.4 | | | 2.4 | | | |
| V_{IL} | LOW Level Input Voltage | 2.0 | | | 0.5 | | 0.5 | V | |
| | | 3.0 | | | 0.8 | | 0.8 | | |
| | | 3.6 | | | 0.8 | | 0.8 | | |
| V_{OH} | HIGH Level Output Voltage | 2.0 | 1.9 | 2.0 | | 1.9 | | V | $V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -50 \mu A$ $I_{OH} = -50 \mu A$ $I_{OH} = -4 mA$ |
| | | 3.0 | 2.9 | 3.0 | | 2.9 | | | |
| | | 3.0 | 2.58 | | | 2.48 | | | |
| V_{OL} | LOW Level Output Voltage | 2.0 | | 0.0 | 0.1 | | 0.1 | V | $V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 50 \mu A$ $I_{OL} = 50 \mu A$ $I_{OL} = 4 mA$ |
| | | 3.0 | | 0.0 | 0.1 | | 0.1 | | |
| | | 3.0 | | | 0.36 | | 0.44 | | |
| I_{IN} | Input Leakage Current | 3.6 | | | ± 0.1 | | ± 1.0 | μA | $V_{IN} = 5.5V$ or GND |
| I_{CC} | Quiescent Supply Current | 3.6 | | | 2.0 | | 20.0 | μA | $V_{IN} = V_{CC}$ or GND |

Noise Characteristics (Note 3)

| Symbol | Parameter | V_{CC} (V) | $T_A = 25^\circ C$ | | Units | C_L (pF) |
|-----------|--|--------------|--------------------|-------|-------|------------|
| | | | Typ | Limit | | |
| V_{OLP} | Quiet Output Maximum Dynamic V_{OL} | 3.3 | 0.3 | 0.5 | V | 50 |
| V_{OLV} | Quiet Output Minimum Dynamic V_{OL} | 3.3 | -0.3 | -0.5 | V | 50 |
| V_{IHD} | Minimum High Level Dynamic Input Voltage | 3.3 | | 2.0 | V | 50 |
| V_{ILD} | Maximum Low Level Dynamic Input Voltage | 3.3 | | 0.8 | V | 50 |

Note 3: Input $t_r = t_f = 3$ ns

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| AC Electrical Characteristics | | | | | | | | | |
|-------------------------------|--|---------------------|------------------------|------|------|---------------------------------|------|-------|---------------------|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | | T _A = -40°C to +85°C | | Units | C _L (pF) |
| | | | Min | Typ | Max | Min | Max | | |
| t _{PLH} | Propagation Delay | 2.7 | | 7.3 | 15 | 1.0 | 18.5 | ns | 15 |
| t _{PHL} | CP _n to Q _n or \bar{Q}_n | 3.3 ± 0.3 | | 9.8 | 18.5 | 1.0 | 22 | | 50 |
| | | | | 5.7 | 9.7 | 1.0 | 11.5 | | 15 |
| | | | | 8.2 | 13.2 | 1.0 | 15 | | 50 |
| t _{PLH} | Propagation Delay | 2.7 | | 8.4 | 15.6 | 1.0 | 18.5 | ns | 15 |
| t _{PHL} | \bar{C}_{Dn} to \bar{S}_{Dn} to Q _n or \bar{Q}_n | 3.3 ± 0.3 | | 10.9 | 19.1 | 1.0 | 22 | | 50 |
| | | | | 6.6 | 10.1 | 1.0 | 12 | | 15 |
| | | | | 9.1 | 13.6 | 1.0 | 15.5 | | 50 |
| t _W | CP _n or \bar{C}_{Dn} or \bar{S}_{Dn} Pulse Width | 2.7 | 8.5 | | | 10 | | ns | |
| | | 3.3 ± 0.3 | 6 | | | 7 | | | |
| t _S | Setup Time D _n to CP _n | 2.7 | 8.0 | | | 9.5 | | ns | |
| | | 3.3 ± 0.3 | 5.5 | | | 6.5 | | | |
| t _H | Hold Time D _n to CP _n | 2.7 | 0.5 | | | 0.5 | | ns | |
| | | 3.3 ± 0.3 | 0.5 | | | 0.5 | | | |
| t _{REC} | Recovery Time \bar{C}_{Pn} or \bar{S}_{Dn} to CP _n | 2.7 | 6.5 | | | 7.5 | | ns | |
| | | 3.3 ± 0.3 | 5.0 | | | 5.0 | | | |
| f _{MAX} | Maximum Clock Frequency | 2.7 | 55 | 135 | | 50 | | MHz | 15 |
| | | 3.3 ± 0.3 | 45 | 60 | | 40 | | | 50 |
| | | | 95 | 145 | | 80 | | | 15 |
| | | | 60 | 85 | | 50 | | | 50 |
| t _{OSLH} | Output to Output Skew | 2.7 | | | 1.5 | | 1.5 | ns | 50 |
| t _{OSHL} | (Note 4) | 3.3 | | | 1.5 | | 1.5 | | |

Note 4: Parameter guaranteed by design. t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|

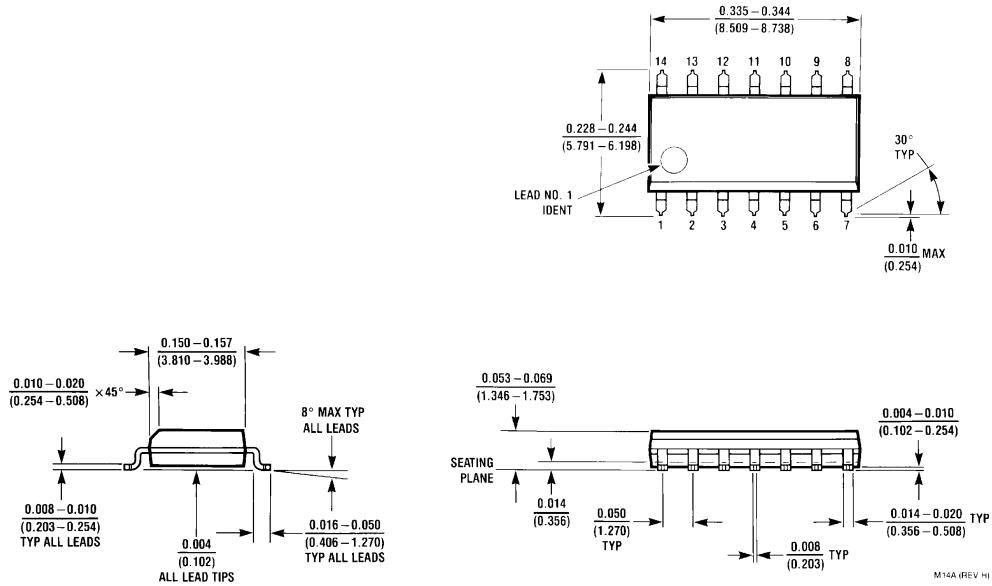
Capacitance

| Symbol | Parameter | T _A = +25°C | | | T _A = -40°C to +85°C | | Units |
|-----------------|---|------------------------|-----|-----|---------------------------------|-----|-------|
| | | Min | Typ | Max | Min | Max | |
| C _{IN} | Input Capacitance | | 4 | 10 | | 10 | pF |
| C _{PD} | Power Dissipation Capacitance (Note 5) | | 25 | | | | pF |

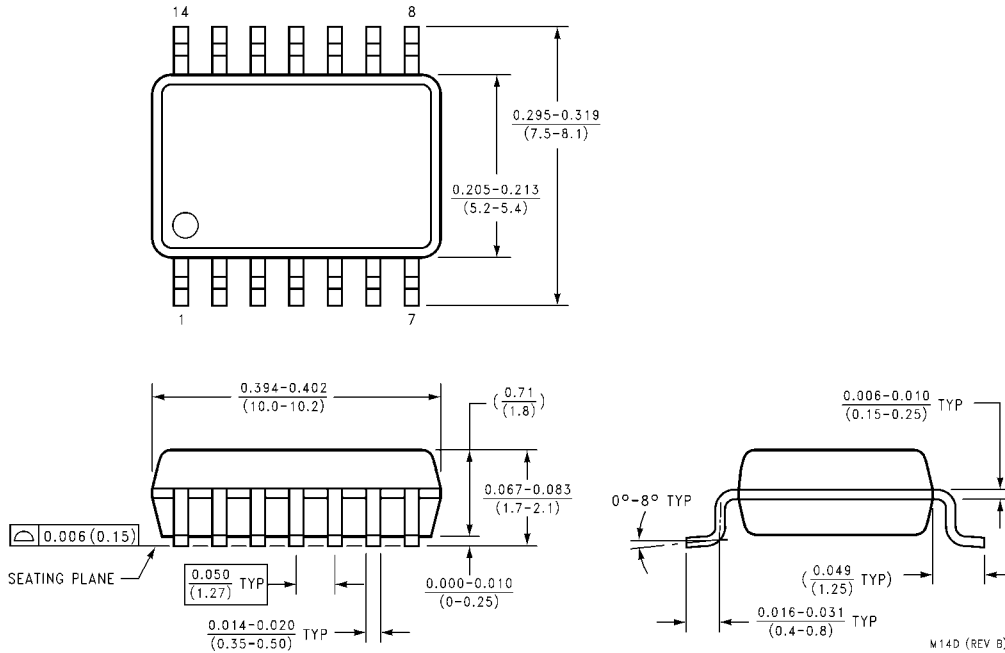
Note 5: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

$$\text{Average operating current can be obtained by the equation: } I_{CC(\text{opr.})} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{2 \text{ (per F/F)}}$$

Physical Dimensions inches (millimeters) unless otherwise noted

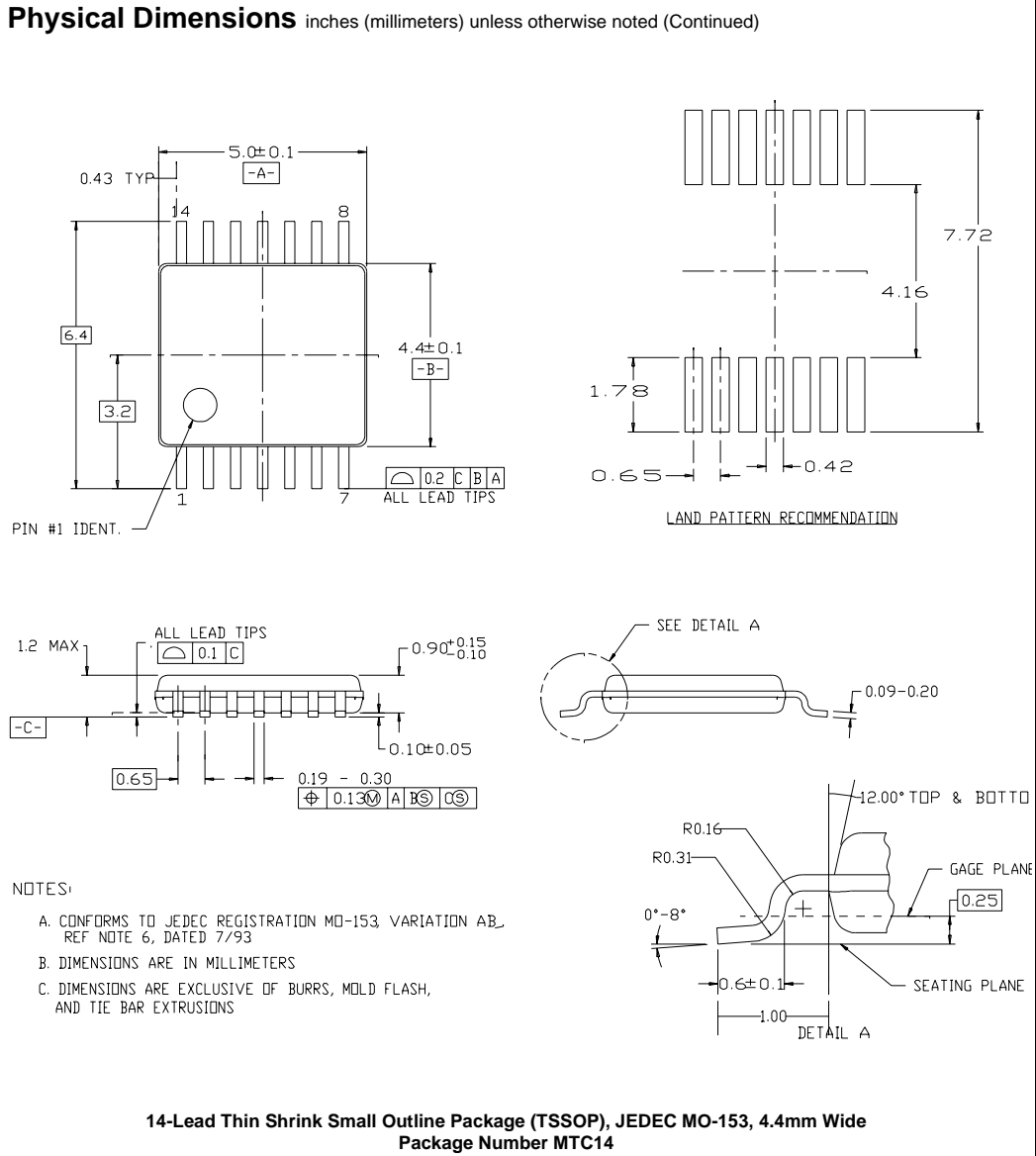


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Package Number M14A



14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M14D

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