

Absolute Maximum Ratings (Note 1)

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If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales Office/
Distributors for availability and specifications.

ESD Tolerance (Note 2)

Human Body Model 2000V

Machine Model 200V

 V_S $\pm 6V$ I_{IN} (Input Pins) ± 20 mA I_{OUT} (Note 3)Input Voltage Range V^- to V^+ Maximum Junction Temperature $+150^\circ C$

Storage Temperature Range

 $-65^\circ C$ to $+150^\circ C$

Soldering Information

Infrared or Convection (20 sec.)

 $235^\circ C$

Wave Soldering (10 sec.)

 $260^\circ C$ **Operating Ratings** (Note 1)

Temperature Range (Note 4)

 $-40^\circ C$ to $+85^\circ C$

Supply Voltage Range

 $\pm 3V$ to $\pm 5.5V$

Thermal Resistance

 θ_{JA} θ_{JC}

64-Pin Exposed Pad TQFP

 $27^\circ C/W$ $0.82^\circ C/W$ **$\pm 3.3V$ Electrical Characteristics** (Note 5)

Unless otherwise specified, typical conditions are: $T_A = 25^\circ C$, $A_V = +2$, $V_S = \pm 3.3V$, $R_L = 100\Omega$; **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
Frequency Domain Performance						
SSBW	–3 dB Bandwidth	V _{OUT} = 0.5 V _{PP}		425		MHz
LSBW		V _{OUT} = 2 V _{PP} , R _L = 1 kΩ		500		
		V _{OUT} = 2 V _{PP} , R _L = 150Ω		450		
GF	0.1 dB Gain Flatness	V _{OUT} = 2 V _{PP} , R _L = 150Ω		80		MHz
DG	Differential Gain	R _L = 150Ω, 3.58 MHz/ 4.43 MHz		0.05		%
DP	Differential Phase	R _L = 150Ω, 3.58 MHz/ 4.43 MHz		0.05		deg
Time Domain Response						
t _r	Rise Time	2V Step, 10% to 90%		1.7		ns
t _f	Fall Time	2V Step, 10% to 90%		1.4		ns
OS	Overshoot	2V Step		4		%
SR	Slew Rate	4 V _{PP} , 40% to 60% (Note 6)		1700		V/μs
t _s	Settling Time	2V Step, V _{OUT} within 0.5%		9		ns
Distortion And Noise Response						
HD2	2 nd Harmonic Distortion	2 V _{PP} , 10 MHz		–76		dBc
HD3	3 rd Harmonic Distortion	2 V _{PP} , 10 MHz		–76		dBc
e _n	Input Referred Voltage Noise	>1 MHz		12		nV/√Hz
i _n	Input Referred Noise Current	>1 MHz		2		pA/√Hz
	Switching Time			16		ns
XTLK	Crosstalk	All Hostile, f = 100 MHz		–45		dBc
ISOL	Off Isolation	f = 100 MHz		–60		dBc
Static, DC Performance						
A _V	Gain		1.986	2.00	2.014	
V _{OS}	Output Offset Voltage			±3	±17	mV
TCV _{OS}	Output Offset Voltage Average Drift	(Note 10)		38		μV/°C
I _B	Input Bias Current	Non-Inverting (Note 9)		–5		μA
TCI _B	Input Bias Current Average Drift	Non-Inverting (Note 10)		-12		nA/°C
V _O	Output Voltage Range	R _L = 100Ω	±1.75	±2.1		V
V _O	Output Voltage Range	R _L = ∞ (Note 11)	+2.1 -2.05	±2.2		V
PSRR	Power Supply Rejection Ratio			45		dB
I _{CC}	Positive Supply Current	R _L = ∞		98	120	mA

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
I_{EE}	Negative Supply Current	$R_L = \infty$		92	115	mA
	Tri State Supply Current	RST Pin > 2.0V		17	25	mA
Miscellaneous Performance						
R_{IN}	Input Resistance	Non-Inverting		100		k Ω
C_{IN}	Input Capacitance	Non-Inverting		1		pF
R_O	Output Resistance Enabled	Closed Loop, Enabled		300		m Ω
R_O	Output Resistance Disabled	Disabled	1100	1300	1450	Ω
CMVR	Input Common Mode Voltage Range			± 1.3		V
I_O	Output Current	Sourcing, $V_O = 0$ V		± 50		mA
Digital Control						
V_{IH}	Input Voltage High		2.0			V
V_{IL}	Input Voltage Low				0.8	V
V_{OH}	Output Voltage High			>2.2		V
V_{OL}	Output Voltage Low			<0.4		V
T_S	Setup Time			7		ns
T_H	Hold Time			7		ns
$\pm 5V$ Electrical Characteristics (Note 5)						
Unless otherwise specified, typical conditions are: $T_A = 25^\circ\text{C}$, $A_V = +2$, $V_S = \pm 5V$, $R_L = 100\Omega$; Boldface limits apply at the temperature extremes.						
Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
Frequency Domain Performance						
SSBW	-3 dB Bandwidth	$V_{OUT} = 0.5 V_{PP}$		475		MHz
LSBW		$V_{OUT} = 2 V_{PP}$, $R_L = 1\text{ k}\Omega$		550		
		$V_{OUT} = 2 V_{PP}$, $R_L = 150\Omega$		450		
GF	0.1 dB Gain Flatness	$V_{OUT} = 2 V_{PP}$, $R_L = 150\Omega$		100		MHz
DG	Differential Gain	$R_L = 150\Omega$, 3.58 MHz/ 4.43 MHz		0.04		%
DP	Differential Phase	$R_L = 150\Omega$, 3.58 MHz/ 4.43 MHz		0.04		deg
Time Domain Response						
t_r	Rise Time	2V Step, 10% to 90%		1.4		ns
t_f	Fall Time	2V Step, 10% to 90%		1.3		ns
OS	Overshoot	2V Step		2		%
SR	Slew Rate	$6 V_{PP}$, 40% to 60% (Note 6)		1800		V/ μs
t_s	Settling Time	2V Step, V_{OUT} Within 0.5%		7		ns
Distortion And Noise Response						
HD2	2 nd Harmonic Distortion	$2 V_{PP}$, 5 MHz		-80		dBc
HD3	3 rd Harmonic Distortion	$2 V_{PP}$, 5 MHz		-70		dBc
e_n	Input Referred Voltage Noise	>1 MHz		12		nV/ $\sqrt{\text{Hz}}$
i_n	Input Referred Noise Current	>1 MHz		2		pA/ $\sqrt{\text{Hz}}$
	Switching Time			15		ns
XTLK	Cross Talk	All Hostile, $f = 100$ MHz		-45		dBc
		Channel to Channel, $f = 100$ MHz		-52		dBc
ISOL	Off Isolation	$f = 100$ MHz		-65		dBc
Static, DC Performance						
A_V	Gain	LMH6583	1.986	2.00	2.014	

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
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V_{OS}	Offset Voltage	Input Referred		± 2	± 17	mV
TCV_{OS}	Output Offset Voltage Average Drift	(Note 10)		38		$\mu V/^{\circ}C$
I_B	Input Bias Current	Non-Inverting (Note 9)		-5	-12	μA
TCI_B	Input Bias Current Average Drift	Non-Inverting (Note 10)		-12		nA/ $^{\circ}C$
V_O	Output Voltage Range	$R_L = 100\Omega$	+3.3 -3.4	± 3.6		V
V_O	Output Voltage Range	$R_L = \infty$	± 3.7	± 3.9		V
PSRR	Power Supply Rejection Ratio	DC	42	45		dB
XTLK	DC Crosstalk	DC, Channel to Channel	-58	-90		dB
ISOL	DC Off Isolation	DC	-60	-90		dB
I_{CC}	Positive Supply Current	$R_L = \infty$		110	130	mA
I_{EE}	Negative Supply Current	$R_L = \infty$		104	124	mA
	Tri State Supply Current	RST Pin > 2.0V		22	30	mA

Miscellaneous Performance

R_{IN}	Input Resistance	Non-Inverting		100		k Ω
C_{IN}	Input Capacitance	Non-Inverting		1		pF
R_O	Output Resistance Enabled	Closed Loop, Enabled		300		m Ω
R_O	Output Resistance Disabled	Disabled, Resistance to Ground	1100	1300	1450	Ω
CMVR	Input Common Mode Voltage Range			± 3.0		V
I_O	Output Current	Sourcing, $V_O = 0 V$	± 60	± 70		mA

Digital Control

V_{IH}	Input Voltage High		2.0			V
V_{IL}	Input Voltage Low				0.8	V
V_{OH}	Output Voltage High			>2.4		V
V_{OL}	Output Voltage Low			<0.4		V
T_S	Setup Time			5		ns
T_H	Hold Time			5		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

Note 2: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 3: The maximum output current (I_{OUT}) is determined by device power dissipation limitations.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$ and θ_{JA} . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Note 5: Electrical table values apply only for factory testing conditions at the temperature indicated. No guarantee of parametric performance is indicated in the electrical tables under conditions different than those tested.

Note 6: Slew Rate is the average of the rising and falling edges.

Note 7: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 8: Room Temperature limits are 100% production tested at 25 $^{\circ}C$. Device self heating results in $T_J \geq T_A$, however, test time is insufficient for T_J to reach steady state conditions. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

Note 9: Negative input current implies current flowing out of the device.

Note 10: Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.

Note 11: This parameter is guaranteed by design and/or characterization and is not tested in production.

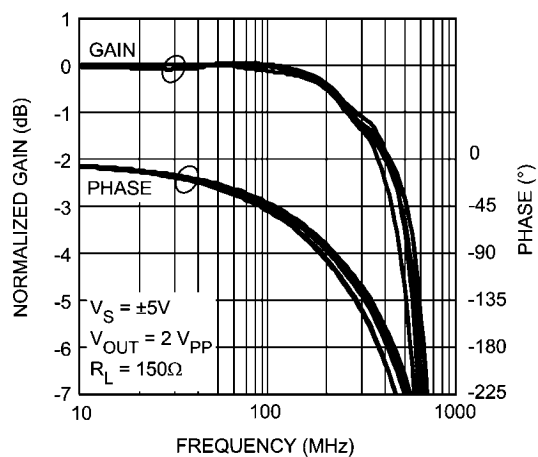
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
64-Pin QFP	LMH6583YA	LMH6583YA	160 Units/Tray	VXE64A

Typical Performance Characteristics

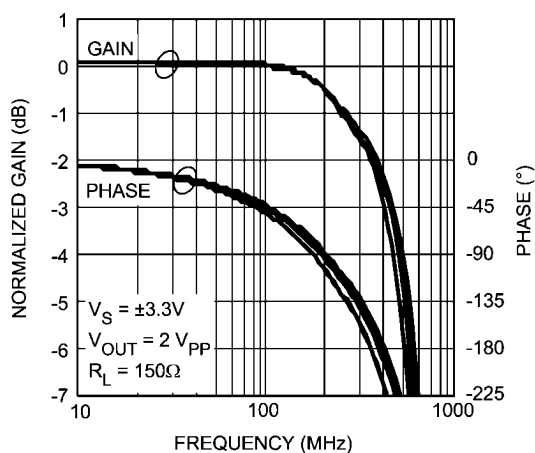
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2 V_{PP} Frequency Response



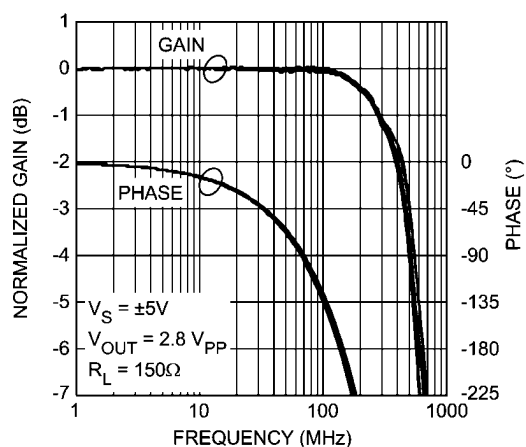
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2 V_{PP} Frequency Response



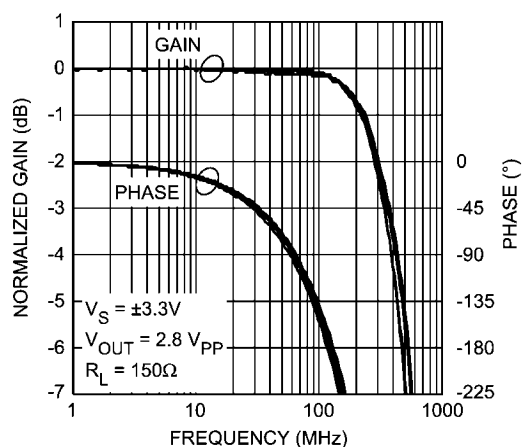
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Large Signal Bandwidth



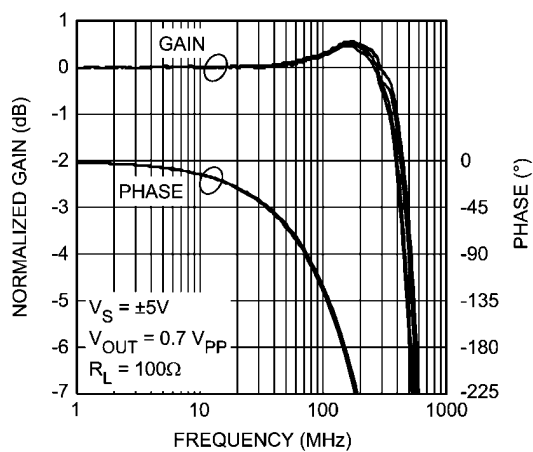
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Large Signal Bandwidth



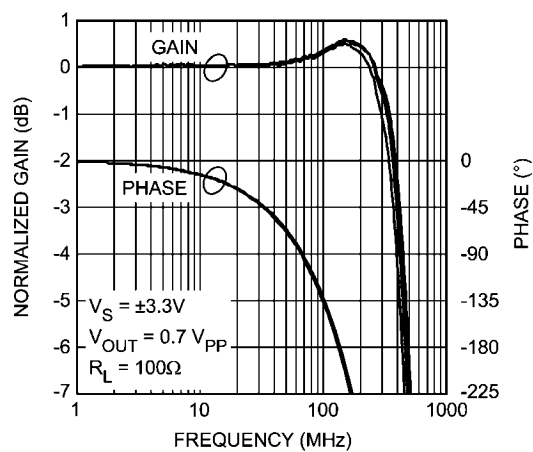
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Small Signal Bandwidth



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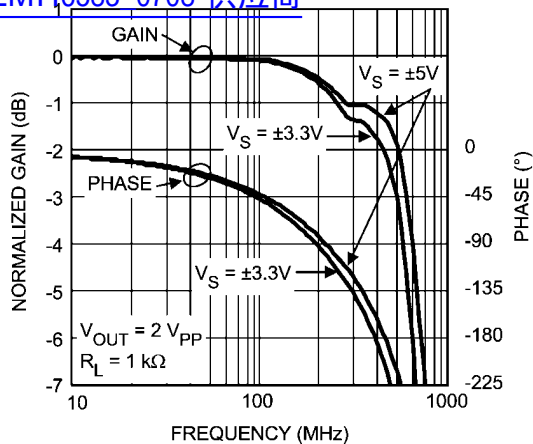
Small Signal Bandwidth



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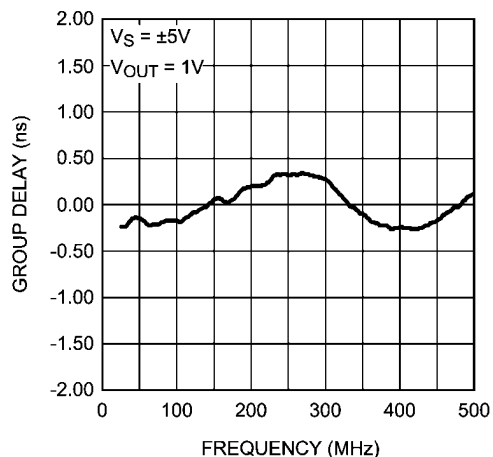
Frequency Response 1 k Ω Load

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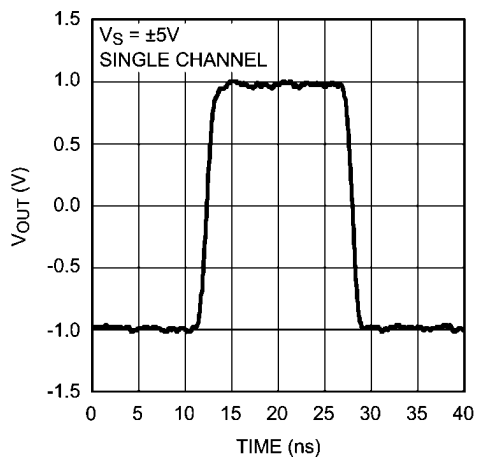
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Group Delay



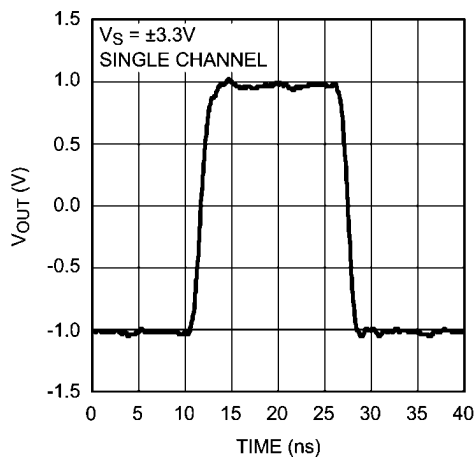
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2 V_{PP} Pulse Response



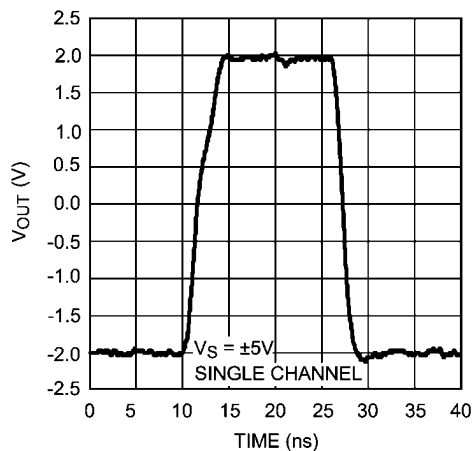
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2 V_{PP} Pulse Response



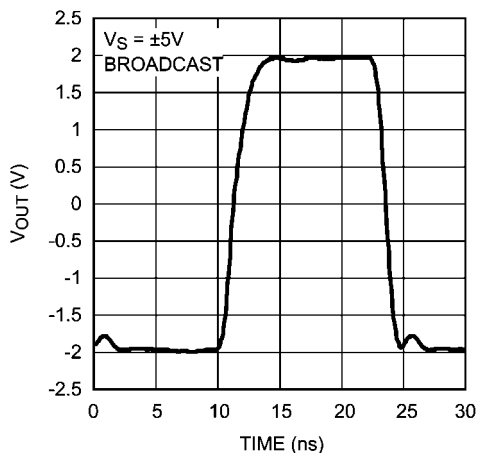
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4 V_{PP} Pulse Response



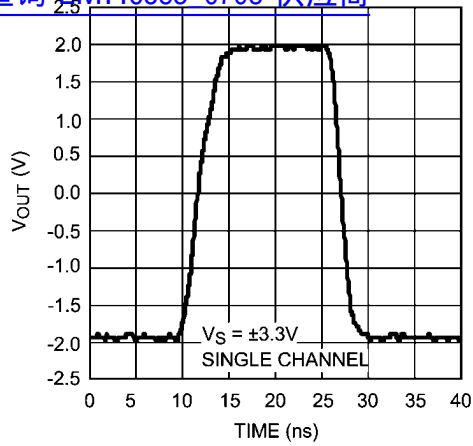
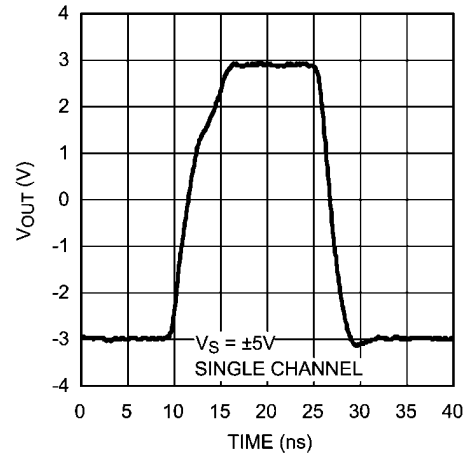
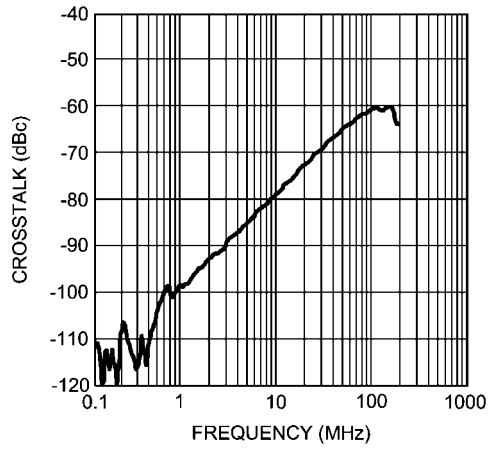
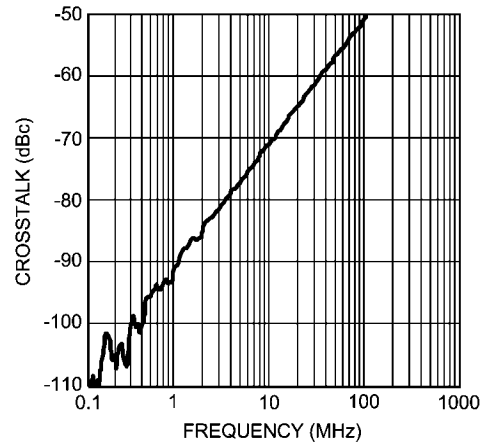
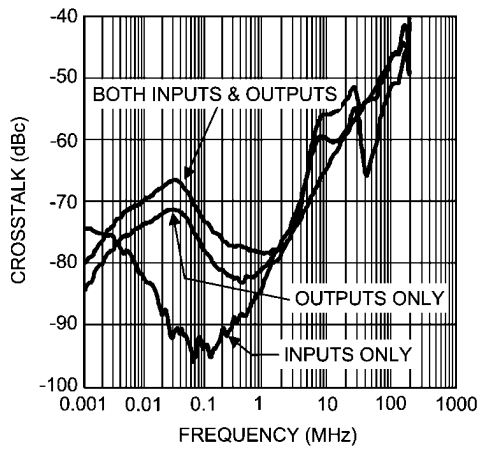
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4 V_{PP} Pulse Response Broadcast

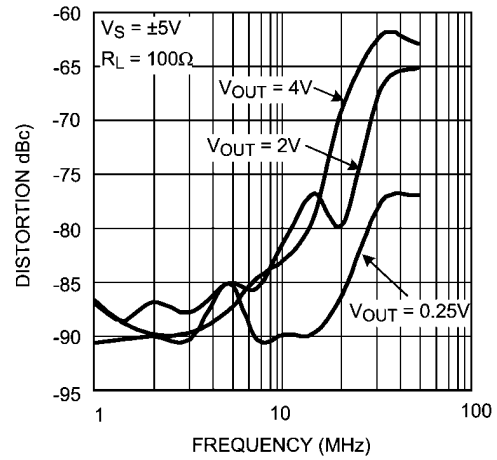


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4 V_{PP} Pulse Response
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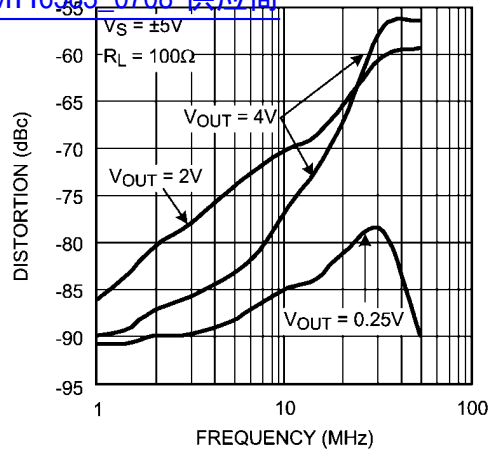
6 V_{PP} Pulse Response2 V_{PP} Off Isolation2 V_{PP} Crosstalk2 V_{PP} All Hostile Crosstalk

Second Order Distortion (HD2) vs. Frequency



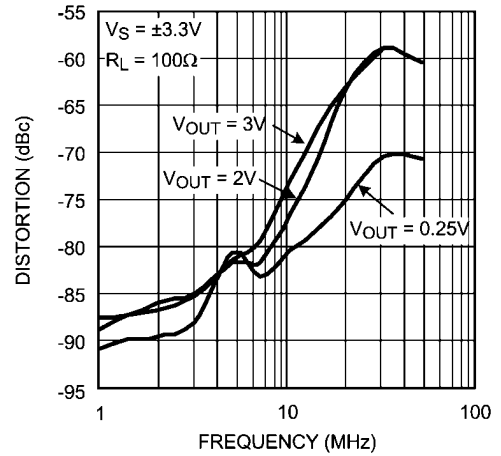
Third Order Distortion (HD3) vs. Frequency

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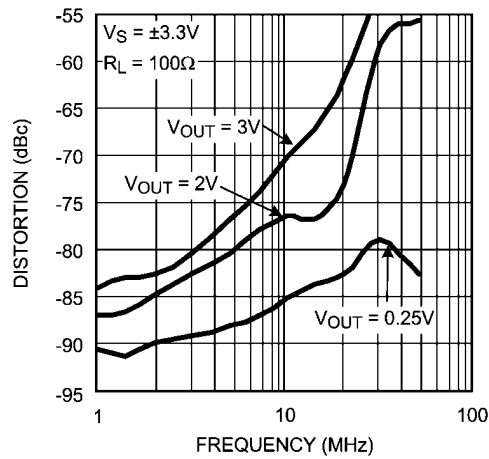
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Second Order Distortion vs. Frequency



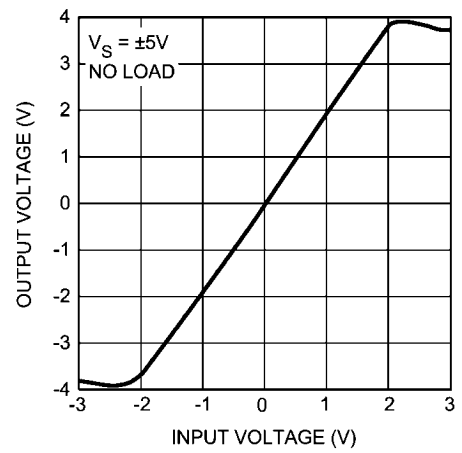
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Third Order Distortion vs. Frequency



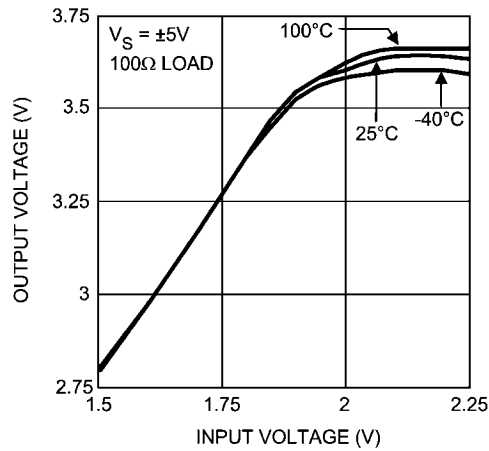
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No Load Output Swing



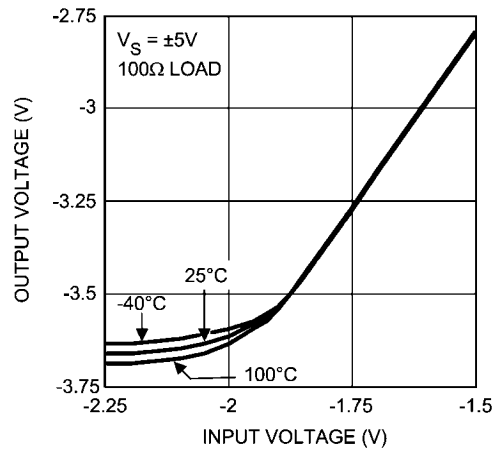
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Positive Swing over Temperature



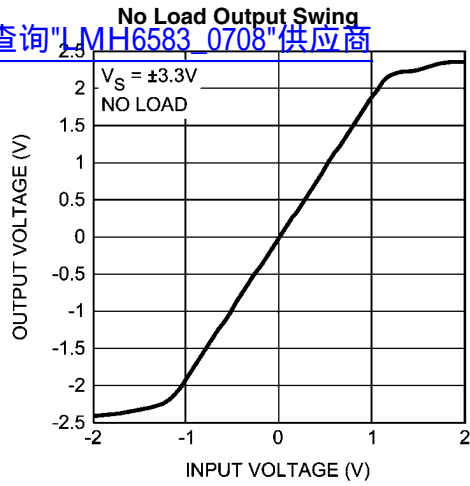
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Negative Swing Over Temperature

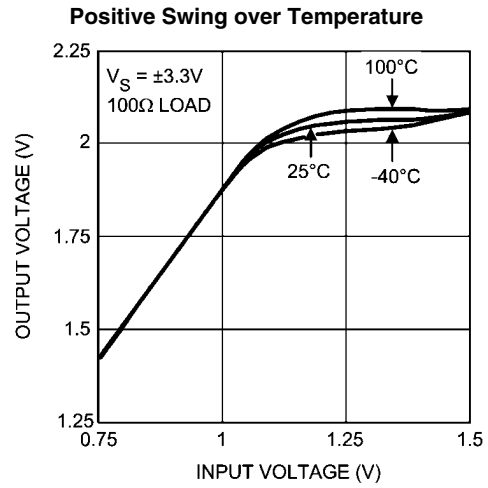


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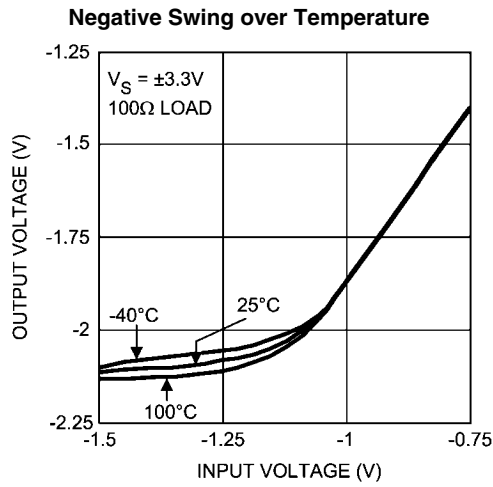
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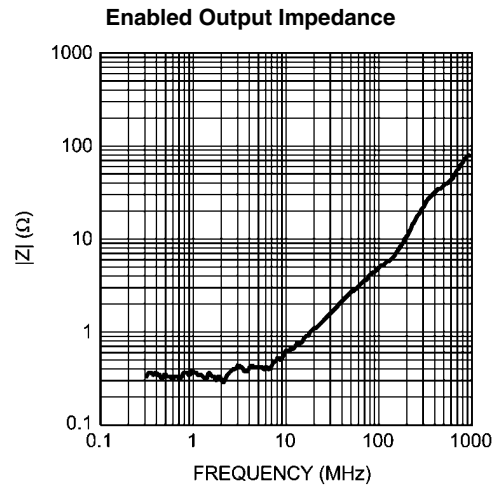
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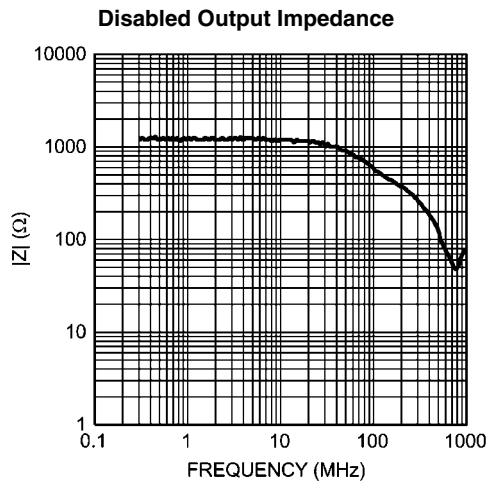
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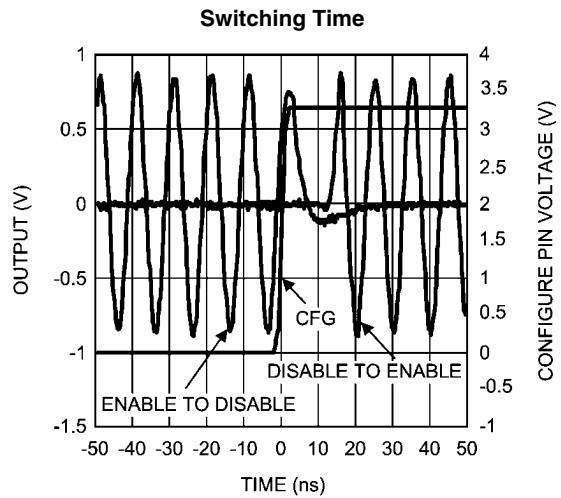
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Application Information

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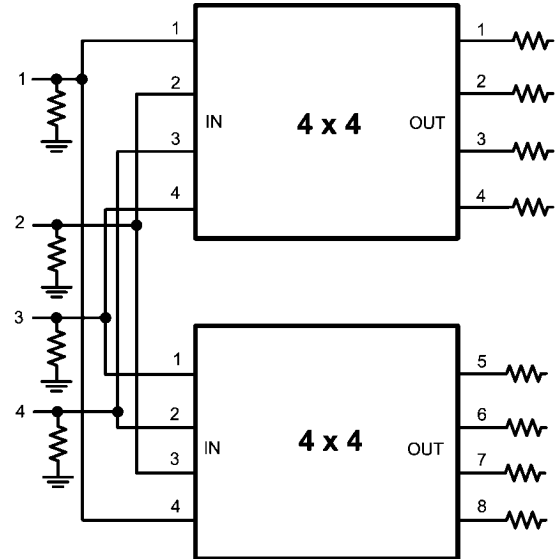
The LMH6583 is a high speed, fully buffered, non blocking, analog crosspoint switch. Having fully buffered inputs allows the LMH6583 to accept signals from low or high impedance sources without the worry of loading the signal source. The fully buffered outputs will drive 75Ω or 50Ω back terminated transmission lines with no external components other than the termination resistor. When disabled, the outputs are in a high impedance state. The LMH6583 can have any input connected to any (or all) output(s). Conversely, a given output can have only one associated input.

INPUT AND OUTPUT EXPANSION

The LMH6583 has high impedance inactive states for both inputs and outputs allowing maximum flexibility for Crosspoint expansion. In addition the LMH6583 employs diagonal symmetry in pin assignments. The diagonal symmetry makes it easy to use direct pin to pin vias when the parts are mounted on opposite sides of a board. As an example two LMH6583 chips can be combined on one board to form either an 16×16 crosspoint or a 32×8 crosspoint. To make a 16×16 crosspoint all 16 input pins would be tied together (Input 0 on side 1 to input 15 on side 2 and so on) while the 8 output pins on each chip would be left separate. To make the 32×8 crosspoint, the 8 outputs would be tied together while all 32 inputs would remain independent. In the 32×8 configuration it is important not to have 2 connected outputs active at the same time. With the 16×16 configuration, on the other hand, having two connected inputs active is a valid state. Crosspoint expansion as detailed above has the advantage that the signal path has only one crosspoint in it at a time. Expansion methods that have cascaded stages will suffer bandwidth loss far greater than the small loading effect of parallel expansion.

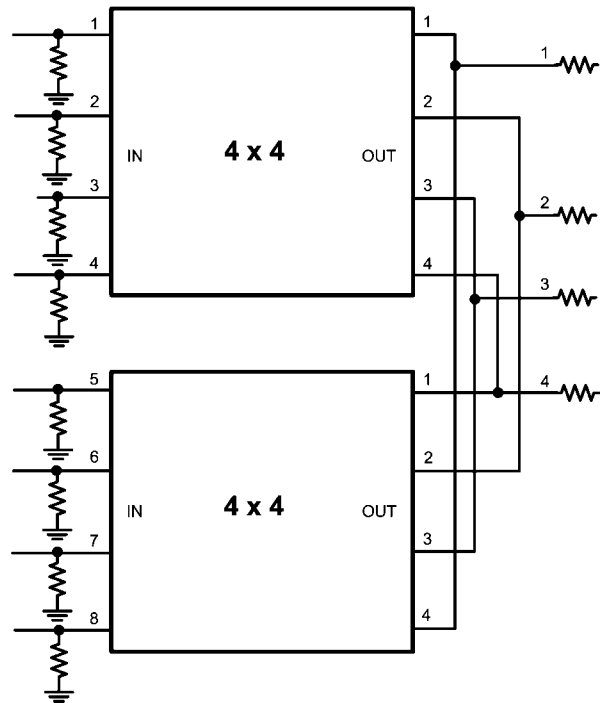
Output expansion is very straight forward. Connecting the inputs of two crosspoint switches has a very minor impact on performance. Input expansion requires more planning. As show in Figure 1 and Figure 2 there are two ways to connect the outputs of the crosspoint switches. In Figure 2 the crosspoint switch outputs are connected directly together and share one termination resistor. This is the easiest configuration to implement and has only one drawback. Because the disabled output of the unused crosspoint (only one output can be active at a time) has a small amount of capacitance the frequency response of the active crosspoint will show peaking. This is illustrated in Figure 4 and Figure 5. In most cases this small amount of peaking is not a problem.

As illustrated in Figure 1 each crosspoint output can be given its own termination resistor. This results in a frequency response nearly identical to the non expansion case. There is one drawback for the gain of 2 crosspoint, and that is gain error. With a 75Ω termination resistor the 1250Ω resistance of the disabled crosspoint output will cause a gain error. In order to counter act this the termination resistors of both crosspoints should be adjusted to approximately 71Ω . This will provide very good matching, but the gain accuracy of the system will now be dependent on the process variations of the crosspoint resistors which have a variability of approximately $\pm 20\%$.



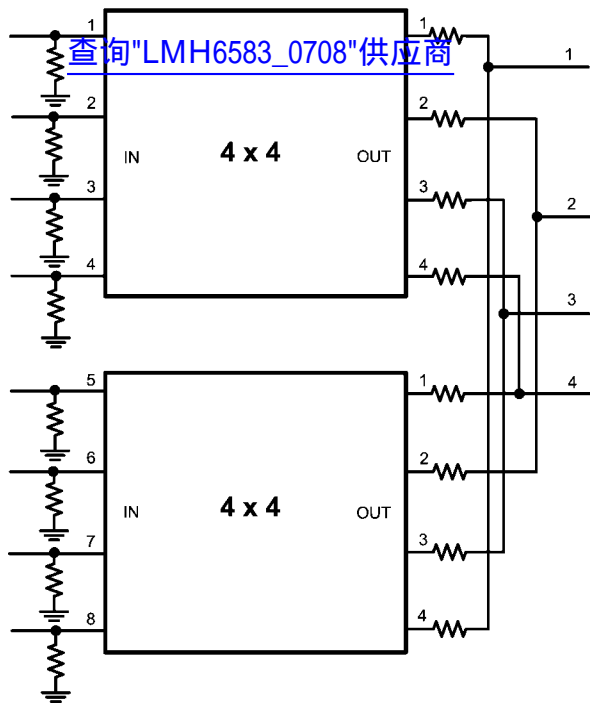
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FIGURE 1. Output Expansion



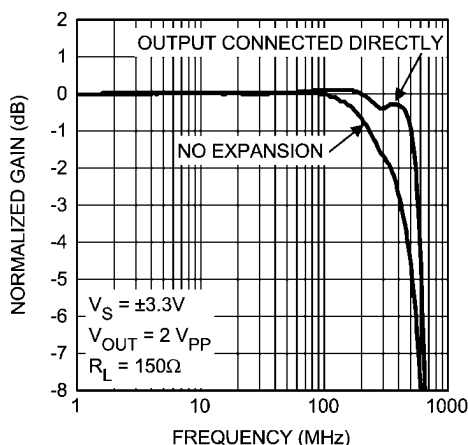
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FIGURE 2. Input Expansion with Shared Termination Resistors



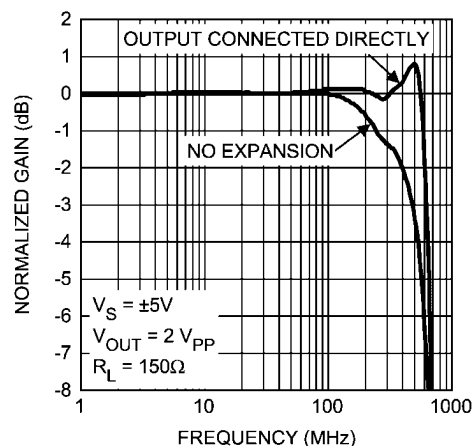
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FIGURE 3. Input Expansion with Separate Termination Resistors



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FIGURE 4. Input Expansion Frequency Response



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FIGURE 5. Input Expansion Frequency Response

DRIVING CAPACITIVE LOADS

Capacitive output loading applications will benefit from the use of a series output resistor R_{OUT} . Capacitive loads of 5 pF to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. The chart "Suggested R_{OUT} vs. Cap Load" gives a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for 0.5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of R_{OUT} can be reduced slightly from the recommended values. When driving transmission lines the 50Ω or 75Ω matching resistor makes the series output resistor unnecessary.

USING OUTPUT BUFFERING TO ENHANCE BANDWIDTH AND INCREASE RELIABILITY

The LMH6583 crosspoint switch can offer enhanced bandwidth and reliability with the use of external buffers on the outputs. The bandwidth is increased by unloading the outputs and driving a higher impedance. The 1 kΩ load resistor was chosen to provide the best performance on our evaluation board. See the Frequency Response 1 kΩ Load curve in the Typical Performance section for an example of bandwidth achieved with less loading on the outputs. For this technique to provide maximum benefit a very high speed amplifier such as the LMH6703 should be used, as shown in Figure 6.

Besides offering enhanced bandwidth performance using an external buffer provides for greater system reliability. The first advantage is to reduce thermal loading on the crosspoint switch. This reduced die temperature will increase the life of the crosspoint. The second advantage is enhanced ESD reliability. It is very difficult to build high speed devices that can withstand all possible ESD events. With external buffers the crosspoint switch is isolated from ESD events on the external system connectors.

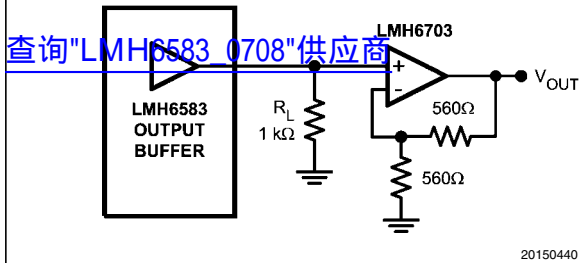


FIGURE 6. Buffered Output

In the example in *Figure 6* the resistor R_L is required to provide a load for the crosspoint output buffer. Without R_L excessive frequency response peaking is likely and settling times of transient signals will be poor. As the value of R_L is reduced the bandwidth will also go down. The amplifier shown in the example is an LMH6703 this amplifier offers high speed and flat bandwidth. Another suitable amplifiers is the LMH6702. The LMH6702 is a faster amplifier that can be used to generate high frequency peaking in order to equalize longer cable lengths. If board space is at a premium the LMH6739 or the LMH6734 are triple selectable gain buffers which require no external resistors.

CROSSTALK

When designing a large system such as a video router crosstalk can be a very serious problem. Extensive testing in our lab has shown that most crosstalk is related to board layout rather than occurring in the crosspoint switch. There are many ways to reduce board related crosstalk. Using controlled impedance lines is an important step. Using well decoupled power and ground planes will help as well. When crosstalk does occur within the crosspoint switch itself it is often due to signals coupling into the power supply pins. Using appropriate supply bypassing will help to reduce this mode of coupling. Another suggestion is to place as much grounded copper as possible between input and output signal traces. Care must be taken, though, not to influence the signal trace impedances by placing shielding copper too closely. One other caveat to consider is that as shielding materials come closer to the signal trace the trace needs to be smaller to keep the impedance from falling too low. Using thin signal traces will result in unacceptable losses due to trace resistance. This effect becomes even more pronounced at higher frequencies due to the skin effect. The skin effect reduces the effective thickness of the trace as frequency increases. Resistive losses make crosstalk worse because as the desired signal is attenuated with higher frequencies crosstalk increases at higher frequencies.

DIGITAL CONTROL

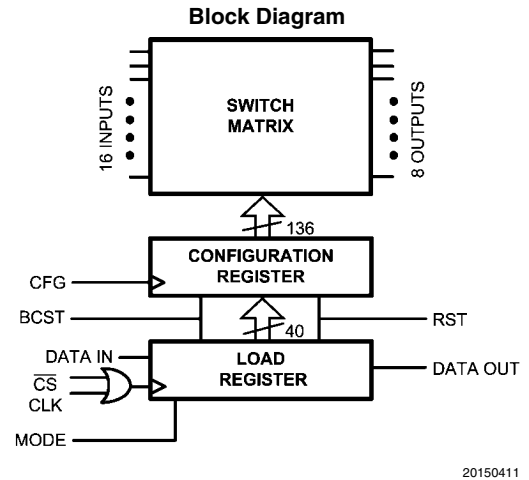


FIGURE 7.

The LMH6583 has internal control registers that store the programming states of the crosspoint switch. The logic is two staged to allow for maximum programming flexibility. The first stage of the control logic is tied directly to the crosspoint switching matrix. This logic consists of one register for each output that stores the on/off state and the address of which input to connect to. These registers are not directly accessible by the user. The second level of logic is another bank of registers identical to the first, but set up as shift registers. These registers are accessed by the user via the serial input bus. As described further below, there are two modes for programming the LMH6582, Serial Mode and Addressed Mode.

The LMH6583 is programmed via a serial input bus with the support of 4 other digital control pins. The Serial bus consists of a clock pin (CLK), a serial data in pin (DIN), and a serial data out pin (D_{OUT}). The serial bus is gated by a chip select pin (CS). The chip select pin is active low. While the chip select pin is high all data on the serial input pin and clock pins is ignored. When the chip select pin is brought low the internal logic is set to begin receiving data by the first positive transition (0 to 1) of the clock signal. The chip select pin must be brought low at least 5 ns before the first rising edge of the clock signal. The first data bit is clocked in on the next negative transition (1 to 0) of the clock signal. All input data is read from the bus on the negative edge of the clock signal. Once the last valid data has been clocked in, the chip select pin must go high then the clock signal must make at least one more low to high transition. Otherwise invalid data will be clocked into the chip. The data clocked into the chip is not transferred to the crosspoint matrix until the CFG pin is pulsed high. This is the case regardless of the state of the Mode pin. The CFG pin is not dependent on the state of the Chip select pin. If no new data is clocked into the chip subsequent pulses on the CFG pin will have no effect on device operation.

The programming format of the incoming serial data is selected by the MODE pin. When the mode pin is HIGH the crosspoint can be programmed one output at a time by entering a string of data that contains the address of the output that is going to be changed (Addressed Mode). When the mode pin is LOW the crosspoint is in Serial Mode. In this mode the crosspoint accepts a 40 bit array of data that programs all of the outputs. In both modes the data fed into the chip does not change the chip operation until the Configure

pin is pulsed high. The configure and mode pins are independent of the chip select pin.

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THREE WIRE VS. FOUR WIRE CONTROL

There are two ways to connect the serial data pins. The first way is to control all 4 pins separately, and the second option is to connect the CFG and the CS pins together for a 3 wire interface. The benefit of the 4 wire interface is that the chip can be configured independently of the CS pin. This would be an advantage in a system with multiple crosspoint chips where all of them could be programmed ahead of time and then configured simultaneously. The 4 wire solution is also helpful in a system that has a free running clock on the CLK pin. In this case, the CS pin needs to be brought high after the last valid data bit to prevent invalid data from being clocked into the chip.

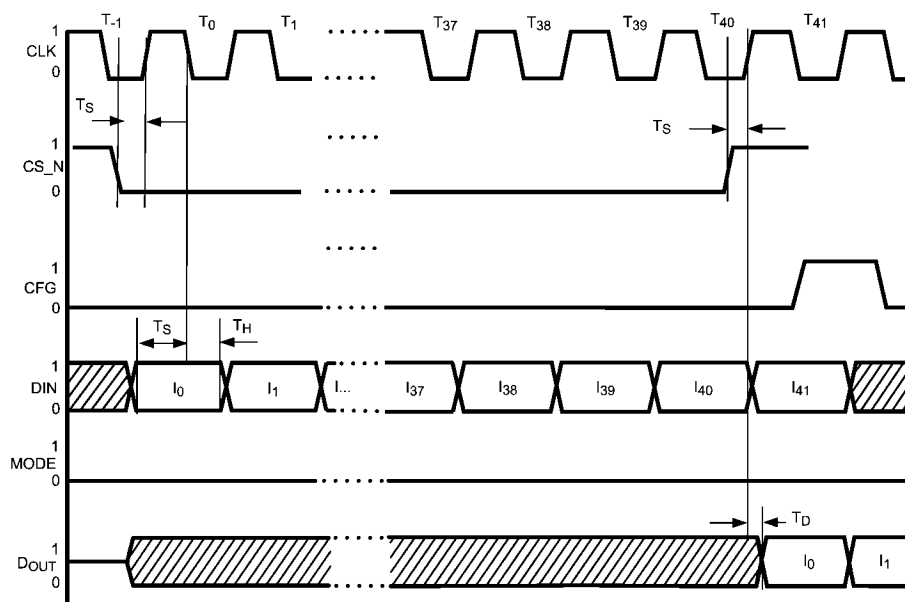
The three wire option provides the advantage of one less pin to control at the expense of having less flexibility with the configure pin. One way around this loss of flexibility would be if the clock signal is generated by an FPGA or microcontroller where the clock signal can be stopped after the data is clocked in. In this case the Chip select function is provided by the presence or absence of the clock signal.

SERIAL PROGRAMMING MODE

Serial programming mode is the mode selected by bringing the MODE pin low. In this mode a stream of 40 bits programs

all 8 outputs of the crosspoint. The data is fed to the chip as shown in the Serial Mode Data Frame tables below (4 tables are required to show the entire data frame). The table is arranged such that the first bit clocked into the crosspoint register is labeled bit number 0. The register labeled Load Register in the block diagram is a shift register. If the chip select pin is left low after the valid data is shifted into the chip and if the clock signal keeps running then additional data will be shifted into the register, and the desired data will be shifted out.

Also illustrated is the timing relationships for the digital pins in the Timing Diagram for Serial Mode shown below. It is important to note that all the pin timing relationships are important, not just the data and clock pins. One example is that the Chip Select pin (CS) must transition low before the first rising edge of the clock signal. This allows the internal timing circuits to synchronize to allow data to be accepted on the next falling edge. After the final data bit has been clocked in, the chip select pin must go high, then the clock signal must make at least one more low to high transition. As shown in the timing diagram, the chip select pin state should always occur while the clock signal is low. The configure (CFG) pin timing is not so critical, but it does need to be kept low until all data has been shifted into the crosspoint registers.



Timing Diagram for Serial Mode

20150409

Serial Mode Data Frame (First 2 Words)

Output 0					Output 1				
Input Address				On = 0	Input Address				On = 0
LSB			MSB	Off = 1	LSB			MSB	Off = 1
0	1	2	3	4	5	6	7	8	9

Off = TRI-STATE®, Bit 0 is first bit clocked into device.

Serial Mode Data Frame (Continued)

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Output 2					Output 3				
Input Address				On = 0	Input Address				On = 0
LSB			MSB	Off = 1	LSB			MSB	Off = 1
10	11	12	13	14	15	16	17	18	19

Serial Mode Data Frame (Continued)

Output 4					Output 5				
Input Address				On = 0	Input Address				On = 0
LSB			MSB	Off = 1	LSB			MSB	Off = 1
20	21	22	23	24	25	26	27	28	29

Serial Mode Data Frame (Last 2 Words)

Output 6					Output 7				
Input Address				On = 0	Input Address				On = 0
LSB			MSB	Off = 1	LSB			MSB	Off = 1
30	31	32	33	34	35	36	37	38	39

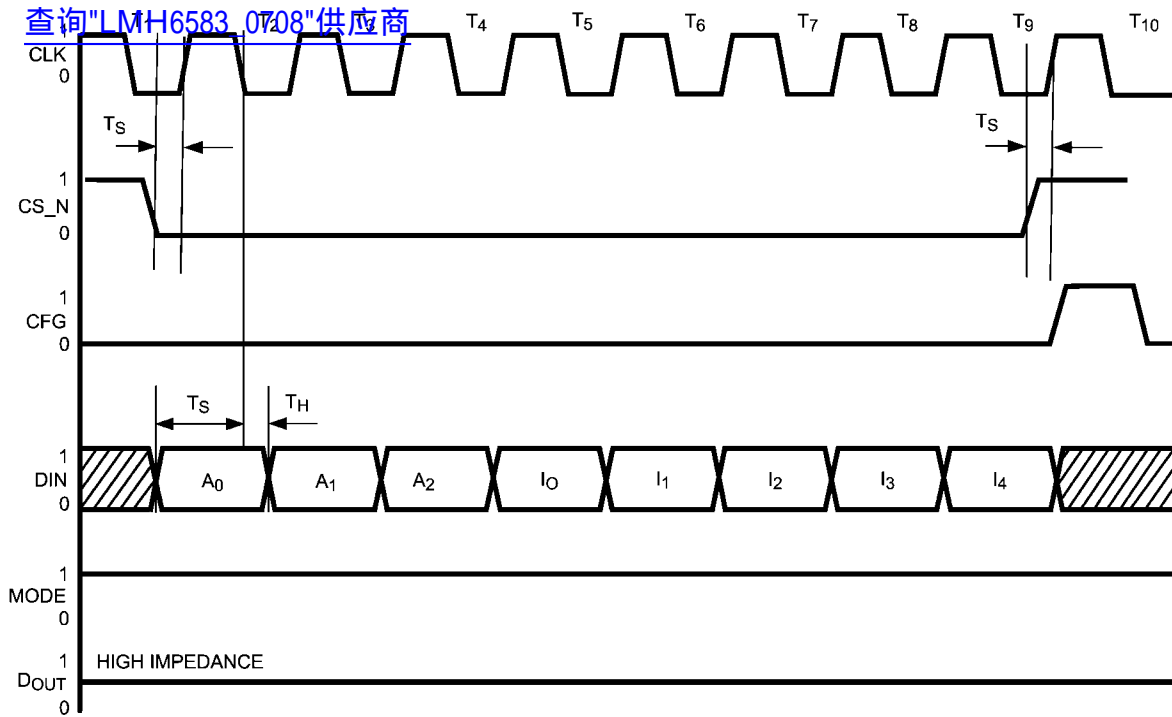
Bit 39 is last bit clocked into device.

ADDRESSED PROGRAMMING MODE

Addressed programming mode makes it possible to change only one output register at a time. To utilize this mode the mode pin must be High. All other pins function the same as in serial programming mode except that the word clocked in is 8 bits and is directed only at the output specified. In addressed mode the data format is shown below in the table titled Addressed Mode Word Format.

Also illustrated is the timing relationships for the digital pins in the Timing Diagram for Addressed Mode shown below. It is important to note that all the pin timing relationships are

important, not just the data and clock pins. One example is that the Chip Select pin (CS) must transition low before the first rising edge of the clock signal. This allows the internal timing circuits to synchronize to allow data to be accepted on the next falling edge. After the final data bit has been clocked in, the chip select pin must go high, then the clock signal must make at least one more low to high transition. As shown in the timing diagram, the chip select pin state should always occur while the clock signal is low. The configure (CFG) pin timing is not so critical, but it does need to be kept low until all data has been shifted into the crosspoint registers.



Timing Diagram for Addressed Mode

20150410

Addressed Mode Word Format

Output Address			Input Address				TRI-STATE
LSB		MSB	LSB			MSB	1 = TRI-STATE 0 = On
0	1	2	3	4	5	6	7

Bit 0 is first bit clocked into device.

DAISY CHAIN OPTION IN SERIAL MODE

The LMH6583 supports daisy chaining of the serial data stream between multiple chips. This feature is available only in the Serial programming mode. To use this feature serial data is clocked into the first chip DIN pin, and the next chip DIN pin is connected to the DOUT pin of the first chip. Both chips may share a chip select signal, or the second chip can be enabled separately. When the chip select pin goes low on both chips a double length word is clocked into the first chip. As the first word is clocking into the first chip the second chip is receiving the data that was originally in the shift register of the first chip (invalid data). When a full 40 bits have been clocked into the first chip the next clock cycle begins moving the first frame of the new configuration data into the second chip. With a full 80 clock cycles both chips have valid data and the chip select pin of both chips should be brought high to prevent the data from overshooting. A configure pulse will activate the new configuration on both chips simultaneously, or each chip can be configured separately. The mode, chip select, configure and clock pins of both chips can be tied together and driven from the same sources.

SPECIAL CONTROL PINS

The LMH6583 has two special control pins that function independent of the serial control bus. One of these pins is the reset (RST) pin. The RST pin is active high meaning that a

logic 1 level the chip is configured with all outputs disabled and in a high impedance state. The RST pin programs all the registers with input address 0 and all the outputs are turned off. In this configuration the device draws only 20 mA. The reset pin can be used as a shutdown function to reduce power consumption. The other special control pin is the broadcast (BCST) pin. The BCST pin is also active high and sets all the outputs to the on state connected to input 0. Both of these pins are level sensitive and require no clock signal. The two special control pins overwrite the contents of the configuration register.

THERMAL MANAGEMENT

The LMH6583 is packaged in a thermally enhanced Quad Flat Pack package. Even so, it is a high performance device that produces a significant amount of heat. With a $\pm 5V$ supply, the LMH6583 will dissipate approximately 1.1W of idling power with all outputs enabled. Idling power is calculated based on the typical supply current of 110 mA and a 10V supply voltage. This power dissipation will vary within the range of 800 mW to 1.4W due to process variations. In addition, each equivalent video load (150Ω) connected to the outputs should be budgeted 30 mW of power. For a typical application with one video load for each output this would be a total power of 1.14 W. With a typical θ_{JA} of 27°C/W this will result in the silicon being 31°C over the ambient temperature. A more aggressive application would be two video loads per output which would

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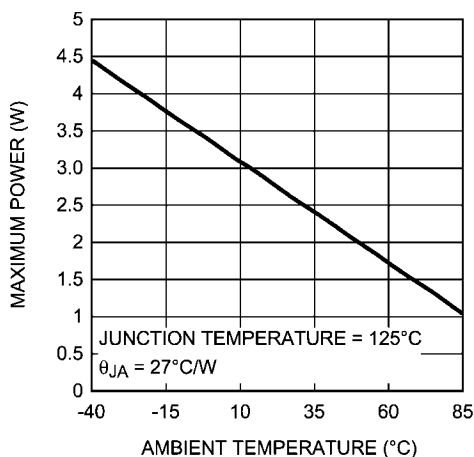
result in 1.38 W of power dissipation. This would result in a 37°C temperature rise. For heavy loading, the QFP package thermal performance can be significantly enhanced with an external heat sink and by providing for moving air ventilation. Also, be sure to calculate the increase in ambient temperature from all devices operating in the system case. Because of the high power output of this device, thermal management should be considered very early in the design process. Generous passive venting and vertical board orientation may avoid the need for fan cooling or heat sinks. Also, the LMH6583 can be operated with a $\pm 3.3\text{V}$ power supply. This will cut power dissipation substantially while only reducing bandwidth by about 10% (2 V_{PP} output). The LMH6583 is fully characterized and factory tested at the $\pm 3.3\text{V}$ power supply condition for applications where reduced power is desired.

If a heat sink is desired AAVD/Thermalloy part # 375324B00035G is the proper size for the LMH6583 package. This heat sink comes with adhesive tape for ease in assembly. With natural convection the heat sink will reduce the θ_{JA} from 27°C/W to approximately 21°C/W . Using a fan will increase the effectiveness of the heat sink considerably. When doing thermal design it is important to note that everything from board layout to case material will impact the actual θ_{JA} of the device. The θ_{JA} specified in the datasheet is for a typical board layout.

PRINTED CIRCUIT LAYOUT

Generally, a good high frequency layout will keep power supply and ground traces away from the input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information). If digital control lines must cross analog signal lines (particularly inputs) it is best if they cross perpendicularly. National Semiconductor suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board Part Number
LMH6583	64-Pin TQFP	LMH730156



20150453

FIGURE 8. Maximum Dissipation vs. Ambient Temperature

Notes

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