National Semiconductor

March 1993

54ACT/74ACT563
Octal Latch with TRI-STATE® Outputs

General Description

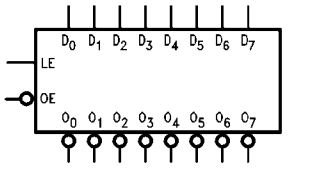
The 'ACT563 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

The 'ACT563 device is functionally identical to the 'ACT573, but with inverted outputs.

Features

- I_{CC} and I_{OZ} reduced by 50%
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'ACT573 but with inverted outputs
- Outputs source/sink 24 mA
- 'ACT563 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  —'ACT563: 5962-89556

Logic Symbols



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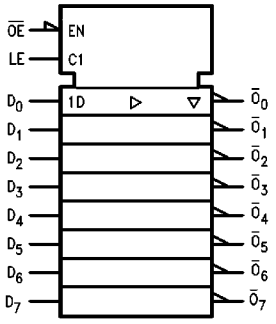
IEEE/IEC



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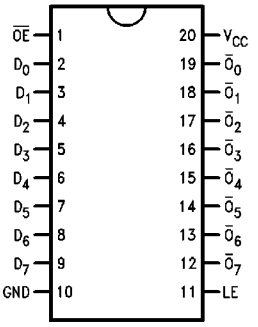
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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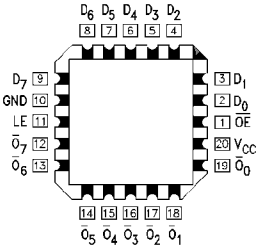
Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	TRI-STATE Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	TRI-STATE Latch Outputs

Pin Assignment for LCC



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RRD-B30M75/Printed in U. S. A.

Functional Description

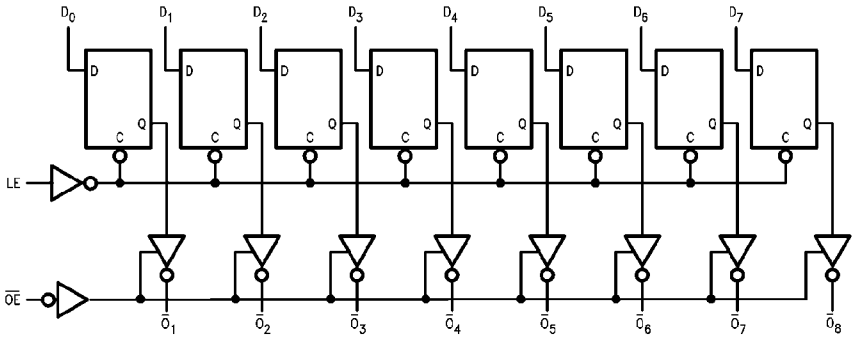
The 'ACT563 contains eight D-type latches with TRI-STATE complementary outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but that does not interfere with entering new data into the latches.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	LE	D	Q	O	
H	X	X	X	Z	High-Z
H	H	L	H	Z	High-Z
H	H	H	L	Z	High-Z
H	L	X	NC	Z	Latched
L	H	L	H	H	Transparent
L	H	H	L	L	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACT	−40°C to +85°C
54ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.25	±5.0	±2.5	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACT Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay D_n to $\overline{O}_n$	5.0	3.0	7.0	11.5	1.0	14.5	2.5	12.5	ns
t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	5.0	3.0	6.0	10.0	1.0	12.0	2.5	11.0	ns
t_{PLH}	Propagation Delay LE to $\overline{O}_n$	5.0	3.0	6.5	10.5	1.0	12.5	2.5	11.5	ns
t_{PHL}	Propagation Delay LE to $\overline{O}_n$	5.0	2.5	5.5	9.5	1.0	11.5	2.0	10.5	ns
t_{PZH}	Output Enable Time	5.0	2.5	5.5	9.0	1.0	11.5	2.0	10.0	ns
t_{PZL}	Output Enable Time	5.0	2.0	5.5	8.5	1.0	11.0	2.0	9.5	ns
t_{PHZ}	Output Disable Time	5.0	3.5	6.5	10.5	1.0	12.0	2.5	11.5	ns
t_{PLZ}	Output Disable Time	5.0	2.0	4.5	8.0	1.0	9.5	1.0	8.5	ns

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	1.5	4.0	4.5	4.5	ns
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	−2.0	0	1.5	0	ns
t_w	LE Pulse Width, HIGH	5.0	2.0	3.0	5.0	3.0	ns

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	50.0	pF	V_{CC} = 5.0V

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74ACT 563 P C QR

Temperature Range Family
- 74ACT = Commercial TTL-Compatible
- 54ACT = Military TTL-Compatible

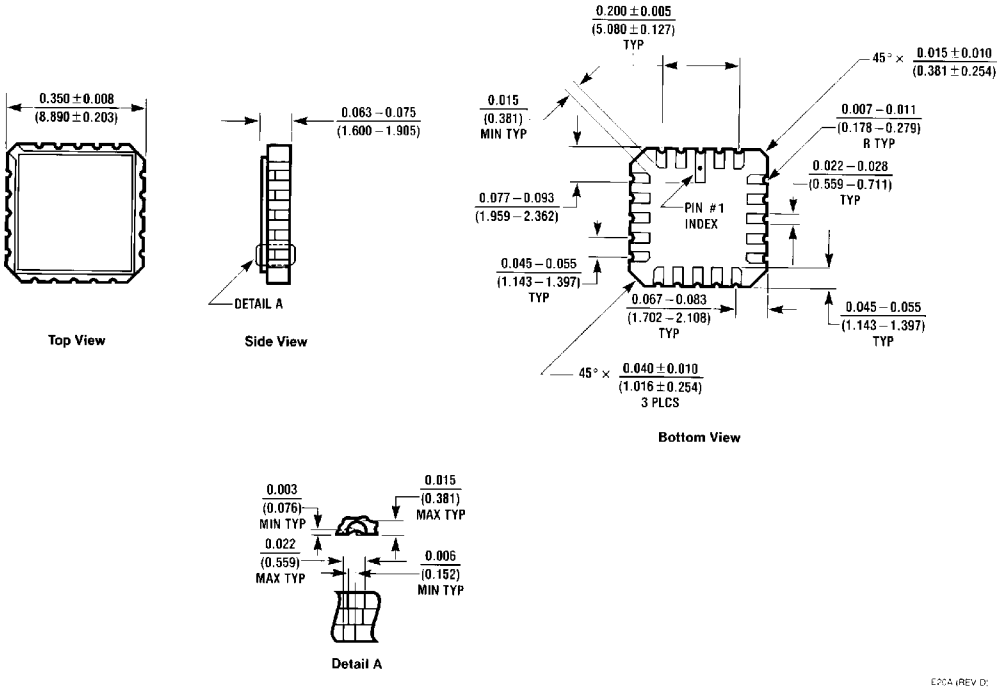
Device Type

Package Code
- P = Plastic DIP
- D = Ceramic DIP
- F = Flatpak
- L = Leadless Ceramic Chip Carrier (LCC)
- S = Small Outline (SOIC)

Special Variations
- X = Devices shipped in 13" reels
- QR = Commercial grade device with burn-in
- QB = Military grade device with environmental and burn-in processing shipped in tubes

Temperature Range
- C = Commercial (−40°C to +85°C)
- M = Military (−55°C to +125°C)

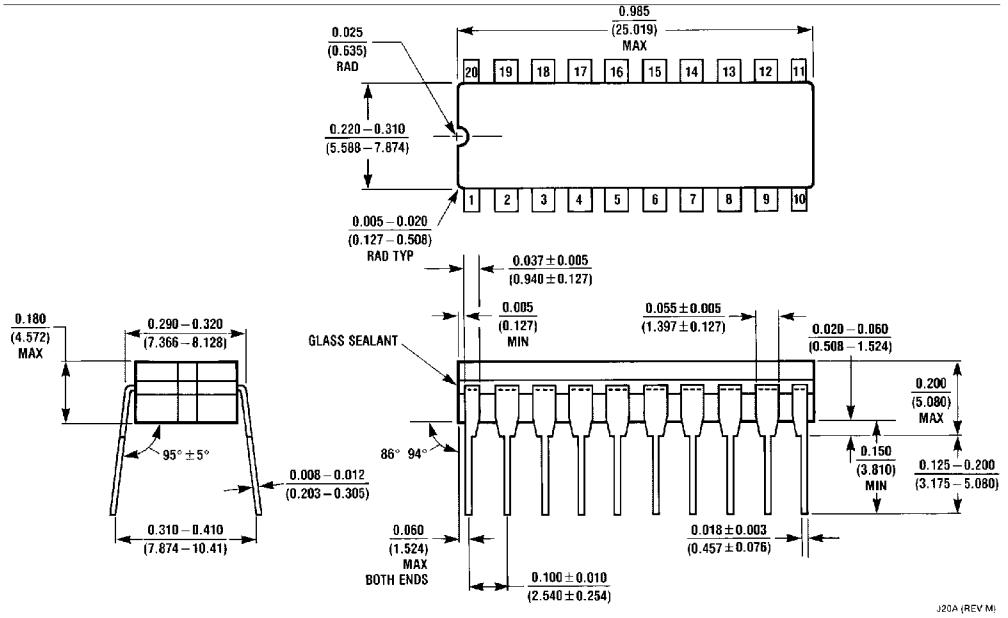
Physical Dimensions inches (millimeters)



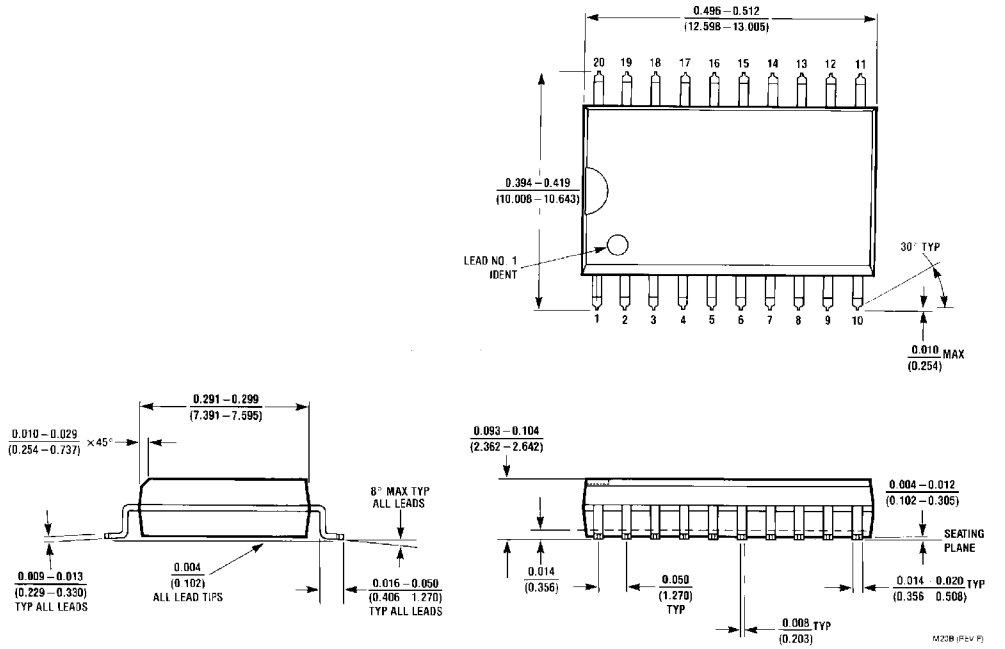
E20A (REV D)

20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

Physical Dimensions inches (millimeters) (Continued)



20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A



20-Lead Small Outline Integrated Circuit (S)
NS Package Number M20B

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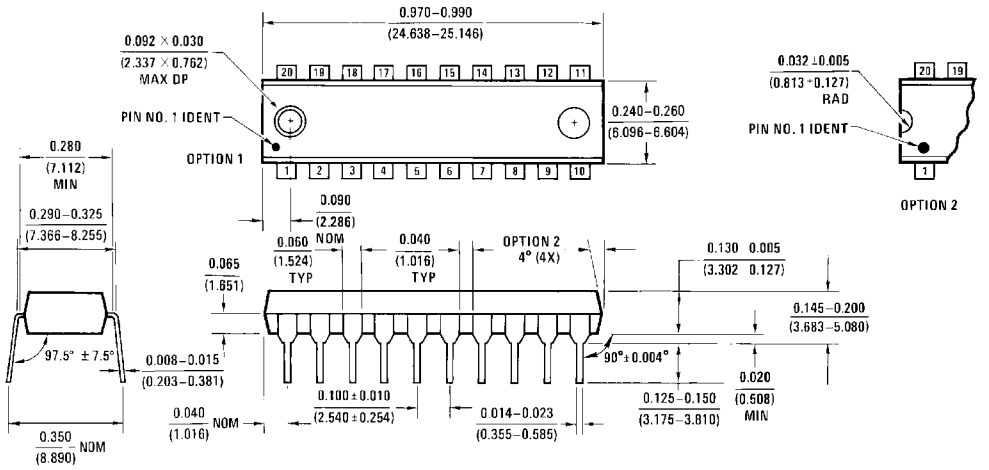
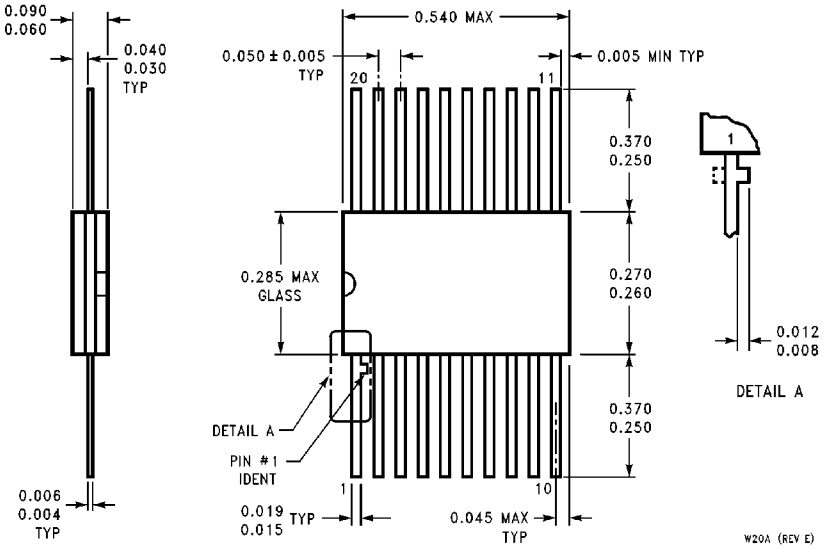
Physical Dimensions inches (millimeters) (Continued)



20-Lead Plastic Dual-In-Line Package (P)
NS Package Number N20B

Physical Dimensions inches (millimeters) (Continued)



20-Lead Ceramic Flatpak (F)
NS Package Number W20A

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