

**LC75010W****LC75010W Car Audio DSP**

## Overview

The LC75010W is a car audio DSP IC that integrates the signal processing required by car audio systems, A/D and D/A converters, volume control, and other functions on a single chip. It can implement a car audio system with a minimal number of external components.

## Features

- Hardware Functions
    - Analog source selector (BTL:1ch, OTL:3 ch)
    - 20 bits A/D (2ch)
    - 24 bits DSP (core, program memory, data memory)
    - SIO (CCB I/F) (CCB is LSB first input.)
    - 24 bits D/A (4ch)
    - EVR (4ch)
  - Software Functions\* (See Note.)
    - Bass/Mid/Treb
    - Bal/Fad
    - Fixed equalizer (Front/Rear/separately controlled)
    - Loudness control
    - Hybrid volume
    - Anti-hard clip
    - Dedekind (Speaton\*\*)
- Note \*: Software specifications can be modified in response to user requests.
- DSP Functions (24 fixed-point DSP)
    - Program ROM — 8k words
    - Data RAM — 896 words

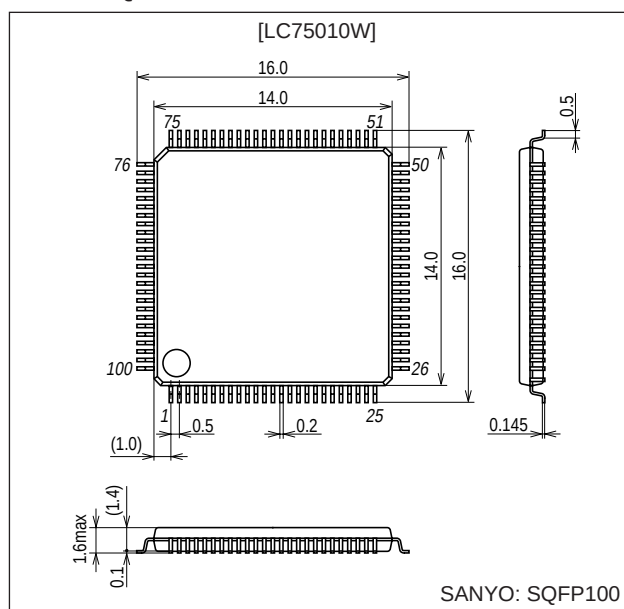
## Supply Voltage and Package Specifications

- DSP core, A/D converter (digital block), D/A converter (digital block): 3.3 V
- A/D converter (analog block), D/A converter (analog block), volume control, crystal oscillator: 5 V
- Package: 100-pin SQFP (14×14 mm)

## Package Dimensions

unit: mm

### 3181C-SQFP100



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  - CCB is Sanyo's original bus format. All bus addresses are managed by Sanyo for this format.
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## Specifications

**Absolute Maximum Ratings at Ta = 25°C, V<sub>SS</sub> = 0 V**

| Parameter                                                    | Symbol              | Pin name                                                                                                                                                                                                    | Ratings |     |                                              | Unit |
|--------------------------------------------------------------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----|----------------------------------------------|------|
|                                                              |                     |                                                                                                                                                                                                             | min     | typ | max                                          |      |
| Supply voltage<br>(A/D, D/A, volume, etc)                    | V <sub>DDmax1</sub> | AV <sub>DD1</sub> , AV <sub>DD2</sub> , AV <sub>DD5</sub> , AV <sub>DD6</sub> , AV <sub>DD7</sub> , AV <sub>DD8</sub> , AV <sub>DD9</sub> ,<br>AV <sub>DD10</sub> , AV <sub>DD11</sub> , AV <sub>DD12</sub> | −0.3    |     | +6.0                                         | V    |
| Supply voltage (crystal oscillator)                          | V <sub>DDmax2</sub> | XV <sub>DD</sub>                                                                                                                                                                                            | −0.3    |     | +6.0                                         | V    |
| Supply voltage<br>(DSP core block)(I/O I/F, PLL block)       | V <sub>DDmax3</sub> | DV <sub>DD1</sub> , DV <sub>DD2</sub> , DV <sub>DD3</sub> , DV <sub>DD4</sub> , DV <sub>DD5</sub> , DV <sub>DD6</sub> , AV <sub>DD4</sub>                                                                   | −0.3    |     | +4.0                                         | V    |
| Maximum input voltage<br>(A/D, D/A, volume, etc)             | V <sub>IN1</sub>    | AINRP1, AINRN1, AINLP1, AINLN1, AINRP2, AINLP2,<br>AINRP3, AINLP3, AINRP4, AINLP4,<br>VFLI, VFRI, VRLI, VRR1                                                                                                | −0.3    |     | V <sub>DDmax1</sub><br>+ 0.3<br>(max +6.0 V) | V    |
| Maximum input voltage<br>(DSP core block)<br>(I/O I/F block) | V <sub>IN2</sub>    | TEST0, TEST1, TEST2, TEST3, TEST4, TEST5,<br>TEST6, TEST7, TEST8, TEST9, TEST10,<br>TEST13, TEST14, PWDB                                                                                                    | −0.3    |     | V <sub>DDmax3</sub><br>+ 0.3<br>(max +4.0 V) | V    |
|                                                              | V <sub>IN3</sub>    | CL, CE, DI, RSTB, INTB                                                                                                                                                                                      | −0.3    |     | +6.0                                         | V    |
| Allowable power dissipation                                  | Pdmax               | (Conditions: Audio disabled operating state, Std. Board<br>installation ; See note)                                                                                                                         |         |     | 830                                          | mW   |
| Maximum output current                                       | I <sub>o</sub>      | DO                                                                                                                                                                                                          | 0       |     | 6.0                                          | mA   |
| Operating temperature                                        | T <sub>opr</sub>    |                                                                                                                                                                                                             | −40     |     | 85                                           | °C   |
| Storage temperature                                          | T <sub>stg</sub>    |                                                                                                                                                                                                             | −55     |     | 125                                          | °C   |

Note Std. board : 114.3 mm × 76.2 mm × 1.5 mm, material ; glass epoxy resin

**Allowable Operating Ranges at Ta = −40 to +85°C, V<sub>SSD</sub> = V<sub>SSA</sub> = 0 V**

| Parameter                              | Symbol              | Pin name                                                                                                                                                                                                    | Ratings                   |         |                           | Unit |
|----------------------------------------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|---------|---------------------------|------|
|                                        |                     |                                                                                                                                                                                                             | min                       | typ     | max                       |      |
| Supply voltage<br>(analog block)       | AV <sub>DD5</sub>   | AV <sub>DD1</sub> , AV <sub>DD2</sub> , AV <sub>DD5</sub> , AV <sub>DD6</sub> , AV <sub>DD7</sub> , AV <sub>DD8</sub> , AV <sub>DD9</sub> ,<br>AV <sub>DD10</sub> , AV <sub>DD11</sub> , AV <sub>DD12</sub> | +4.75                     |         | +5.25                     | V    |
| Supply voltage (crystal oscillator)    | XV <sub>DD5</sub>   | XV <sub>DD</sub>                                                                                                                                                                                            | +4.75                     |         | +5.25                     | V    |
| Supply voltage<br>(digital block, PLL) | DV <sub>DD3.3</sub> | DV <sub>DD1</sub> , DV <sub>DD2</sub> , DV <sub>DD3</sub> , DV <sub>DD4</sub> , DV <sub>DD5</sub> , DV <sub>DD6</sub> , AV <sub>DD4</sub>                                                                   | +3.0                      |         | +3.6                      | V    |
| High-level input voltage               | V <sub>IHD</sub>    | PWDB, INITB, TEST0, TEST1, TEST2, TEST3, TEST4,<br>TEST5, TEST6, TEST7, TEST8, TEST9, TEST10,<br>TEST13, TEST14                                                                                             | 0.7 × DV <sub>DD3.3</sub> |         | DV <sub>DD3.3</sub>       | V    |
|                                        | V <sub>IHD1</sub>   | CL, CE, DI, RSTB                                                                                                                                                                                            | 0.7 × AV <sub>DD5</sub>   |         | AV <sub>DD5</sub>         | V    |
| Low-level input voltage                | V <sub>ILD</sub>    | PWDB, INITB, TEST0, TEST1, TEST2, TEST3, TEST4,<br>TEST5, TEST6, TEST7, TEST8, TEST9, TEST10,<br>TEST13, TEST14                                                                                             | V <sub>SS</sub>           |         | 0.3 × DV <sub>DD3.3</sub> | V    |
|                                        | V <sub>ILD1</sub>   | CL, CE, DI, RSTB                                                                                                                                                                                            | V <sub>SS</sub>           |         | 0.3 × AV <sub>DD5</sub>   | V    |
| Full-scale input level                 |                     | AINRP1, AINRN1, AINLP1, AINLN1, AINRP2,<br>AINLP2, AINRP3, AINLP3, AINRP4, AINLP4                                                                                                                           |                           |         | 0.4 × AV <sub>DD5</sub>   | Vp-p |
| Crystal oscillator frequency *         |                     | X <sub>IN</sub> , X <sub>OUT</sub>                                                                                                                                                                          |                           | 16.9344 |                           | MHz  |

Note\*: Consult with the manufacturer of the crystal oscillator element used to verify that the circuit constant values are appropriate for that crystal oscillator element before using this circuit.

**Electrical Characteristics in the Allowable Operating Ranges**

| Parameter                 | Symbol                  | Pin name                                                                                                                                        | Ratings |                       |      | Unit          |
|---------------------------|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----------------------|------|---------------|
|                           |                         |                                                                                                                                                 | min     | typ                   | max  |               |
| High-level input current  | $I_{IH}$                | PWDB, RSTB, INTB, CE, CL, DI, TEST0, TEST1, TEST2, TEST3, TEST4, TEST5, TEST6, TEST7, TEST8, TEST9, TEST10, TEST13, TEST14                      |         |                       | 5    | $\mu\text{A}$ |
| Low-level input current   | $I_{IL}$                | PWDB, RSTB, INTB, CE, CL, DI, TEST0, TEST1, TEST2, TEST3, TEST4, TEST5, TEST6, TEST7, TEST8, TEST9, TEST10, TEST13, TEST14                      | -5      |                       |      | $\mu\text{A}$ |
| High-level output voltage | $V_{OH}$                | BUSY, DO, TEST11, TEST12 (Microcontroller: 5 V)                                                                                                 | 4.5     |                       | 5.5  | V             |
|                           |                         | BUSY, DO, TEST11, TEST12 (Microcontroller: 3.3 V)                                                                                               | 3.0     |                       | 3.6  | V             |
| Low-level output voltage  | $V_{OL}$                | BUSY, DO, TEST11, TEST12                                                                                                                        |         |                       | 0.5  | V             |
| Analog output level       | $V_{OUT}$               | AOUT1, AOUT2, AOUT3, AOUT4                                                                                                                      |         | $0.6 \times AV_{DD5}$ |      | $V_{P-P}$     |
| Reference voltage output  | Vref1<br>Vref2<br>Vref3 | Vref1, Vref2, Vref3                                                                                                                             | 2.35    | 2.5                   | 2.65 | V             |
| Current drain             | $I_{AVDD5}$             | (Conditions: Audio disabled operating state, Std. board installed ; See note)<br>$AV_{DD5} = X_{VDD5} = 5\text{V}$ , $D_{VDD3.3} = 3.3\text{V}$ |         | 55                    | 72   | mA            |
|                           | $I_{XVDD5}$             | (Conditions: Audio disabled operating state, Std. board installed ; See note)<br>$AV_{DD5} = X_{VDD5} = 5\text{V}$ , $D_{VDD3.3} = 3.3\text{V}$ |         | 5                     | 7    | mA            |
|                           | $I_{DVDD3.3}$           | (Conditions: Audio disabled operating state, Std. board installed ; See note)<br>$AV_{DD5} = X_{VDD5} = 5\text{V}$ , $D_{VDD3.3} = 3.3\text{V}$ |         | 65                    | 85   | mA            |
| Power dissipation         | $P_d$                   | (Conditions: Audio disabled operating state, Std. board installed ; See note)<br>$AV_{DD5} = X_{VDD5} = 5\text{V}$ , $D_{VDD3.3} = 3.3\text{V}$ |         | 515                   | 680  | mW            |

Note Std. board : 114.3 mm × 76.2 mm × 1.5 mm, material : glass epoxy resin

**LC75010W Analog Characteristics**

Conditions: Analog system: 5 V, digital system: 3.3 V, fs: 44.1 kHz, signal frequency: 1 kHz, from the analog source selector input to the volume control circuit output.

Measurement band: 10 Hz to 20 kHz, using the SANYO-specified DSP evaluation board.

Test circuit: LC75010W external circuit structure with the DSP operating in through mode (4-bit shiftup), room temperature

Test equipment: Audio analyzer (Rohde & Schwarz UPD)

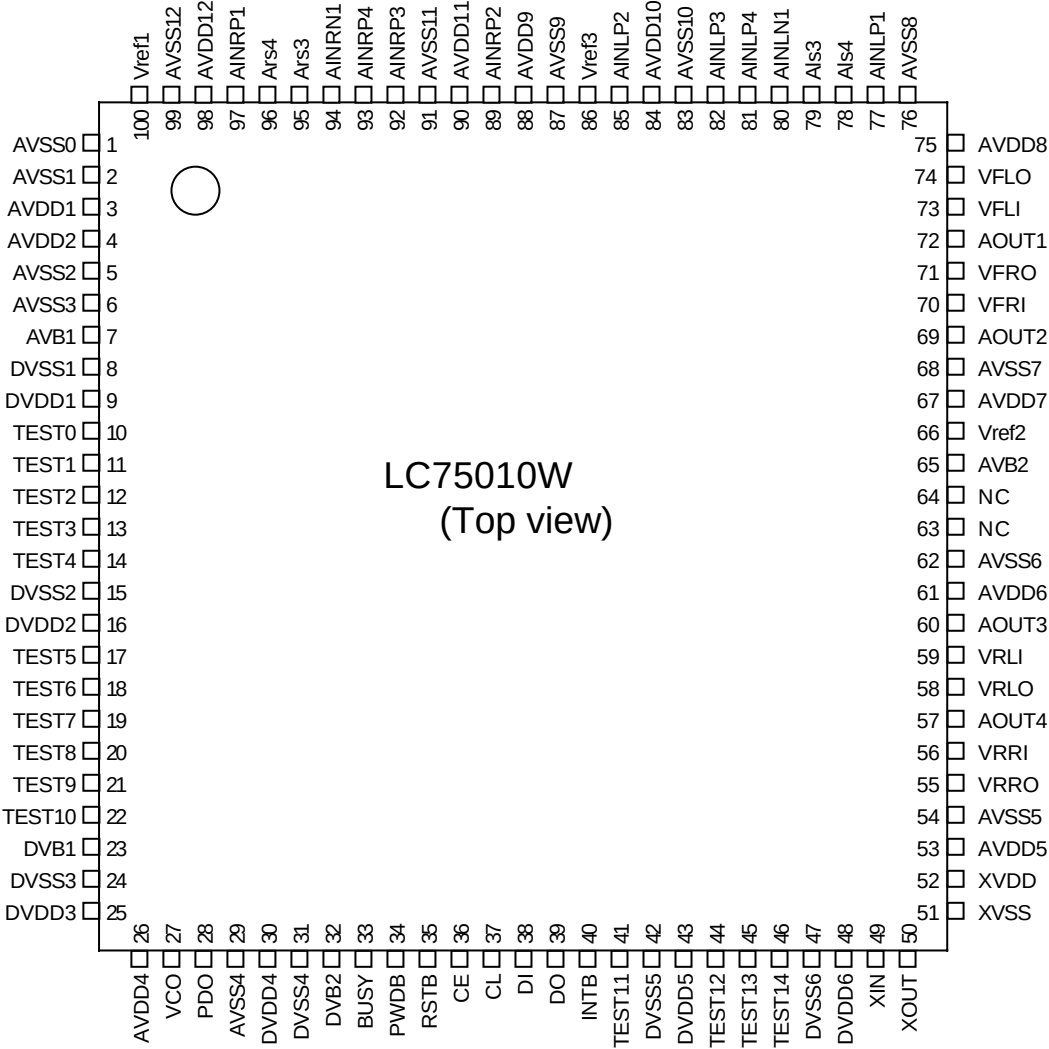
| Parameter     | Conditions                            | Ratings |     |     | Unit |
|---------------|---------------------------------------|---------|-----|-----|------|
|               |                                       | min     | typ | max |      |
| S/N           | A-weighted, Input conditions: 2 Vp-p  | 85      | 90  | —   | dB   |
| Dynamic range | A-weighted                            | 85      | 90  | —   | dB   |
| THD+N         | Input conditions: 1.5 Vp-p. See note. | —       | -86 | -80 | dB   |

Note: THD+N shows the optimal characteristics for an input (1.5 Vp-p) that is 3 dB lower than the full-scale input level.

**CCB Timing**

| Parameter              | Symbol               | Pin name         | Ratings |     |      | Unit          |
|------------------------|----------------------|------------------|---------|-----|------|---------------|
|                        |                      |                  | min     | typ | max  |               |
| Data setup time        | $t_{SU}$             | DI, CL           | 0.75    |     |      | $\mu\text{s}$ |
| Data hold time         | $t_{HD}$             | DI, CL           | 0.75    |     |      | $\mu\text{s}$ |
| Clock low-level time   | $t_{CL}$             | CL               | 0.75    |     |      | $\mu\text{s}$ |
| Clock high-level time  | $t_{CH}$             | CL               | 0.75    |     |      | $\mu\text{s}$ |
| CE wait time           | $t_{EL}$             | CE, CL           | 0.75    |     |      | $\mu\text{s}$ |
| CE setup time          | $t_{ES}$             | CE, CL           | 0.75    |     |      | $\mu\text{s}$ |
| CE hold time           | $t_{EH}$             | CE, CL           | 0.75    |     |      | $\mu\text{s}$ |
| Data latch change time | $t_{LC}$             |                  |         |     | 0.75 | $\mu\text{s}$ |
| Data output time       | $t_{DC}$<br>$t_{DH}$ | DO, CL<br>DO, CE |         |     | 0.35 | $\mu\text{s}$ |

Pin Assignments



**Pin Functions**

| Pin No. | Pin name | Input/Output (I/O) | Function                                                                                                                                                                                                                                                                                                                                  |
|---------|----------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 97      | AINRP1   | I                  | Analog BTL input (Rch +)                                                                                                                                                                                                                                                                                                                  |
| 94      | AINRN1   | I                  | Analog BTL input (Rch -)                                                                                                                                                                                                                                                                                                                  |
| 77      | AINLP1   | I                  | Analog BTL input (Lch +)                                                                                                                                                                                                                                                                                                                  |
| 80      | AINLN1   | I                  | Analog BTL input (Lch -)                                                                                                                                                                                                                                                                                                                  |
| 89      | AINRP2   | I                  | Analog OTL input1 (Rch +)                                                                                                                                                                                                                                                                                                                 |
| 85      | AINLP2   | I                  | Analog OTL input1 (Lch +)                                                                                                                                                                                                                                                                                                                 |
| 92      | AINRP3   | I                  | Analog OTL input2 (Rch +)                                                                                                                                                                                                                                                                                                                 |
| 82      | AINLP3   | I                  | Analog OTL input2 (Lch +)                                                                                                                                                                                                                                                                                                                 |
| 93      | AINRP4   | I                  | Analog OTL input3 (Rch +)                                                                                                                                                                                                                                                                                                                 |
| 81      | AINLP4   | I                  | Analog OTL input3 (Lch +)                                                                                                                                                                                                                                                                                                                 |
| 34      | PWDB     | I                  | Standby mode (active low)<br>Setting the PWDB pin to the low level sets the LC75010W to standby mode (also know as "power down mode").<br>In standby mode, the DSP system clock and the crystal oscillator are stopped and the whole LC75010W goes to the stopped state. This pin must be held at the high level during normal operation. |
| 35      | RSTB     | I                  | Reset (active low)<br>A reset is normally applied at power on, after recovering from a temporary power outage, and after returning from standby mode ("power down mode").                                                                                                                                                                 |
| 40      | INTB     | I                  | Interrupt (active low) (Software clip input (0/1))<br>Provides feedback control to the DSP to prevent clipping when an overflow occurs in the amplifier output.                                                                                                                                                                           |
| 10      | TEST0    | I/O                | Test pin                                                                                                                                                                                                                                                                                                                                  |
| 11      | TEST1    | I/O                | Test pin                                                                                                                                                                                                                                                                                                                                  |
| 12      | TEST2    | I/O                | Test pin                                                                                                                                                                                                                                                                                                                                  |
| 13      | TEST3    | I/O                | Test pin                                                                                                                                                                                                                                                                                                                                  |
| 14      | TEST4    | I/O                | Test pin                                                                                                                                                                                                                                                                                                                                  |
| 17      | TEST5    | I/O                | Test pin                                                                                                                                                                                                                                                                                                                                  |
| 18      | TEST6    | I/O                | Test pin                                                                                                                                                                                                                                                                                                                                  |
| 19      | TEST7    | I/O                | Test pin                                                                                                                                                                                                                                                                                                                                  |
| 20      | TEST8    | I/O                | Test pin                                                                                                                                                                                                                                                                                                                                  |
| 21      | TEST9    | I/O                | Test pin                                                                                                                                                                                                                                                                                                                                  |
| 22      | TEST10   | I/O                | Test pin                                                                                                                                                                                                                                                                                                                                  |
| 41      | TEST11   | I/O                | Test pin                                                                                                                                                                                                                                                                                                                                  |
| 44      | TEST12   | I/O                | Test pin                                                                                                                                                                                                                                                                                                                                  |
| 45      | TEST13   | I/O                | Test pin                                                                                                                                                                                                                                                                                                                                  |
| 46      | TEST14   | I/O                | Test pin                                                                                                                                                                                                                                                                                                                                  |
| 49      | XIN      | I                  | Crystal input (384 fs = 16.9344 MHz) (fs = 44.1 kHz)                                                                                                                                                                                                                                                                                      |
| 50      | XOUT     | O                  | Crystal output                                                                                                                                                                                                                                                                                                                            |
| 27      | VCO      | I                  | VCO control                                                                                                                                                                                                                                                                                                                               |
| 28      | PDO      | O                  | Charge pump output                                                                                                                                                                                                                                                                                                                        |
| 36      | CE       | I                  | CCB enable                                                                                                                                                                                                                                                                                                                                |
| 37      | CL       | I                  | CCB clock                                                                                                                                                                                                                                                                                                                                 |
| 38      | DI       | I                  | Data in                                                                                                                                                                                                                                                                                                                                   |
| 39      | DO       | O                  | Data out                                                                                                                                                                                                                                                                                                                                  |
| 33      | BUSY     | O                  | CCB ready monitor<br>Outputs the state of the DSP CCB receive buffer.<br>A low-level output from the BUSY pin indicates that the buffer is empty.<br>A high-level output indicates that command data is present in the receive buffer.                                                                                                    |
| 74      | VFLO     | O                  | Volume front Lch output                                                                                                                                                                                                                                                                                                                   |
| 73      | VFLI     | I                  | Volume front Lch input                                                                                                                                                                                                                                                                                                                    |
| 71      | VFRO     | O                  | Volume front Rch output                                                                                                                                                                                                                                                                                                                   |
| 70      | VFRI     | I                  | Volume front Rch input                                                                                                                                                                                                                                                                                                                    |
| 58      | VRLO     | O                  | Volume rear Lch output                                                                                                                                                                                                                                                                                                                    |
| 59      | VRLI     | I                  | Volume rear Lch input                                                                                                                                                                                                                                                                                                                     |
| 55      | VRRO     | O                  | Volume rear Rch output                                                                                                                                                                                                                                                                                                                    |
| 56      | VRRI     | I                  | Volume rear Rch input                                                                                                                                                                                                                                                                                                                     |

Continued on next page.

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| Pin No. | Pin name            | Input/Output (I/O) | Function                        |
|---------|---------------------|--------------------|---------------------------------|
| 100     | Vref1               |                    | Reference voltage               |
| 66      | Vref2               |                    | Reference voltage               |
| 86      | Vref3               |                    | Reference voltage               |
| 72      | AOUT1               | O                  | Analog out 1                    |
| 69      | AOUT2               | O                  | Analog out 2                    |
| 60      | AOUT3               | O                  | Analog out 3                    |
| 57      | AOUT4               | O                  | Analog out 4                    |
| 9       | DV <sub>DD</sub> 1  |                    | Digital V <sub>DD</sub> (3.3 V) |
| 16      | DV <sub>DD</sub> 2  |                    | Digital V <sub>DD</sub> (3.3 V) |
| 25      | DV <sub>DD</sub> 3  |                    | Digital V <sub>DD</sub> (3.3 V) |
| 30      | DV <sub>DD</sub> 4  |                    | Digital V <sub>DD</sub> (3.3 V) |
| 43      | DV <sub>DD</sub> 5  |                    | Digital V <sub>DD</sub> (3.3 V) |
| 48      | DV <sub>DD</sub> 6  |                    | Digital V <sub>DD</sub> (3.3 V) |
| 8       | DV <sub>SS</sub> 1  |                    | Digital V <sub>SS</sub>         |
| 15      | DV <sub>SS</sub> 2  |                    | Digital V <sub>SS</sub>         |
| 24      | DV <sub>SS</sub> 3  |                    | Digital V <sub>SS</sub>         |
| 31      | DV <sub>SS</sub> 4  |                    | Digital V <sub>SS</sub>         |
| 42      | DV <sub>SS</sub> 5  |                    | Digital V <sub>SS</sub>         |
| 47      | DV <sub>SS</sub> 6  |                    | Digital V <sub>SS</sub>         |
| 29      | AV <sub>SS</sub> 4  |                    | Digital V <sub>SS</sub>         |
| 23      | DVB1                |                    | Digital board GND               |
| 32      | DVB2                |                    | Digital board GND               |
| 3       | AV <sub>DD</sub> 1  |                    | Analog V <sub>DD</sub> (5 V)    |
| 4       | AV <sub>DD</sub> 2  |                    | Analog V <sub>DD</sub> (5 V)    |
| 53      | AV <sub>DD</sub> 5  |                    | Analog V <sub>DD</sub> (5 V)    |
| 61      | AV <sub>DD</sub> 6  |                    | Analog V <sub>DD</sub> (5 V)    |
| 67      | AV <sub>DD</sub> 7  |                    | Analog V <sub>DD</sub> (5 V)    |
| 75      | AV <sub>DD</sub> 8  |                    | Analog V <sub>DD</sub> (5 V)    |
| 88      | AV <sub>DD</sub> 9  |                    | Analog V <sub>DD</sub> (5 V)    |
| 84      | AV <sub>DD</sub> 10 |                    | Analog V <sub>DD</sub> (5 V)    |
| 90      | AV <sub>DD</sub> 11 |                    | Analog V <sub>DD</sub> (5 V)    |
| 98      | AV <sub>DD</sub> 12 |                    | Analog V <sub>DD</sub> (5 V)    |
| 26      | AV <sub>DD</sub> 4  |                    | Digital V <sub>DD</sub> (3.3 V) |
| 1       | AV <sub>SS</sub> 0  |                    | Analog V <sub>SS</sub>          |
| 2       | AV <sub>SS</sub> 1  |                    | Analog V <sub>SS</sub>          |
| 5       | AV <sub>SS</sub> 2  |                    | Analog V <sub>SS</sub>          |
| 6       | AV <sub>SS</sub> 3  |                    | Analog V <sub>SS</sub>          |
| 54      | AV <sub>SS</sub> 5  |                    | Analog V <sub>SS</sub>          |
| 62      | AV <sub>SS</sub> 6  |                    | Analog V <sub>SS</sub>          |
| 68      | AV <sub>SS</sub> 7  |                    | Analog V <sub>SS</sub>          |
| 76      | AV <sub>SS</sub> 8  |                    | Analog V <sub>SS</sub>          |
| 87      | AV <sub>SS</sub> 9  |                    | Analog V <sub>SS</sub>          |
| 83      | AV <sub>SS</sub> 10 |                    | Analog V <sub>SS</sub>          |
| 91      | AV <sub>SS</sub> 11 |                    | Analog V <sub>SS</sub>          |
| 99      | AV <sub>SS</sub> 12 |                    | Analog V <sub>SS</sub>          |
| 7       | AVB1                |                    | Analog Board GND                |
| 65      | AVB2                |                    | Analog Board GND                |
| 52      | XV <sub>DD</sub>    |                    | OSC V <sub>DD</sub> (5 V)       |
| 51      | XV <sub>SS</sub>    |                    | OSC V <sub>SS</sub>             |
| 95      | Ars3                |                    | Analog Rch source control       |
| 96      | Ars4                |                    | Analog Rch source control       |
| 79      | Als3                |                    | Analog Lch source control       |
| 78      | Als4                |                    | Analog Lch source control       |

The diagram illustrates the internal architecture of the ADSP-21474 DSP. The central components are the DSP CORE (24 bits), Program ROM (8 kw), and Data RAM (896W). The system is powered by DVDD (3.3V), DVSS, AVDD (5V), and AVSS, with a VREF pin. The output is connected to AOUT1, AOUT2, AOUT3, and AOUT4, which are connected to VFLI, VFRI, VRLI, and VRRI respectively. The input is connected to AINLP1, AINLP2, AINLP3, and AINLP4, which are connected to AINLP1, AINLP2, AINLP3, and AINLP4 respectively. The system is also connected to VCO and PDO pins.

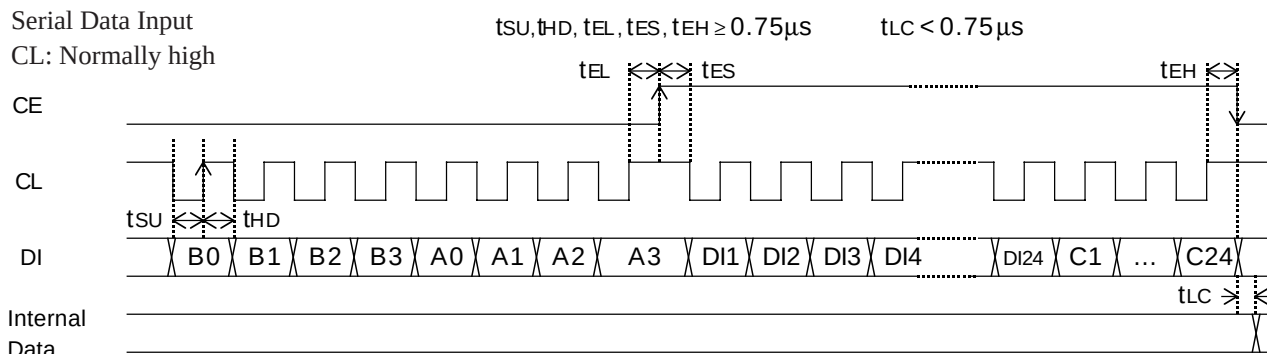
## CCB Control System Timing and Data Format

The LC75010W uses a CCB (Computer Control Bus) serial bus, which is a SANYO-developed bus format.

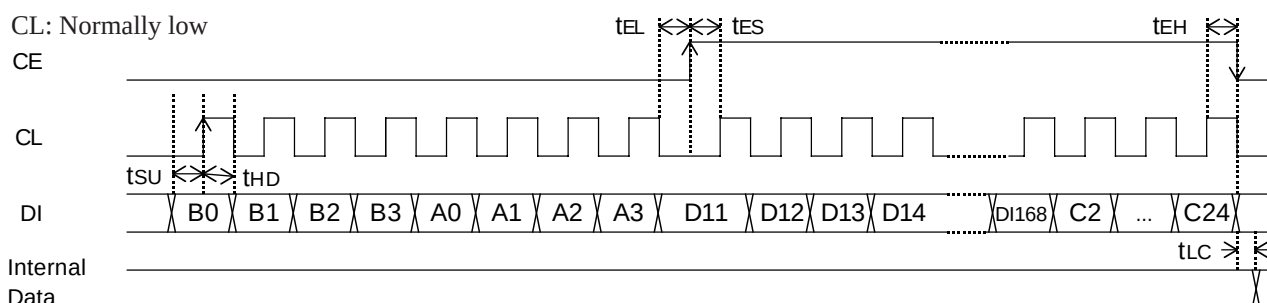
The input serial data consists of a total of  $(8 + DI + C)$  bits. Here, the first 8 bits are the CCB address, the next DI bits are the data bits, and the last C bits are control bits. The output serial data consists of  $(8 + DO)$  bits. Here, the first 8 bits are the CCB address and the next DO bits are the output data bits. Serial data can be input or output after power has been applied, the crystal oscillator and PLL circuits have stabilized, and a reset has been applied.

### Serial Data Input

CL: Normally high

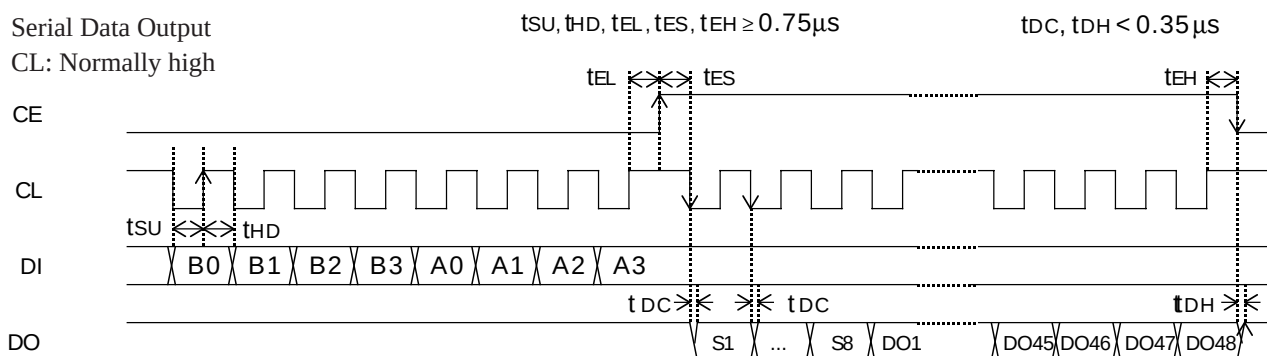


CL: Normally low

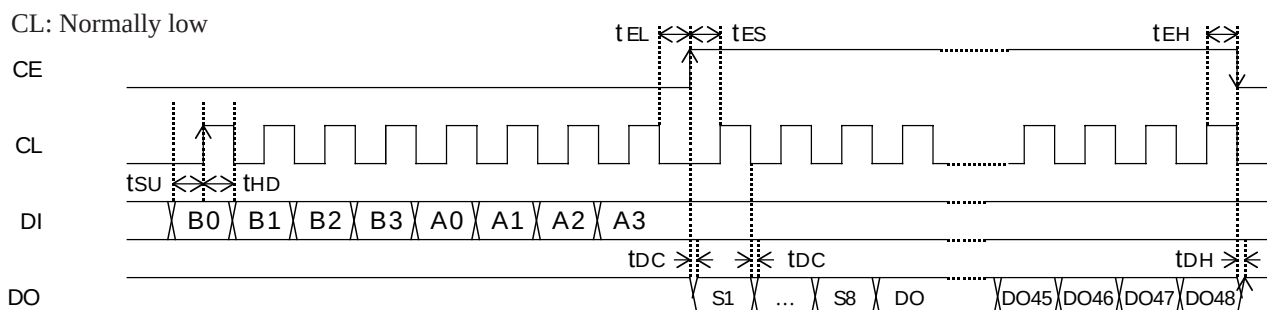


### Serial Data Output

CL: Normally high



CL: Normally low

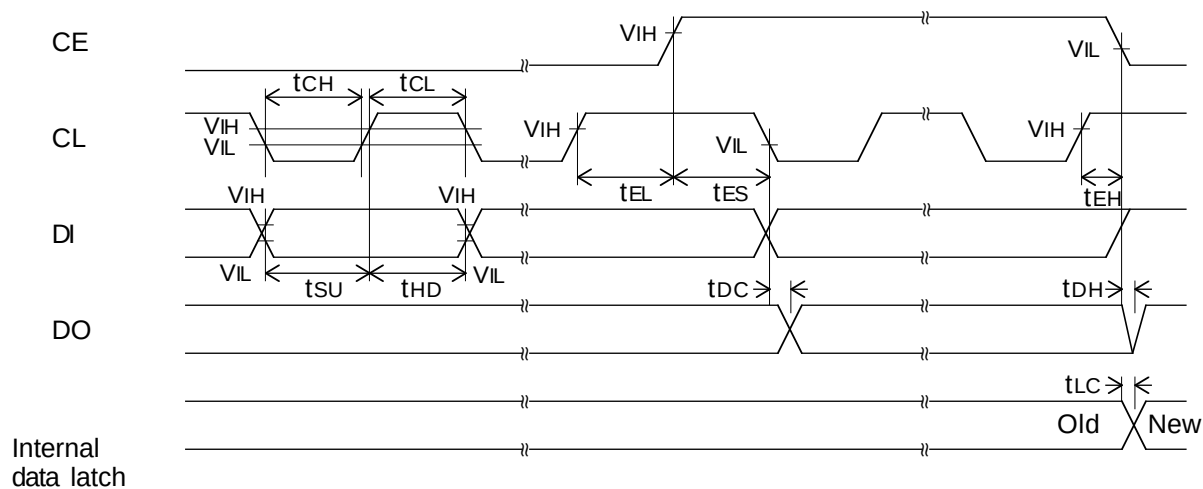


Note: Since the DO pin is an n-channel open-drain output, the data transition times ( $t_{DC}$  and  $t_{DH}$ ) differ depending on the value of the pull-up resistor used.



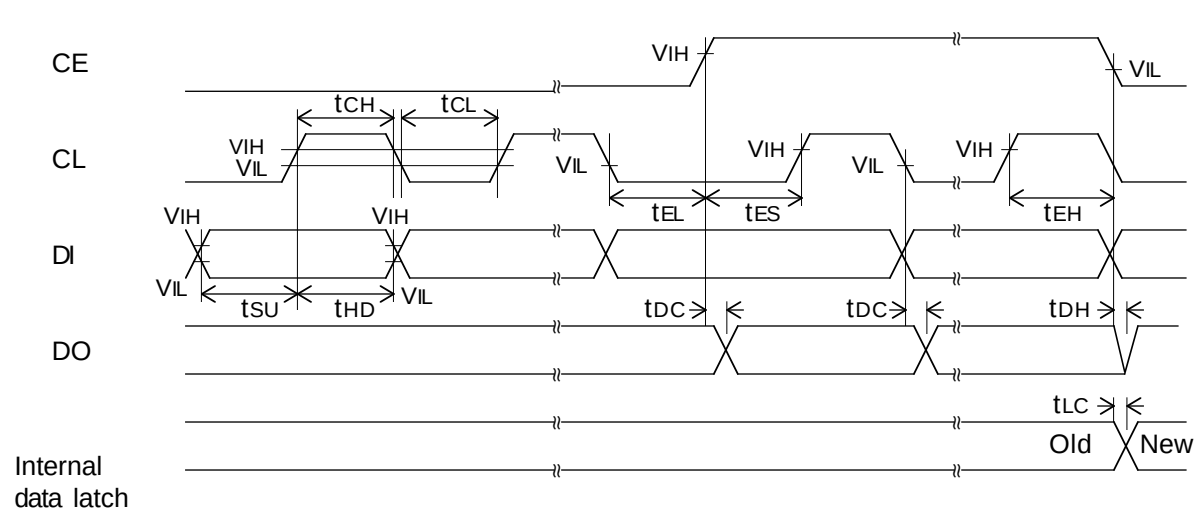
# Serial Data Timing

CL: Normally high



When CL is stopped at the high level

CL: Normally low



When CL is stopped at the low level

## Reset Timing

After power has been applied, and after crystal oscillator operation and PLL circuit operation have stabilized, a reset must be applied at the point that the Vref voltages (Vref1, Vref2, and Vref3) exceed the minimum level of 2.35 V. The reset period must be set up to include a period of at least 0.5  $\mu$ s during which the reset signal is held fixed at the low level. Audio processing (audio input/audio output) cannot be performed during the A/D converter calibration period (100 ms), which directly follows the reset.

## Note on Changes to the DSP Core Main Clock

The LC75010W DSP core main clock can be switched by setting the TEST8 pin either low or high as shown below.

| TEST8                       | DSP core main clock (Crystal oscillator: 16.9344 MHz) |
|-----------------------------|-------------------------------------------------------|
| Low (DV <sub>SS</sub> )     | 38.1024 MHz                                           |
| High (DV <sub>DD</sub> 3.3) | 40.2192 MHz                                           |

## Notes on Filter Coefficient Settings (precision of calculations)

The IIR filter calculations are performed using 24-bit coefficients, 24-bit delay functions,  $24 \times 24 = 48$ -bit multiplications, and  $48 + 48 = 96$ -bit additions.

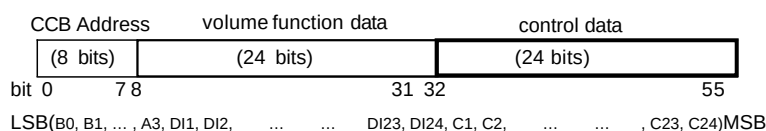
For certain values of the filter coefficients, the precision can become inadequate during the process of the filter calculation. Such errors can result in switching noise occurring when changing between different steps in the volume control.

- \*: This problem can occur when setting the second-order IIR with filter coefficients having low characteristic frequencies (for example, the cutoff frequency or the center frequency). For example, switching noise will occur if the coefficients for a high-pass filter with a cutoff frequency of 25 Hz and a Q of 0.7 are set with FixEQ.) The following workaround can be effective if switching noise occurs due to second-order IIR filter coefficient settings.

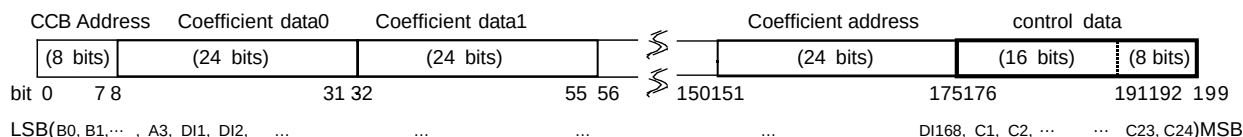
- Increase the characteristic frequency without changing the second-order characteristics, for example, increase the cutoff frequency from 25 Hz to 100 Hz.
- Use the second-order characteristics as the first-order characteristics and define the coefficients for first-order characteristics.

## Serial Input Data Format Examples

### Example 1: Data format for the volume function

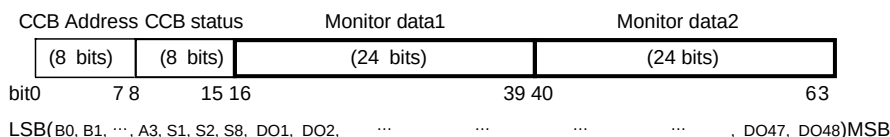


### Example 2: Data format for 24-bit coefficient data (Total: 200 bits maximum)

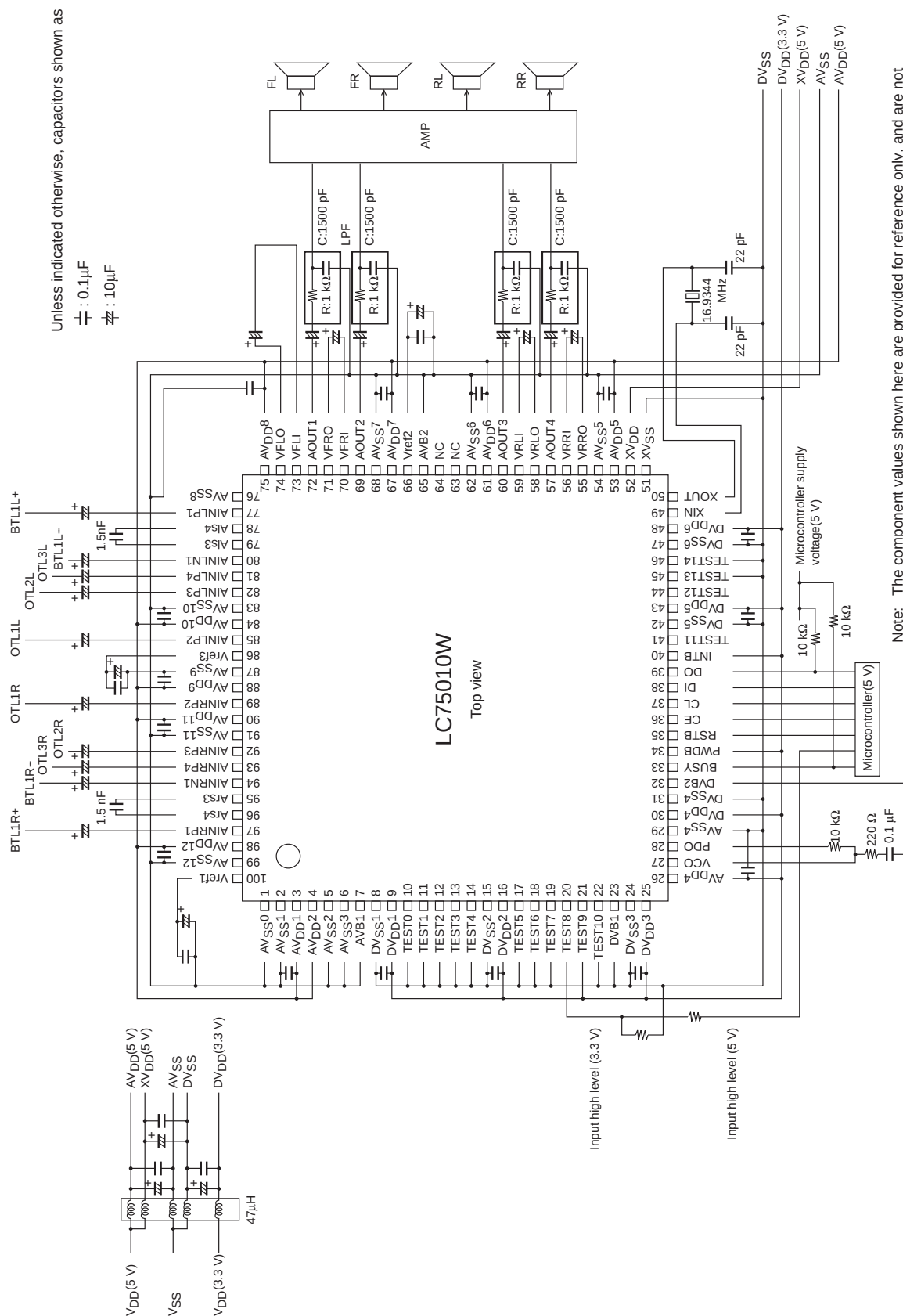


## Serial Output Data Format Example

### Example 1: CCB status register format (Total: 64 bits)



# Peripheral Circuit Example



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