

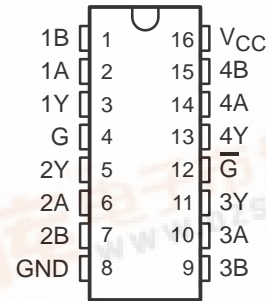
SN75ALS197 QUADRUPLE DIFFERENTIAL LINE RECEIVER

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SLLS045B – JANUARY 1989 – REVISED MAY 1995

- Meets or Exceeds the Requirements of ITU Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- Designed to Operate Up to 20 Mbaud
- 3-State Outputs
- Common-Mode Input Voltage Range – 7 V to 7 V
- Input Sensitivity . . . ± 300 mV
- Input Hysteresis . . . 120 mV Typ
- High-Input Impedance . . . 12 k Ω Min
- Operates from Single 5-V Supply
- Low Supply-Current Requirement 35 mA Max
- Improved Speed and Power Consumption Compared to AM26LS32A

D OR N PACKAGE
(TOP VIEW)



description

The SN75ALS197 is a monolithic, quadruple line receiver with 3-state outputs designed using advanced, low-power, Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication. This, in turn, provides significantly lower power requirements and permits much higher data throughput than other designs. The device meets the specifications of ITU Recommendations V.10, V.11, X.26, and X.27. It features 3-state outputs that permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open.

The device is optimized for balanced, multipoint bus transmission at rates up to 20 megabits per second. The input features high-input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ± 300 mV over a common-mode input voltage range of –7 V to 7 V. It also features active-high and active-low enable functions that are common to the four channels. The SN75ALS197 is designed for optimum performance when used with the SN75ALS192 quadruple differential line driver.

The SN75ALS197 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each receiver)

| DIFFERENTIAL INPUTS A–B | ENABLES | | OUTPUT Y |
|-----------------------------|---------|----------------|-------------|
| | G | \overline{G} | |
| $V_{ID} \geq 0.3$ V | H | X | H |
| | X | L | H |
| -0.3 V < V_{ID} < 0.3 V | H | X | ? |
| | X | L | ? |
| $V_{ID} \leq -0.3$ V | H | X | L |
| | X | L | L |
| X | L | H | Z |
| Open | H | X | H |
| | X | L | H |

H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance (off)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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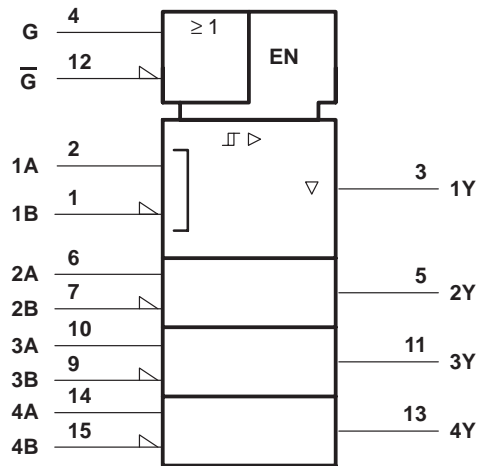
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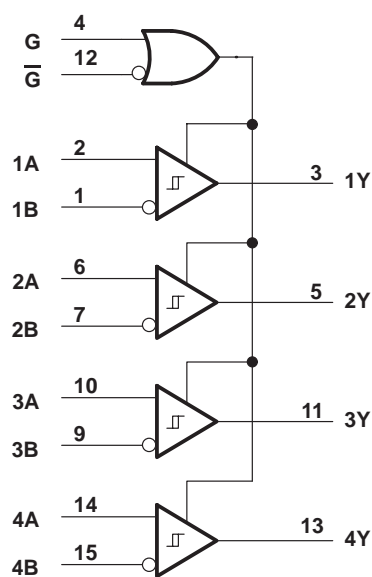
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logic symbol†

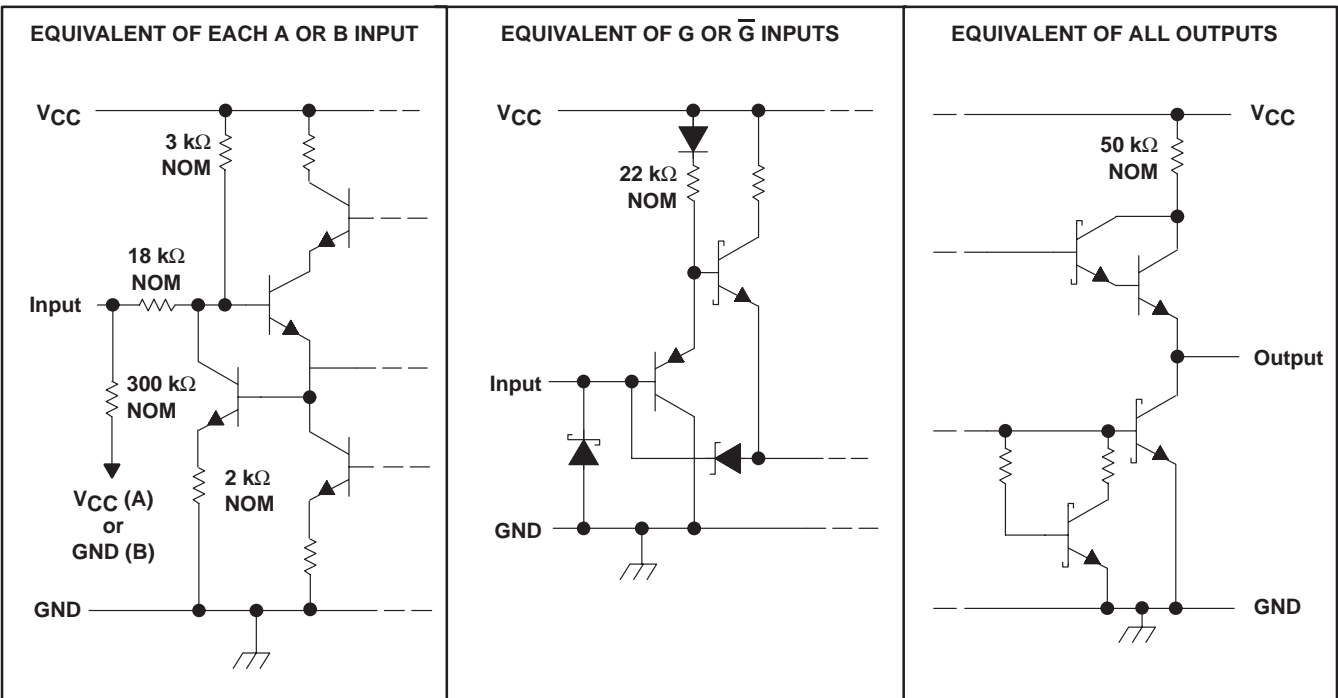


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--------------------------------------------------------------|------------------------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage, V_I (A or B inputs) | ± 15 V |
| Differential input voltage, V_{ID} (see Note 2) | ± 15 V |
| Enable input voltage, V_I | 7 V |
| Low-level output current, I_{OL} | 50 mA |
| Continuous total dissipation | See Dissipation Rating Table |
| Operating free-air temperature range, T_A | 0°C to 70°C |
| Storage temperature range, T_{stg} | – 65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR | $T_A = 70^\circ\text{C}$ POWER RATING |
|---------|---------------------------------------------|--------------------|------------------------------------------|
| D | 950 mW | 7.6 mW/°C | 608 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---------------------------------------|------|-----|----------|---------------|
| Supply voltage, V_{CC} | 4.75 | 5 | 5.25 | V |
| Common-mode input voltage, V_{IC} | | | ± 7 | V |
| Differential input voltage, V_{ID} | | | ± 12 | V |
| High-level input voltage, V_{IH} | 2 | | | V |
| Low-level input voltage, V_{IL} | | | 0.8 | V |
| High-level output current, I_{OH} | | | –400 | μA |
| Low-level output current, I_{OL} | | | 16 | mA |
| Operating free-air temperature, T_A | 0 | | 70 | °C |

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electrical characteristics over recommended range of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|------------------------------------------------------|--------------------------------------------|-------|------|------|------------|
| V_{IT+} Positive-going input threshold voltage | | | | 300 | mV |
| V_{IT-} Negative-going input threshold voltage | | -300‡ | | | mV |
| V_{hys} Hysteresis voltage ($V_{IT+} - V_{IT-}$) | See Figure 4 | | 120 | | mV |
| V_{IK} Enable-input clamp voltage | $I_I = -18$ mA | | | -1.5 | V |
| V_{OH} High-level output voltage | $V_{ID} = 300$ mV, $I_{OH} = -400$ μ A | 2.7 | 3.6 | | V |
| V_{OL} Low-level output voltage | $V_{ID} = -300$ mV | | | 0.45 | V |
| | | | | 0.5 | |
| I_{OZ} High-impedance-state output current | $V_{CC} = 5.25$ V | | | 20 | μ A |
| | | | | -20 | |
| I_I Line input current | Other input at 0 V, See Note 3 | | | 0.7 | mA |
| | | | | -1.0 | |
| I_H High-level enable-input current | | | | 20 | μ A |
| | | | | 100 | |
| I_{IL} Low-level enable-input current | $V_{IL} = 0.4$ V | | | -100 | μ A |
| | Input resistance | 12 | 18 | | k Ω |
| I_{OS} Short-circuit output current§ | $V_{ID} = 3$ V, $V_O = 0$ | -15 | -78 | -130 | mA |
| I_{CC} Supply current | Outputs disabled | | 22 | 35 | mA |

† All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

‡ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 3: Refer to ANSI Standard EIA/TIA-422-B and EIA/TIA-423-B for exact conditions.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------------------------------|--------------------------------------------|-----|-----|-----|------|
| t_{PLH} Propagation delay time, low- to high-level output | $V_{ID} = -2.5$ V to 2.5 V, $C_L = 15$ pF, | 15 | 22 | | ns |
| t_{PHL} Propagation delay time, high- to low-level output | See Figure 2 | 15 | 22 | | ns |
| t_{PZH} Output enable time to high level | $C_L = 15$ pF, See Figure 3 | 13 | 25 | | ns |
| t_{PZL} Output enable time to low level | | 11 | 25 | | |
| t_{PHZ} Output disable time from high level | $C_L = 15$ pF, See Figure 3 | 13 | 25 | | ns |
| t_{PLZ} Output disable time from low level | | 15 | 22 | | |



PARAMETER MEASUREMENT INFORMATION

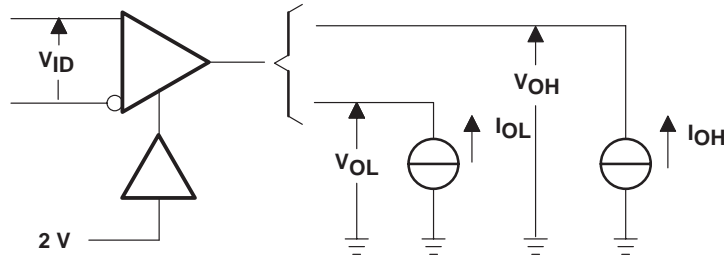
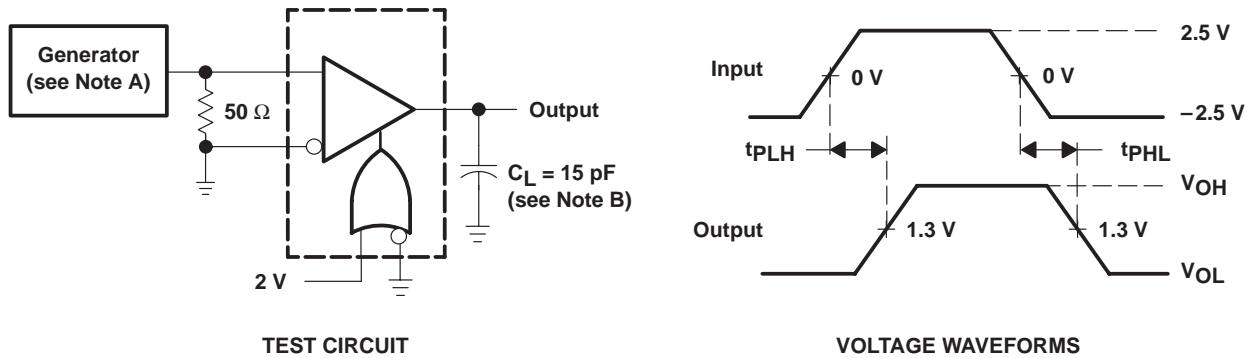


Figure 1. V_{OH} and V_{OL} Test Circuit



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, duty cycle $\leq 50\%$, $Z_O = 50 \Omega$, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$.
B. C_L includes probe and jig capacitance.

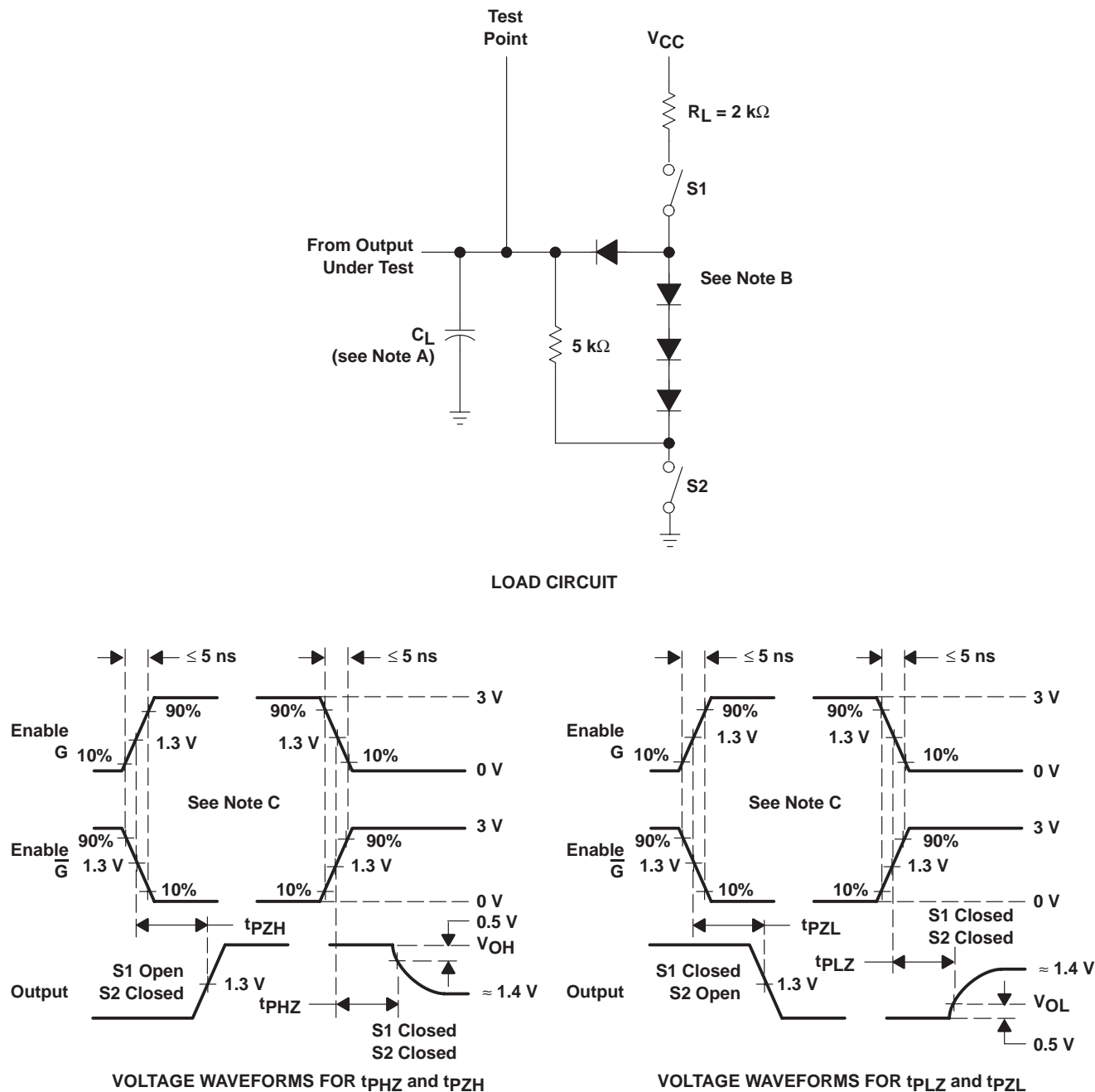
Figure 2. t_{PLH} and t_{PHL} Test Circuit and Voltage Waveforms

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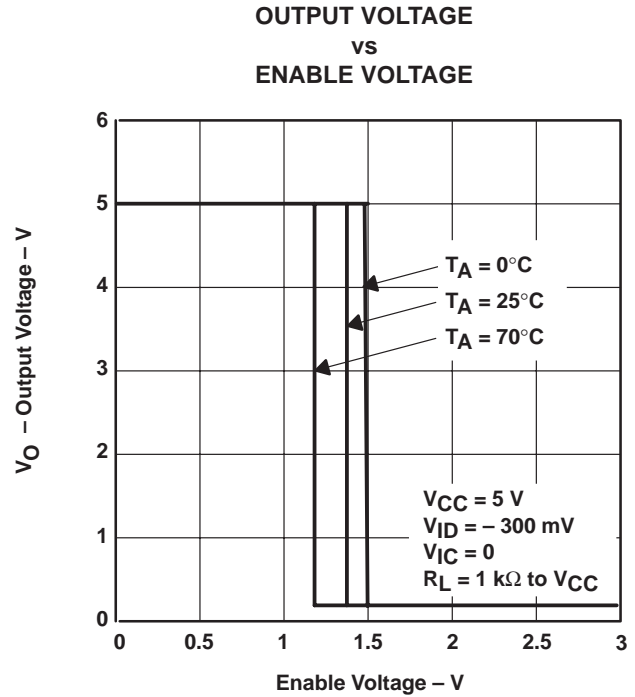
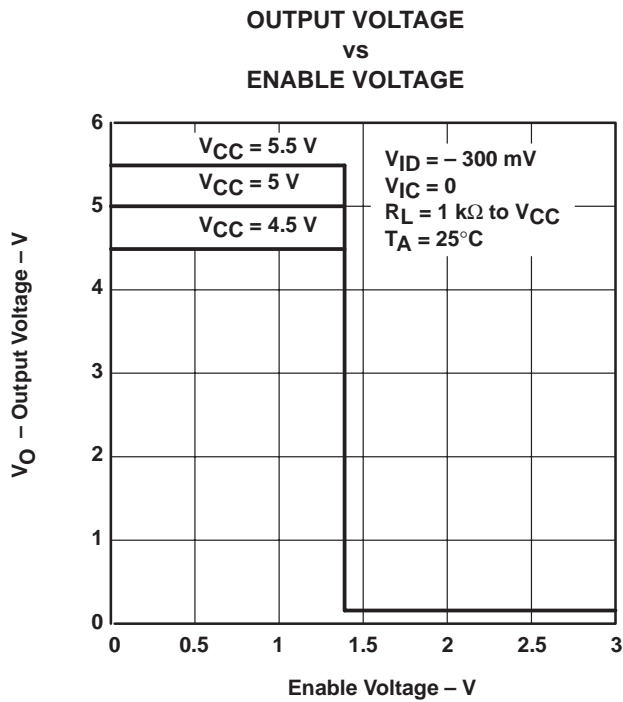
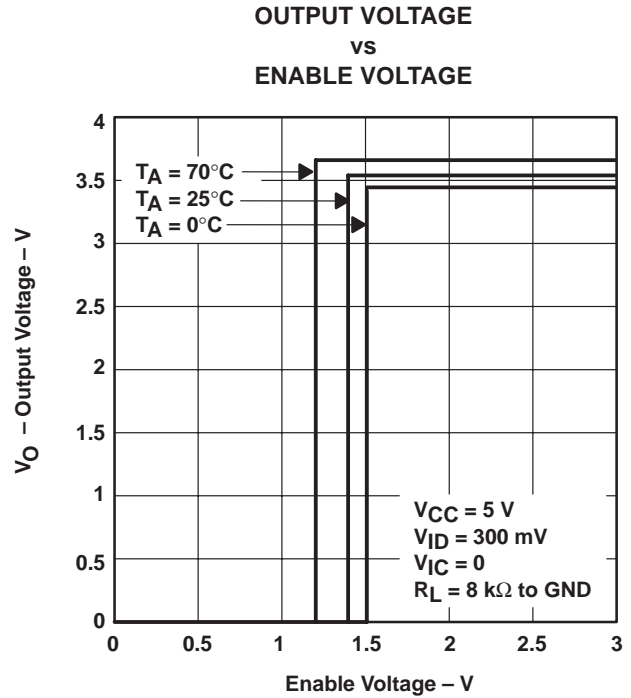
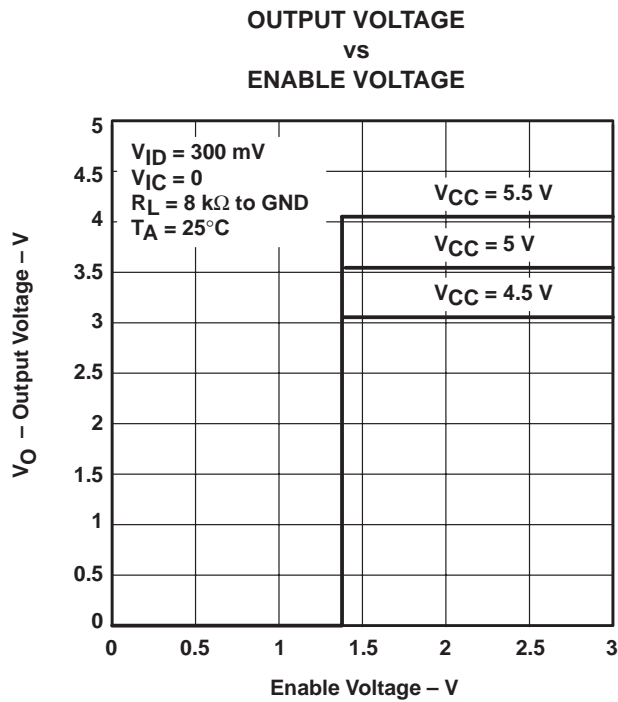
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable \overline{G} is tested with \overline{G} high; G is tested with G low.

Figure 3. t_{PHZ} , t_{PHZ} , t_{PLZ} , and t_{PLZ} Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS



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TYPICAL CHARACTERISTICS

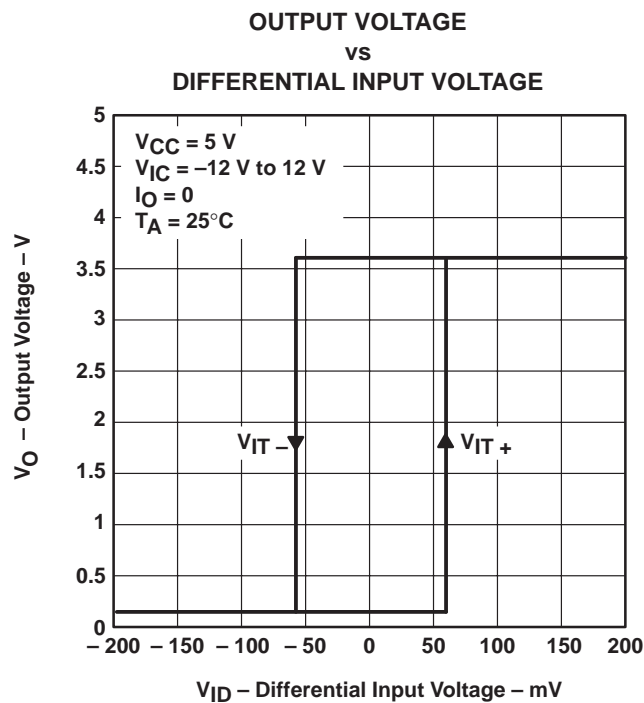


Figure 8

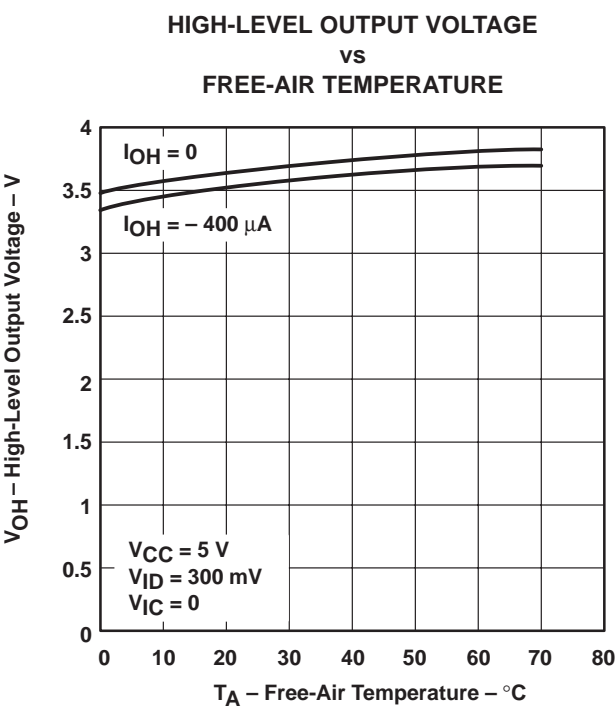


Figure 9

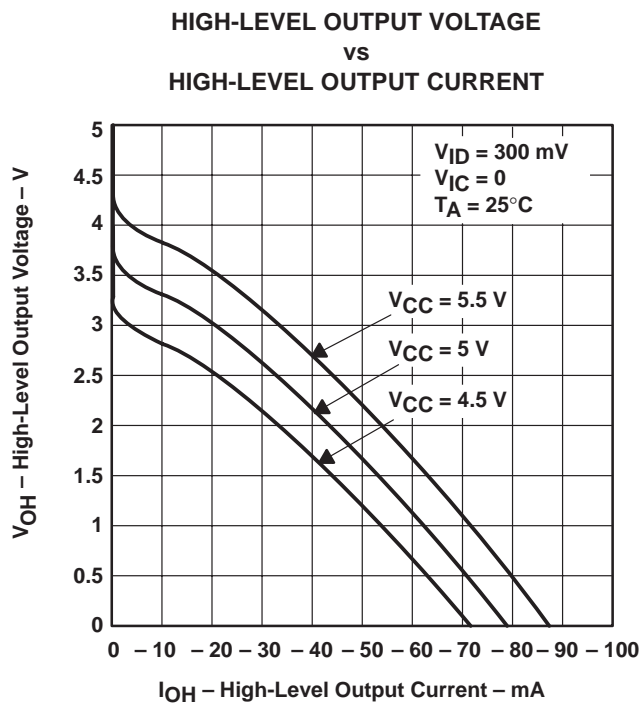


Figure 10

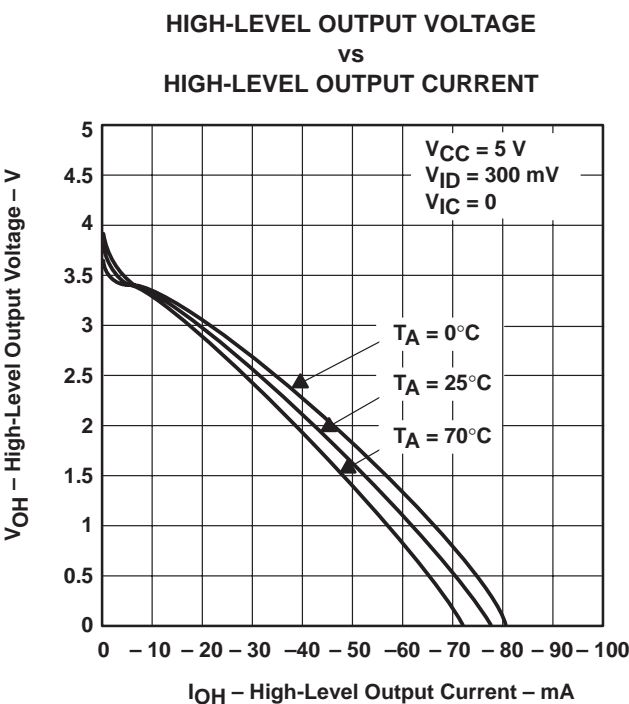


Figure 11

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

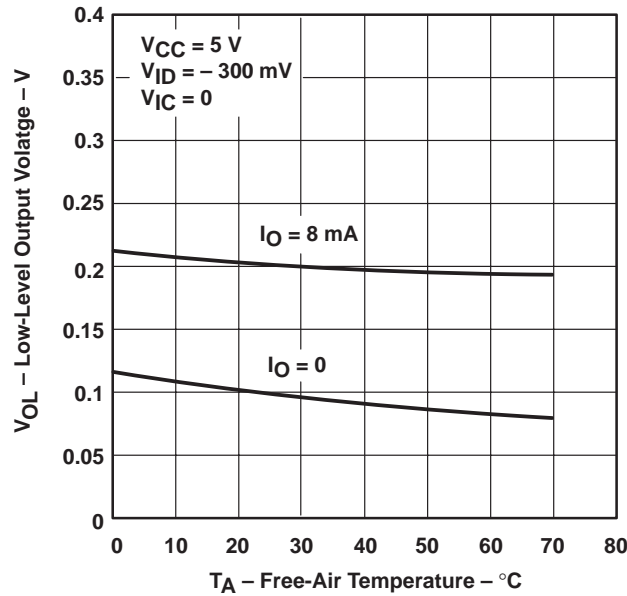


Figure 12

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

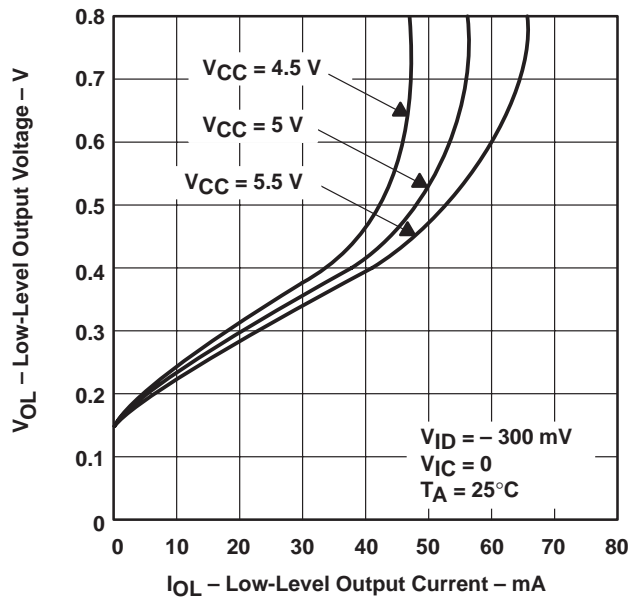


Figure 13

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

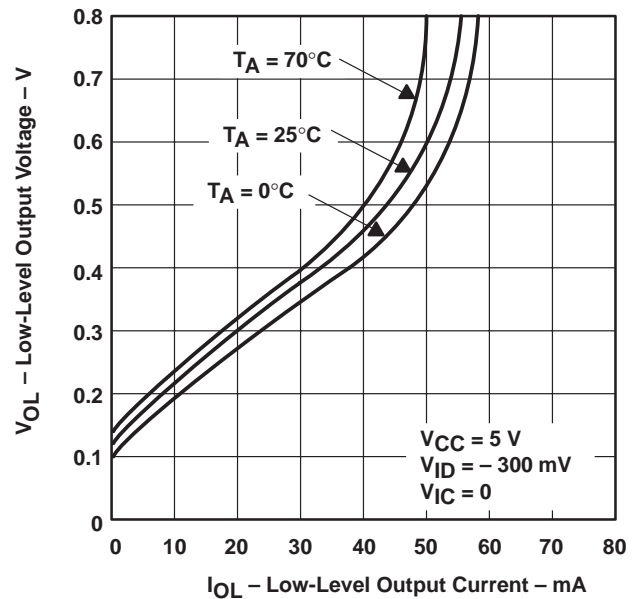


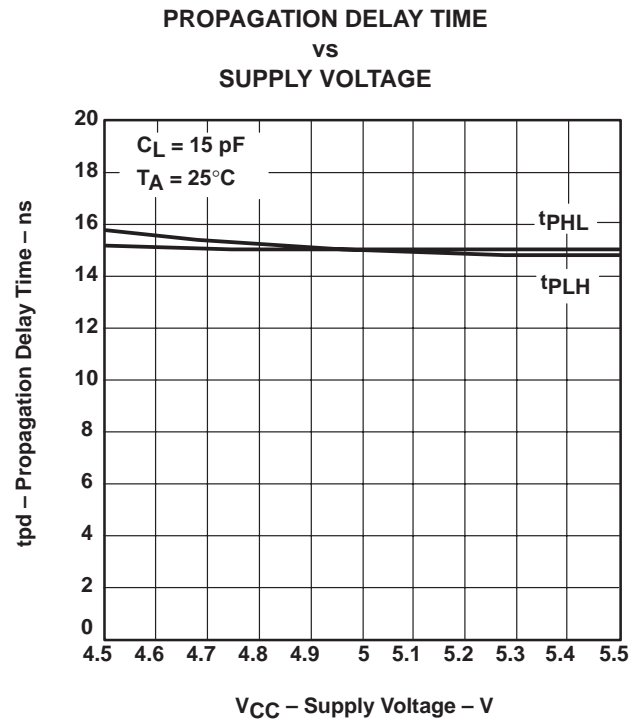
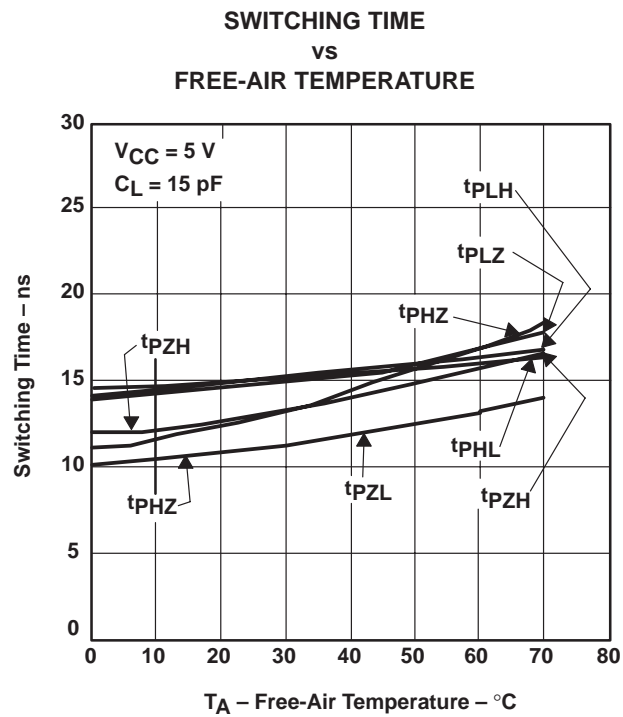
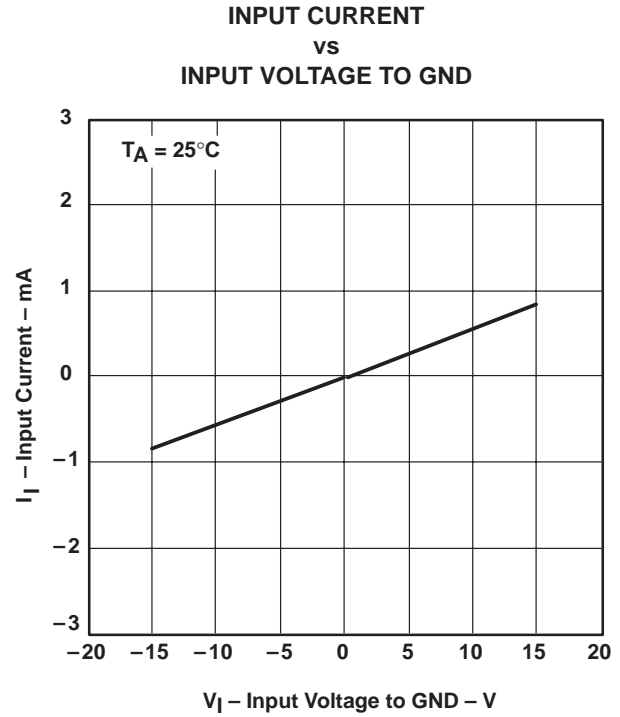
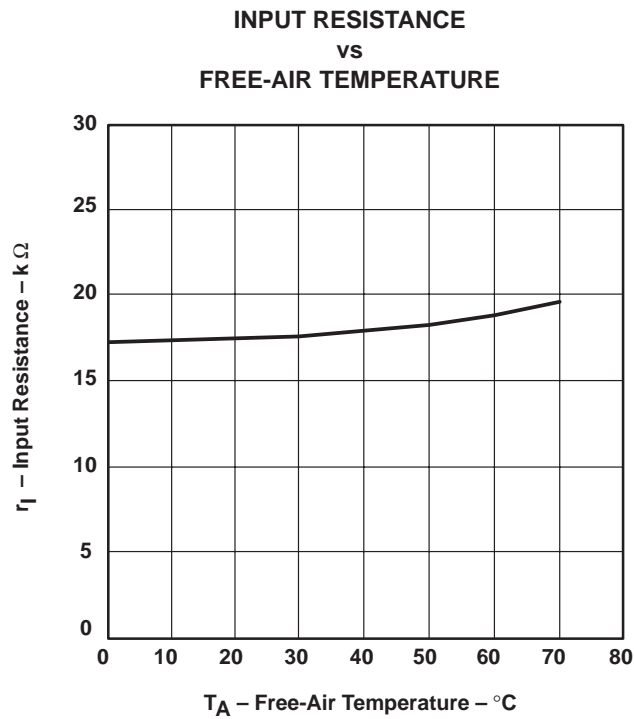
Figure 14

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**SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE**



TYPICAL CHARACTERISTICS



PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN75ALS197D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS197DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS197DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS197DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS197DRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS197DRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS197J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| SN75ALS197N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN75ALS197NE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN75ALS197NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS197NSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS197NSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

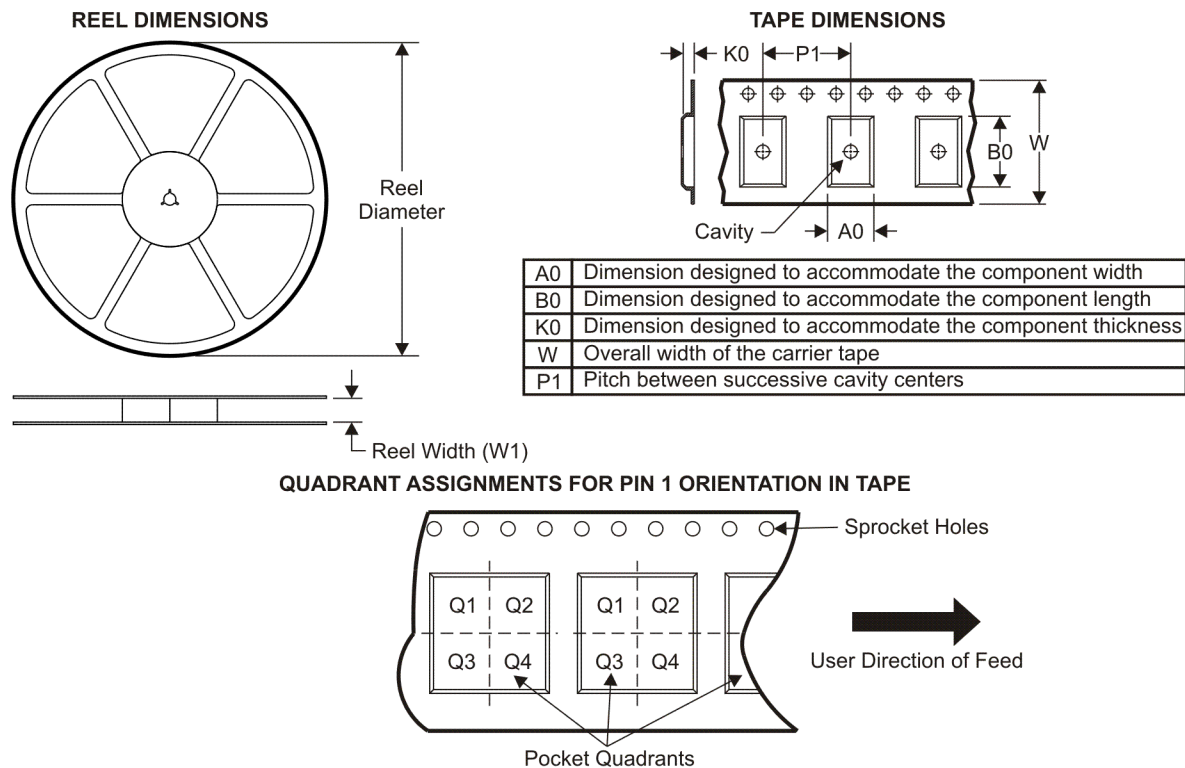
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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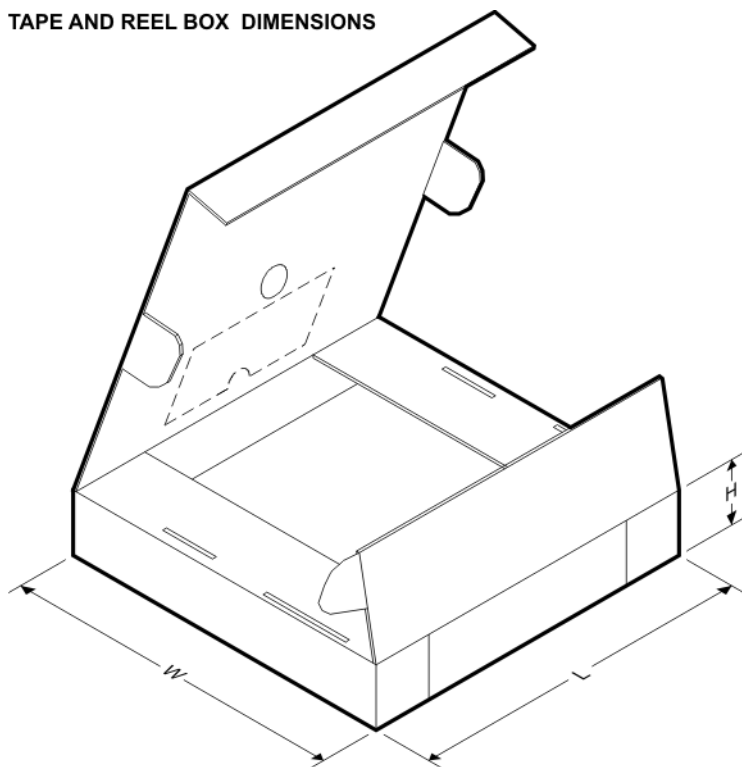
TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN75ALS197DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN75ALS197NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



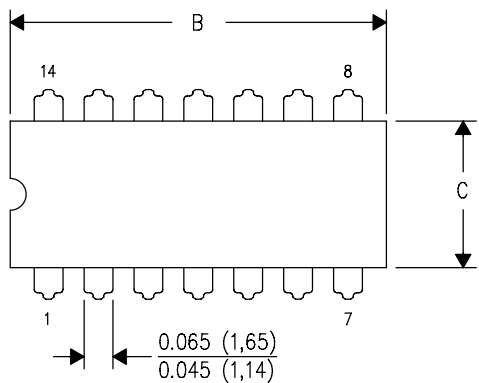
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN75ALS197DR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN75ALS197NSR | SO | NS | 16 | 2000 | 346.0 | 346.0 | 33.0 |

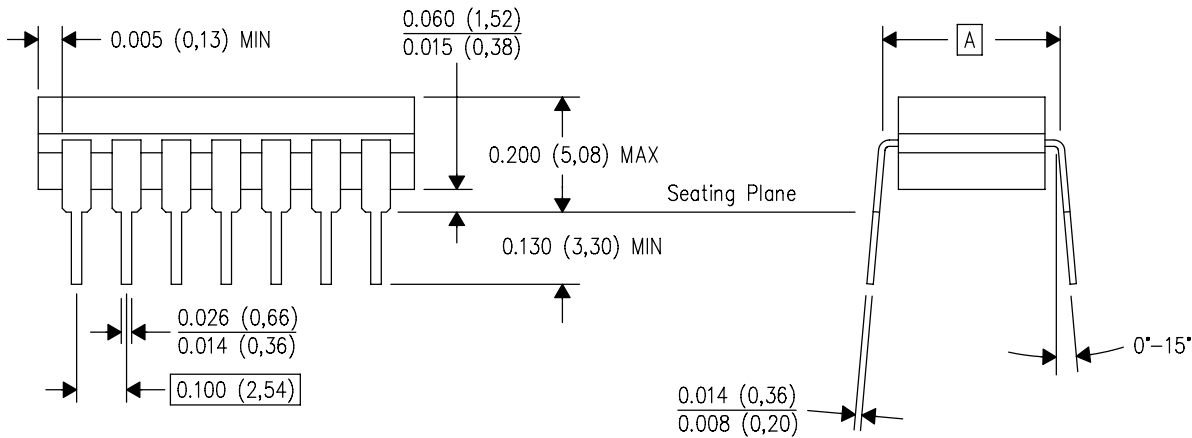
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| PINS ** DIM | 14 | 16 | 18 | 20 |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



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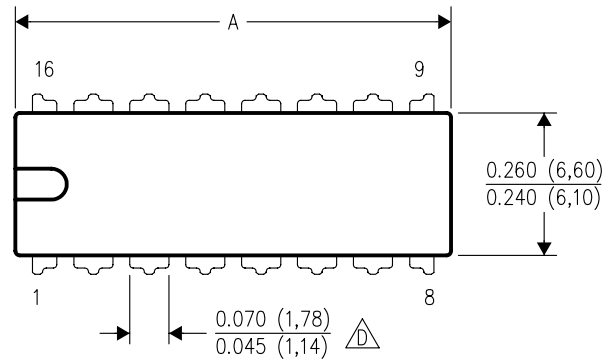
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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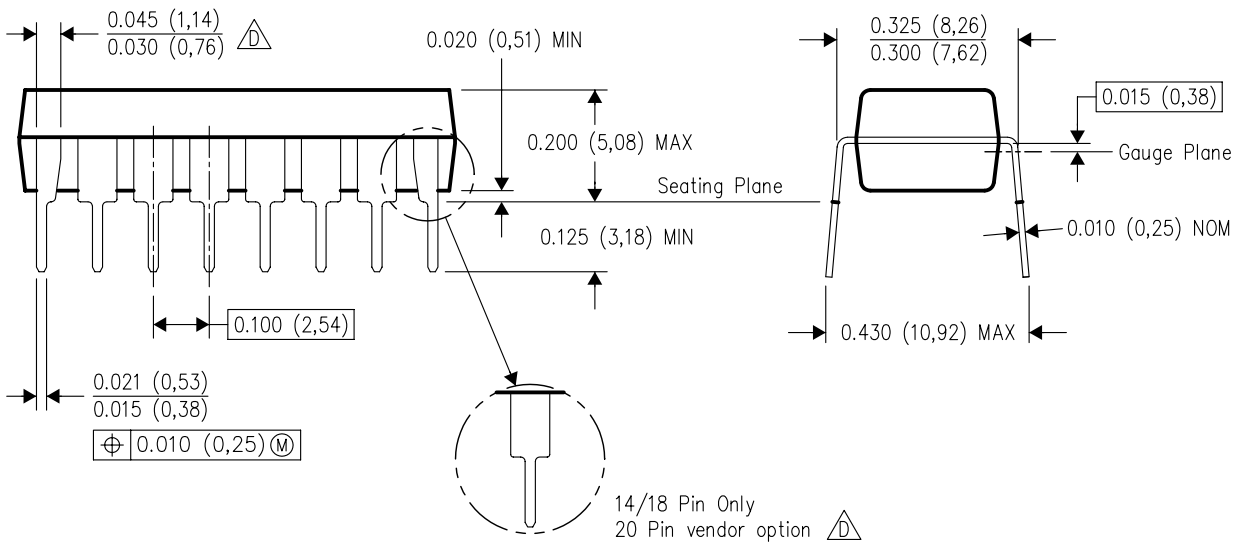
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



| PINS ** | 14 | 16 | 18 | 20 |
|---------------------|------------------|------------------|------------------|------------------|
| DIM | | | | |
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | AA | BB | AC | AD |

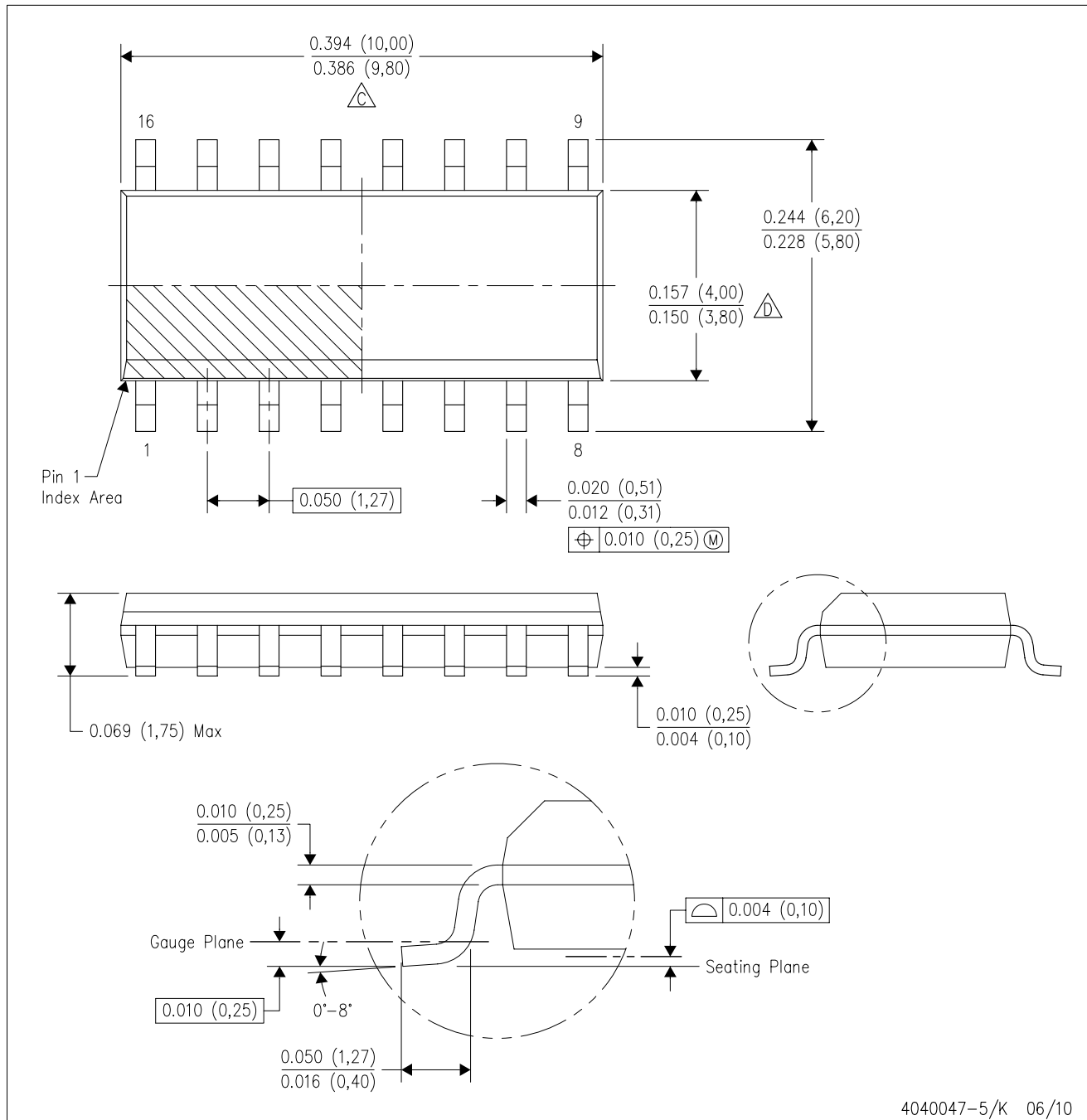


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- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

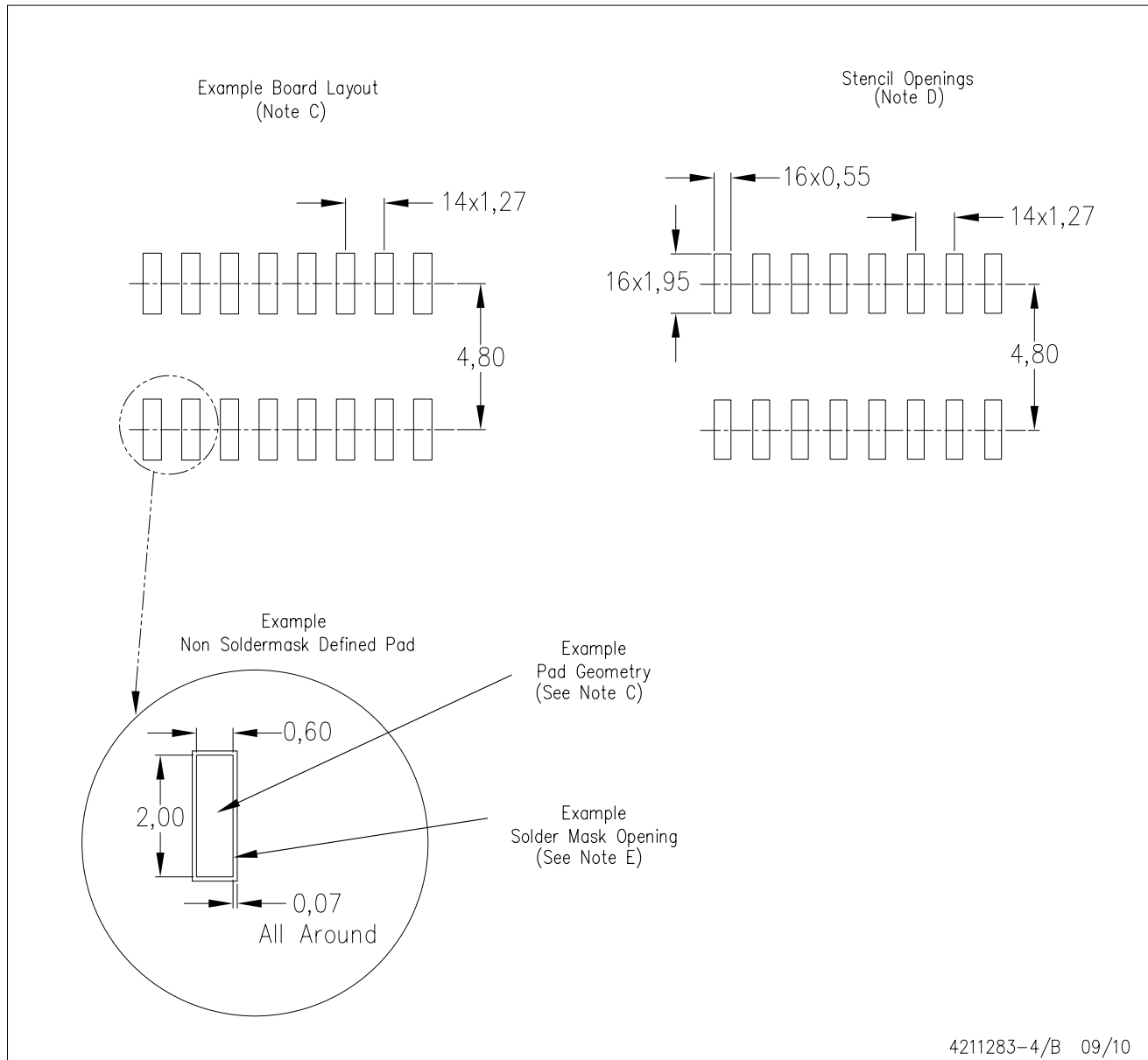
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



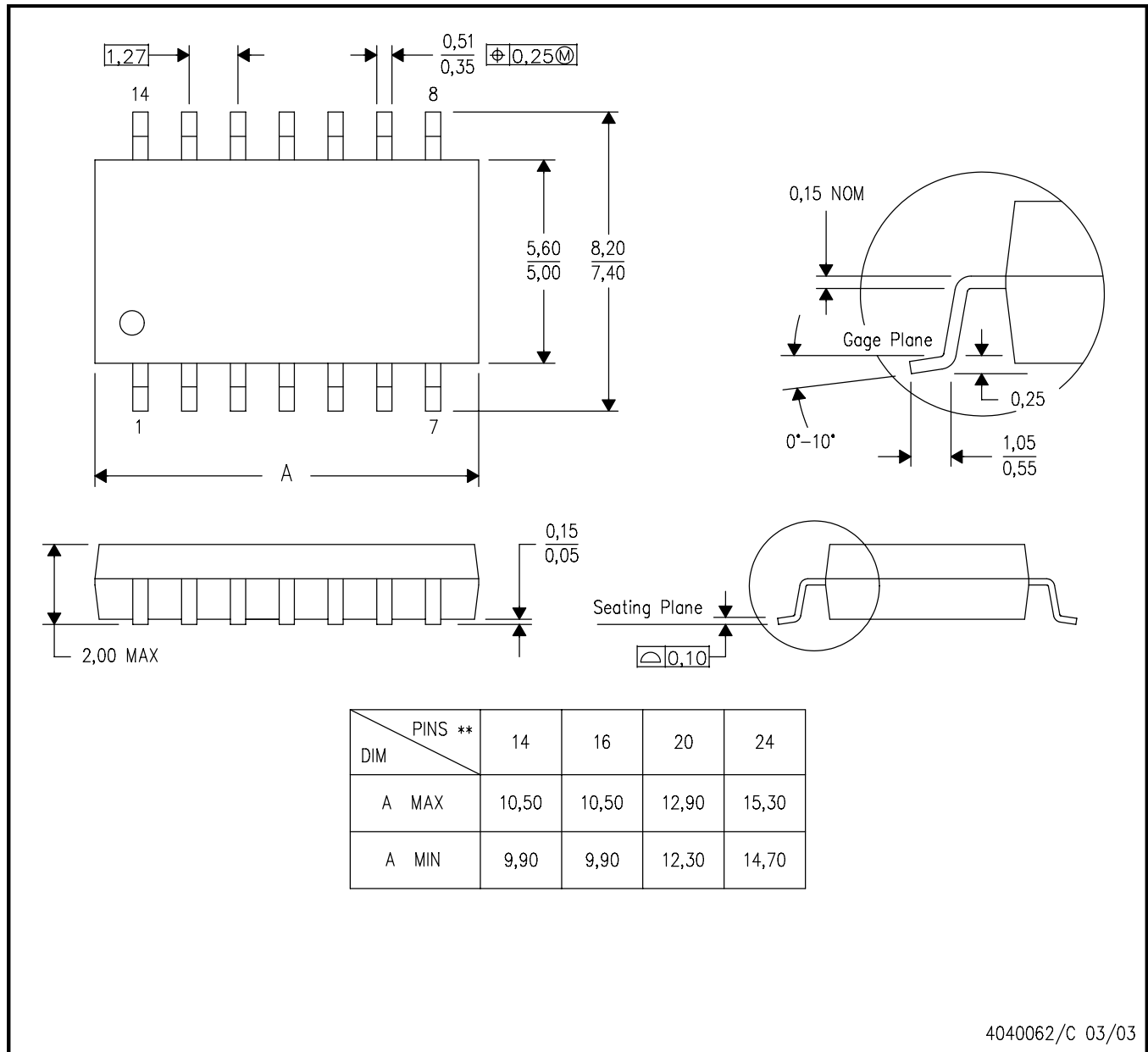
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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