Product Preview

1:10 LVCMOS Fanout Buffer

MPC9120

1:10 LVCMOS FANOUT BUFFER

The MPC9120 is a 1:10 LVCMOS fanout buffer targeted to support Intel based Pentium II™ microprocessor chip sets. The device features 10 low skew outputs optimized to drive the clock inputs of standard unbuffered SO–DIMM SDRAM modules. Standard unbuffered SO–DIMM SDRAM modules require two clocks per module allowing for the device to drive up to four modules. The output buffers have been optimized to drive the load presented by the SDRAM module.

The MPC9120 provides output shut off capabilities via an I^2C serial port for applications which plan to use fewer than four modules and desire to minimize the power dissipation of the chip. Every output clock can be individually enabled/disabled through fields in the I^2C control registers. After power up the default state is all outputs enabled. In applications where this default state is acceptable the I^2C ports need not be exercised.

- Supports Intel Pentium™ and Pentium II Processor Architectures
- 10 Skew Controlled 3.3V Compatible SDRAM Clocks
- I^2C Serial Bus Interface
- Extensive Output Enable Control Capability
- Space Efficient 28–Lead SSOP Package
- Operating Temperature Range of 0°C to 70°C
- 3.3V ± 5% Power Supply

SD SUFFIX
28–LEAD PLASTIC SSOP PACKAGE
CASE 940E–02

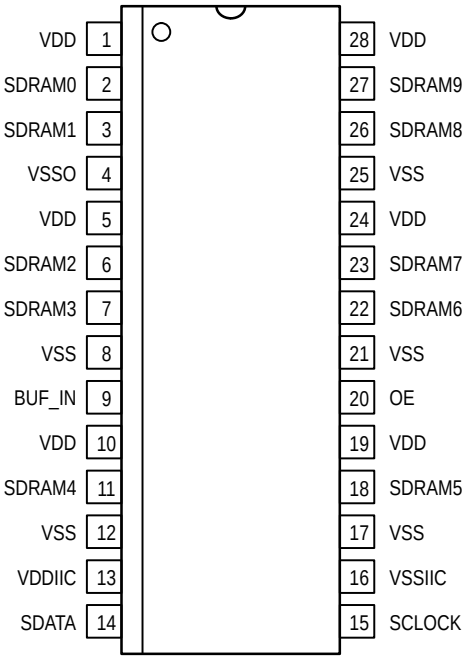

Figure 1. 28–Lead Pinout (Top View)

FUNCTION TABLE

OE	V1, V2
0	High–Z
1	1x BUF_IN

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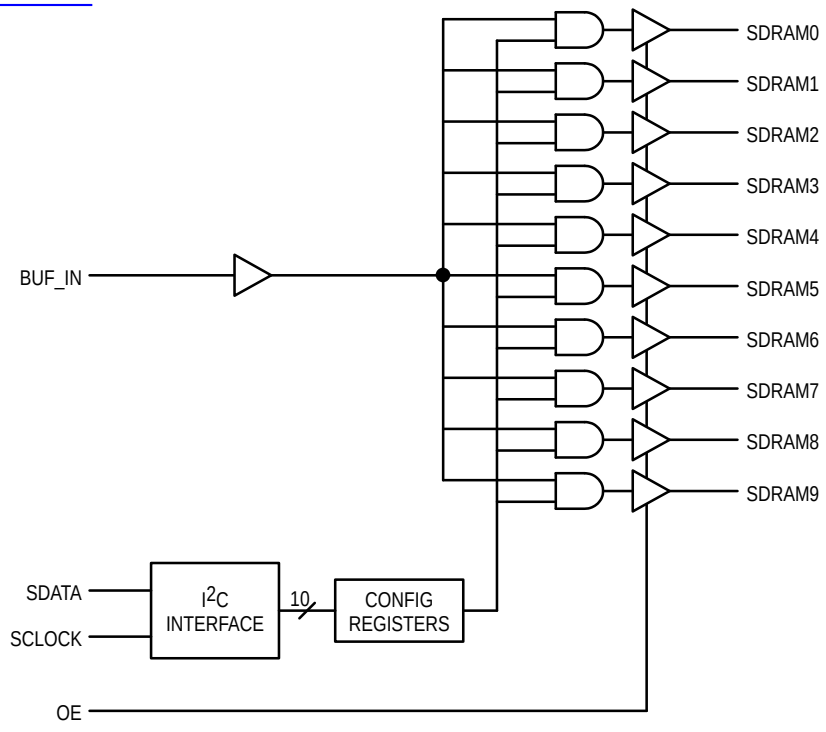


Figure 2. Block Diagram

Table 1. Pin Descriptions

Pin Name	I/O	Function
BUF_IN	I	3.3V CMOS clock input
SDRAM0:9	O	3.3V CMOS SDRAM clock outputs
SDATA	I/O	Serial data for configuration control
SCLK	I	Serial clock input for configuration control. The state of the SDATA input is clocked into the device on the rising edge of this clock
OE	I	A Low forces all outputs into High–Z state
VDD	–	3.3V power supply connection
VSS	–	Ground connection which should be connected directly to the ground plane

I2C Interface

The device has an I2C serial bus interface consisting of a serial clock input (SCLK) and a data line (SDATA) . The clock driver acts as a slave receiver on the I2C bus with a standard data transfer rate of up to 100 kbit/s. The MPC9120 is a 'write only' device which will not respond to general call requests from the bus master. The I2C interface transfers data in byte length packets except for the start, stop and acknowledge bits. The clock driver supports block writes consisting of the following elements.

1) Start Bit
2) Address
3) Acknowledge Bit
4) Command Code
5) Acknowledge Bit
6) Byte Count
7) Acknowledge Bit
8) Data Fields (see Table 2)
9) Acknowledge Bit
10) Stop Bit

After each byte, the clock driver pulls down the data line to acknowledge the transfer. The clock driver holds SDATA low during the high state of SCLK. The 7–bit address of the clock driver is:

A7	A6	A5	A4	A3	A2	A1	R/W
1	1	0	1	0	0	1	0

Note: A7 is the first address bit

The 'Command Code' should be set to all '0's and the 'Byte Count' can range from 1 to 3. The data fields are transferred sequentially in ascending order starting with Byte 0 – Configuration Function.

The MPC9120 is compliant with the DC/AC characteristics of a "Standard–Mode" I2C bus device. The logic thresholds are dependent on the 3.3V supply. For additional information on the I2C bus, refer to the document, 3114 – "The I2C–bus and how to use it (including specifications)" available from Philips Semiconductors:

http://www.semiconductors.philips.com

Table 2. Serial Data Fields

Byte	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	SDRAM0:3	Not Used	Not Used	Not Used	Not Used	SDRAM3	SDRAM2	SDRAM1	SDRAM0
	Package Pin	N/A	N/A	N/A	N/A	7	6	3	2
1	SDRAM6:9	SDRAM9	SDRAM8	SDRAM7	SDRAM6	Not Used	Not Used	Not Used	Not Used
	Package Pin	27	26	23	22	N/A	N/A	N/A	N/A
2	SDRAM4:5	SDRAM5	SDRAM4	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
	Package Pin	18	11	N/A	N/A	N/A	N/A	N/A	N/A

1. Not Used bits fields are "Don't Care" conditions.
2. When a bit field is programmed with a "1" (enable), the clock is active. A "0" (disable) means the clock is inactive.

MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
VDD	3.3V Core Supply Voltage	–0.5	4.6	V
T_{stg}	Storage Temperature Range	–65	150	°C
V_{IH}	3.3V Input High Voltage (Note 3.)	–0.5	4.6	V
V_{IL}	3.3V Input Low Voltage	–0.5		V
ESD	ESD Input Protection	2000		V

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

3. V_{IH} should not exceed VDD level.

DC CHARACTERISTICS (VDD = 3.3V ±5%; GND = 0.0V; T_A = 0 to +70°C; Unless Otherwise Specified)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
I_{DD}	Supply Current for VDD	No Clock Mode Active 66MHz Active 100MHz			3 230 360	mA	BUF_IN = VSS or VDD
V_{IL}	Input Low Voltage		–0.3		0.8	V	
V_{IH}	Input High Voltage		2.0		VDD+0.3	V	
I_{IL}	Input Leakage Current		–5.0		5	µA	0 < V_{IN} < VCC/VCCI
V_{OL}	3.3V Output Low Voltage				0.40	V	I_{OL} = 1mA
V_{OH}	3.3V Output High Voltage		2.4			V	I_{OH} = –1.0mA
C_I	Input Capacitance			TBD		pF	Except XTL_In, XTL_Out
L_I	Input Inductance			TBD		nH	Except XTL_In, XTL_Out

AC CHARACTERISTICS (VDD = 3.3V ±5%; GND = 0.0V; T_A = 0 to +70°C; Unless Otherwise Specified)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
SDRAM Clock Outputs (SDRAM0:17)							
t_{sk}	Output Clock Skew				250	ps	Note 4.
d_t	Output Duty Cycle		45		55	%	Note 5.
t_p	Clock Period	66MHz 100MHz	15.0 10.0		15.5 10.5	ns	Note 4.
t_{VIH}	High Time	66MHz 100MHz	5.6 3.3			ns	Measured at 2.4V
t_{VIL}	Low Time	66MHz 100MHz	5.3 3.1			ns	Measured at 0.4V
t_{rise}	Rise Time		1.5		4.0	V/ns	From 0.4V to 2.4V
t_{fall}	Fall Time		1.5		4.0	V/ns	From 2.4V to 0.4V
t_{PLH}	Low to High Propagation Delay		1.0		5.0	ns	
t_{PHL}	High to Low Propagation Delay		1.0		5.0	ns	
t_{PZL}, t_{PZH}	Enable Delay		1.0		8.0	ns	
t_{PLZ}, t_{PHZ}	Disable Delay		1.0		8.0	ns	

4. Measured on the rising edge of the clock at 1.5V.
5. Input slew rate >1V/ns.

APPLICATIONS INFORMATION

Output Series Termination

With typical MPC9120 edge rates of 1.5V/ns, a PCB trace becomes a transmission line when it is over 1–inch in length. This transmission line needs some sort of termination scheme to ensure good signal integrity at the load (device receiving clock signal). Most motherboards use the practice of *series termination*. In series termination, a series termination resistor (external resistor) is added in series with the driver device output, as shown in Figure 3, series termination resistor value is chosen so that its value, added to the output impedance of the driver, is equal to the PCB trace impedance, or in other words, $R_{TH} = R_S + Z_L$. The series termination resistor must be located close to the device output.

Typical system PCB trace impedance is 50–70Ω, which is low enough to produce sufficient signal rise and fall time at the load capacitance presented by a standard CMOS input. Figure 4 illustrates proper series termination of the 15Ω MPC9120 output driving a 60Ω transmission line.

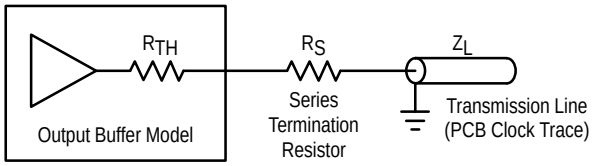


Figure 3. Clock Output Series Termination

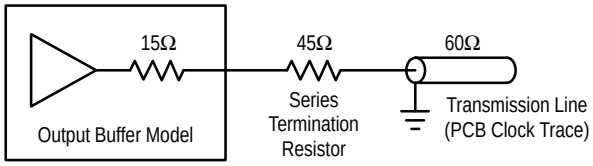


Figure 4. Clock Output Series Termination

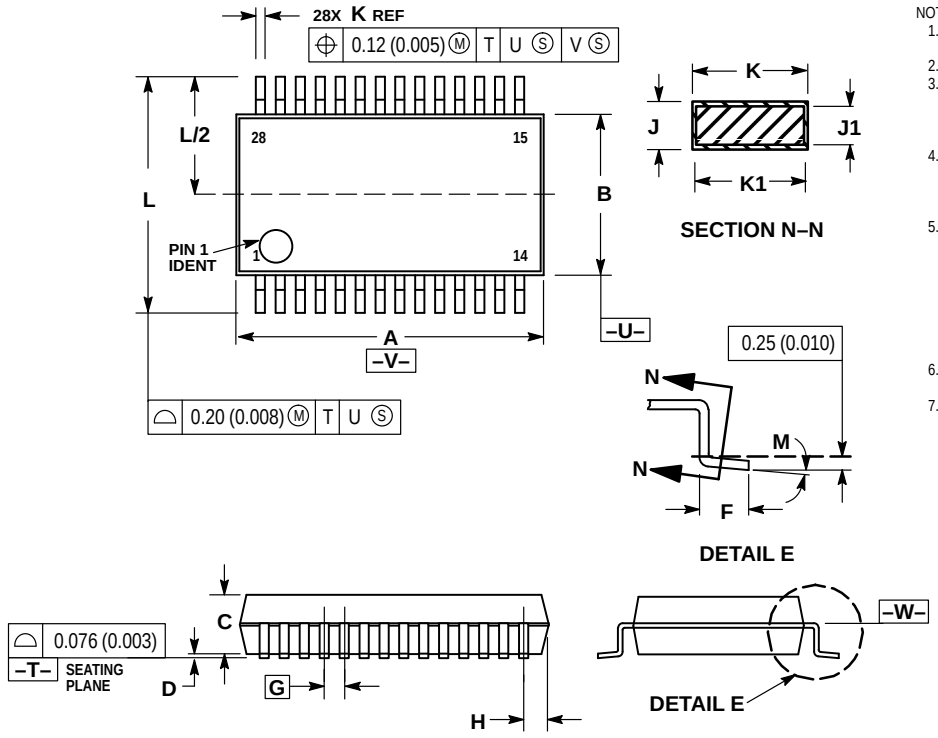
Pull–Up			
Voltage (V)	**I_{min}** (mA)	**I_{typ}** (mA)	**I_{max}** (mA)
0	–72	–116	–198
1.000	–72	–116	–198
1.400	–68	–110	–188
1.500	–67	–107	–184
1.650	–64	–103	–177
1.800	–60	–98	–170
2.000	–54	–90	–157
2.400	–39	–69	–126
2.600	–30	–56	–107
3.135	0	–15	–46
3.300	–	0	–23
3.465	–	–	0

Pull–Down			
Voltage (V)	**I_{min}** (mA)	**I_{typ}** (mA)	**I_{max}** (mA)
0	0	0	0
0.400	23	34	53
0.650	35	52	83
0.850	43	65	104
1.000	49	74	118
1.400	61	93	152
1.500	64	98	159
1.650	67	103	168
1.800	70	108	177
1.950	72	112	184
3.315	72	112	204
3.600	–	112	204

Figure 5. Typical Output V/I Characteristics for MPC9120

OUTLINE DIMENSIONS

SD SUFFIX
PLASTIC SSOP PACKAGE
CASE 940E–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.07	10.33	0.396	0.406
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.47	0.63	0.018	0.024
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0 °	8 °	0 °	8 °

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