High-performance Clock Generator Series

Compact 1ch Clock Generators for Digital Cameras

BU3071HFV, BU3072HFV, BU3073HFV, BU3076HFV BU7322HFV, BU7325HFV

Pb Free ROHM Electronic Components   RoHS Directive Compliance

●Description

These Clock Generators incorporates compact package compared to oscillators, which provides the generation of high-frequency CCD, USB, VIDEO clocks necessary for digital still cameras and digital video cameras.

●Features

1) SEL pin allowing for the selection of frequencies
2) Selection of OE pin enabling Power-down function
3) Crystal-oscillator-level clock precision with high C/N characteristics and low jitter
4) Microminiature HVSOF6 Package incorporated
5) Single power supply of 3.3 V

●Applications

Digital Still Camera, Digital Video Camera, and others

●Lineup

	BU3071HFV	BU3072HFV	BU3073HFV	BU3076HFV	BU7322HFV	BU7325HFV
Supply voltage	3.0 V～3.6V	3.0 V～3.6V	3.0 V～3.6V	2.85 V～3.6V	2.85 V～3.6V	2.85 V～3.6V
Operating temperature range	-5℃～70℃	-5℃～70℃	-5℃～70℃	-5℃～75℃	-5℃～75℃	-30℃～85℃
Reference input clock	28.6363MHz	48.0000MHz	48.0000MHz	27.0000MHz	27.0000MHz	27.0000MHz
Output clock	54.0000MHz	27.0000MHz	24.3750MHz	54.0000MHz	49.5000MHz	48.0000MHz
	-	36.0000MHz	24.5454MHz	67.5000MHz	36.0000MHz	78.0000MHz
Power-down function	Provided	Provided	Provided	Provided	Provided	Provided
Operating current (TYP)	10mA	11mA	11mA	12mA	10mA	12mA
Package	HVSOF6	HVSOF6	HVSOF6	HVSOF6	HVSOF6	HVSOF6

●Absolute Maximum Ratings（Ta=25℃）

	Symbol	Limit	Unit
Supply voltage	VDD	-0.3～4.0	V
Input voltage	VIN	-0.3～VDD+0.3	V
Storage temperature range	Tstg	-30～125	℃
Power dissipation	Pd	410	mW

*1 Operating is not guaranteed.
*2 In the case of exceeding Ta = 25℃, 4.1mW should be reduced per 1℃.
*3 The radiation-resistance design is not carried out.
*4 Power dissipation is measured when the IC is mounted to the printed circuit board.

Sep. 2008

●Recommended Operating Range

Parameter	Symbol	Limit	Unit
Supply voltage	VDD	3.0～3.6	V
Input H voltage	VINH	0.8VDD～VDD	V
Input L voltage	VINL	0.0～0.2VDD	V
Operating temperature	Topr	-5～70	℃
Output load	CL	15(MAX)	pF

●Electrical characteristics

BU3071HFV（Ta=25℃, VDD=3.3V,Crystal frequency=28.6363MHz, unless otherwise specified.）

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output H voltage	VOH	2.8	-	-	V	IOH=-4.0mA
Output L voltage	VOL	-	-	0.5	V	IOL=4.0mA
Consumption current 1	IDD1	-	10	15	mA	OE=H, at no load
Consumption current 2	IDD2	-	1	1.3	mA	OE=L
Output frequency		-	54.0000	-	MHz	IN*264/35/4
The following parameters represent design guaranteed performance.						
Duty	Duty	45	50	55	%	Measured at a voltage of 1/2 of VDD
Period-Jitter 1 σ	PJsSD	-	50	-	psec	※1
Period-Jitter MIN-MAX	PJsABS	-	300	-	psec	※2
Rise time	tr	-	2.5	-	nsec	Period of transition time required for the output to reach 80% from 20% of VDD. Provided with 15pF output load.
Fall time	tf	-	2.5	-	nsec	Period of transition time required for the output to reach 20% from 80% of VDD. Provided with 15pF output load.
Output Lock time	tLOCK	-	-	1	msec	※3

Note) The output frequency is determined by the arithmetic (frequency division) expression of a frequency input to IN.If the input frequency is set to 28.6363MHz, the output frequency will be as listed above.

BU3072HFV（Ta=25℃, VDD=3.3V, Crystal frequency=48.0000MHz, unless otherwise specified.）

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output H voltage	VOH	2.8	-	-	V	IOH=-4.0mA
Output L voltage	VOL	-	-	0.5	V	IOL=4.0mA
Consumption current 1	IDD1	-	11	16	mA	PD=H, at no load
Consumption current 2	IDD2	-	-	5	μA	PD=L
Output frequency	CLK_27	-	27.0000	-	MHz	SEL=L, IN*18/8/4
	CLK_36	-	36.0000	-	MHz	SEL=H, IN*24/8/4
The following parameters represent design guaranteed performance.						
Duty	Duty	45	50	55	%	Measured at a voltage of 1/2 of VDD
Period-Jitter 1 σ	PJsSD	-	35	-	psec	※1
Long-Term-Jitter MIN-MAX	LTJsABS	-	0.9	1.5	nsec	MIN-MAX of long-term jitter (100 μsec from trigger)
Rise time	tr	-	2.5	-	nsec	Period of transition time required for the output to reach 80% from 20% of VDD. Provided with 15pF output load.
Fall time	tf	-	2.5	-	nsec	Period of transition time required for the output to reach 20% from 80% of VDD. Provided with 15pF output load.
Output Lock time	tLOCK	-	-	1	msec	※3

Note) The output frequency is determined by the arithmetic (frequency division) expression of a frequency input to IN.If the input frequency is set to 48.0000MHz, the output frequency will be as listed above.

BU3073HFV（Ta=25℃, VDD=3.3V, Crystal frequency=48.0000MHz, unless otherwise specified.）

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output H voltage	VOH	2.8	-	-	V	IOH=-4.0mA
Output L voltage	VOL	-	-	0.5	V	IOL=4.0mA
Consumption current 1	IDD1	-	11	16	mA	PD=H, at no load
Consumption current 2	IDD2	-	-	5	mA	PD=L
Output frequency	CLK_375	-	24.3750	-	MHz	SEL=L, IN*65/16/8
	CLK_545	-	24.5454	-	MHz	SEL=H, IN*45/11/8
The following parameters represent design guaranteed performance.						
Duty	Duty	45	50	55	%	Measured at a voltage of 1/2 of VDD
Period-Jitter 1σ	PJsSD	-	45	-	psec	※1
Long-Term-Jitter MIN-MAX	LTJsABS	-	0.9	1.5	nsec	MIN-MAX of long-term jitter (100 μsec from trigger)
Rise time	tr	-	2.5	-	nsec	Period of transition time required for the output to reach 80% from 20% of VDD. Provided with 15pF output load.
Fall time	tf	-	2.5	-	nsec	Period of transition time required for the output to reach 20% from 80% of VDD. Provided with 15pF output load.
Output Lock time	tLOCK	-	-	1	msec	※3

Note) The output frequency is determined by the arithmetic (frequency division) expression of a frequency input to IN.
If the input frequency is set to 48.0000MHz, the output frequency will be as listed above.

BU3076HFV（Ta=25℃, VDD=3.3V, Crystal frequency=27.0000MHz, unless otherwise specified.）

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output H voltage	VOH	2.8	-	-	V	IOH=-4.0mA
Output L voltage	VOL	-	-	0.5	V	IOL=4.0mA
Pull-down resistance	Rpd	25	50	100	KΩ	Pull-down resistance on input pin
Consumption current 1	IDD1	-	10	15	mA	54MHz output, at no load
Consumption current 2	IDD2	-	12	18	mA	67.5MHz output, at no load
Standby current	IDDst	-	-	1	μA	OE=L
Output frequency	CLK_54	-	54.0000	-	MHz	SEL=L, IN*48/6/4
	CLK_67.5	-	67.5000	-	MHz	SEL=H, IN*60/6/4
The following parameters represent design guaranteed performance.						
Duty	Duty	45	50	55	%	Measured at a voltage of 1/2 of VDD
Period-Jitter 1σ	PJsSD	-	50	-	psec	※1
Period-Jitter MIN-MAX	PJsABS	-	300	-	psec	※2
Rise time	tr	-	1.5	-	nsec	Period of transition time required for the output to reach 80% from 20% of VDD. Provided with 15pF output load.
Fall time	tf	-	1.5	-	nsec	Period of transition time required for the output to reach 20% from 80% of VDD. Provided with 15pF output load.
Output Lock time	tLOCK	-	-	200	usec	※3

Note) The output frequency is determined by the arithmetic (frequency division) expression of a frequency input to IN.
If the input frequency is set to 27.0000MHz, the output frequency will be as listed above.

BU7322HFV（Ta=25℃, VDD=3.3V, Crystal frequency=27.0000MHz, unless otherwise specified.）

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output H voltage	VOH	2.8	-	-	V	IOH=-4.0mA
Output L voltage	VOL	-	-	0.5	V	IOL=4.0mA
Pull-down resistance	Rpd	25	50	100	kΩ	Pull-down resistance on input pin
Consumption current 1	IDD	-	10	13.5	mA	49.5MHz output, at no load
Consumption current 2	IDD2	-	9.5	13.0	mA	36.0MHz output, at no load
Standby current	IDDst	-	-	1	μA	OE=L
Output frequency	CLK_49.5	-	49.5000	-	MHz	SEL=L, IN*66/6/6
	CLK_36	-	36.0000	-	MHz	SEL=H, IN*64/6/8
The following parameters represent design guaranteed performance.						
Duty	Duty	45	50	55	%	Measured at a voltage of 1/2 of VDD
Period-Jitter 1σ	PJsSD	-	50	-	psec	※1
Period-Jitter MIN-MAX	PJsABS	-	300	-	psec	※2
Rise time	tr	-	2.5	-	nsec	Period of transition time required for the output to reach 80% from 20% of VDD. Provided with 15pF output load.
Fall time	tf	-	2.5	-	nsec	Period of transition time required for the output to reach 20% from 80% of VDD. Provided with 15pF output load.
Output Lock time	tLOCK	-	-	200	usec	※3

Note) The output frequency is determined by the arithmetic (frequency division) expression of a frequency input to IN.
If the input frequency is set to 27.0000MHz, the output frequency will be as listed above.

BU7325HFV（Ta=25℃, VDD=3.3V, Crystal frequency=27.0000MHz, unless otherwise specified.）

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output H voltage	VOH	2.8	-	-	V	IOH=-4.0mA
Output L voltage	VOL	-	-	0.5	V	IOL=4.0mA
Pull-down resistance	Rpd	25	50	100	kΩ	Pull-down resistance on input pin
Consumption current 1	IDD1	-	11	15	mA	OE=H, SEL=L, at no load
Consumption current 2	IDD2	-	12	16.5	mA	OE=H, SEL=H, at no load
Standby current	IDDst	-	-	1	μA	OE=L
Output frequency	CLK_48	-	48.0000	-	MHz	SEL=L, IN*96/9/6
	CLK_78	-	78.0000	-	MHz	SEL=H, IN*104/9/4
The following parameters represent design guaranteed performance.						
Duty	Duty	45	50	55	%	Measured at a voltage of 1/2 of VDD
Period-Jitter 1σ	PJsSD	-	50	-	psec	※1
Period-Jitter MIN-MAX	PJsABS	-	300	-	psec	※2
Rise time	tr	-	1.5	-	nsec	Period of transition time required for the output to reach 80% from 20% of VDD. Provided with 15pF output load.
Fall time	tf	-	1.5	-	nsec	Period of transition time required for the output to reach 20% from 80% of VDD. Provided with 15pF output load.
Output Lock time	tLOCK	-	-	200	usec	※3

Note) The output frequency is determined by the arithmetic (frequency division) expression of a frequency input to IN.
If the input frequency is set to 27.0000MHz, the output frequency will be as listed above.

Common to BU3071HFV, BU3072HFV, BU3073HFV, BU3076HFV, BU7322HFV, BU7325HFV

∗1 Period-Jitter 1σ

This parameter represents standard deviation (=1σ) on cycle distribution data at the time when the output clock cycles are sampled 1000 times consecutively with the TDS7104 Digital Phosphor Oscilloscope of Tektronix Japan, Ltd.

∗2 Period-Jitter MIN-MAX

This parameter represents a maximum distribution width on cycle distribution data at the time when the output clock cycles are sampled 1000 times consecutively with the TDS7104 Digital Phosphor Oscilloscope of Tektronix Japan, Ltd.

∗3 Output Lock Time

This parameter represents elapsed time after power supply turns ON to reach a voltage of 3.0 V, after the system is switched from Power-Down state to normal operation state, or after the output frequency is switched, until it is stabilized at a specified frequency, respectively.

●Reference data (BU3071HFV basic data)

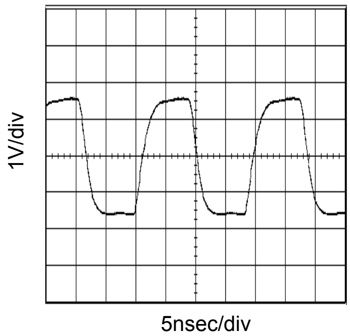


Fig.1 54MHz output waveform
(VDD=3.3V,CL=15pF,Ta=25℃)

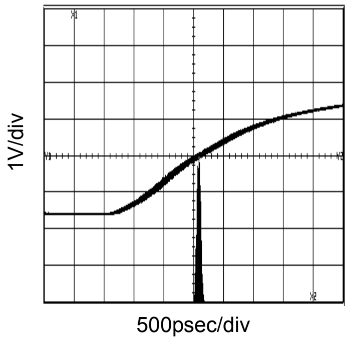


Fig.2 54MHz Period-Jitter
(VDD=3.3V,CL=15pF,Ta=25℃)

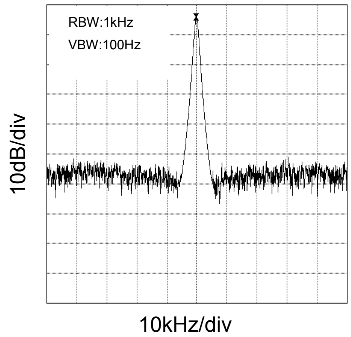


Fig.3 54MHz spectrum
(VDD=3.3V,CL=15pF,Ta=25℃)

●Reference data (BU3072HFV basic data)

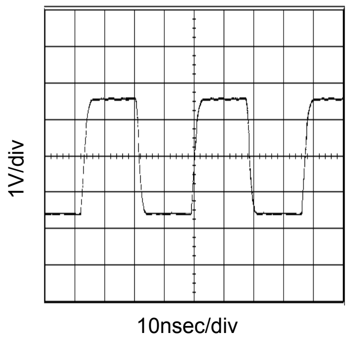


Fig.4 27MHz output waveform
(VDD=3.3V,CL=15pF,Ta=25℃)

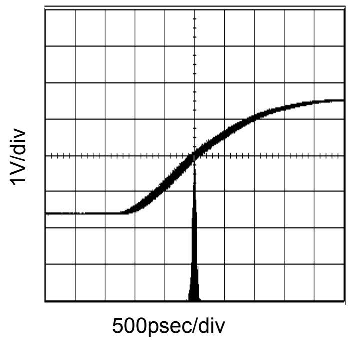


Fig.5 27MHz Period-Jitter
(VDD=3.3V,CL=15pF,Ta=25℃)

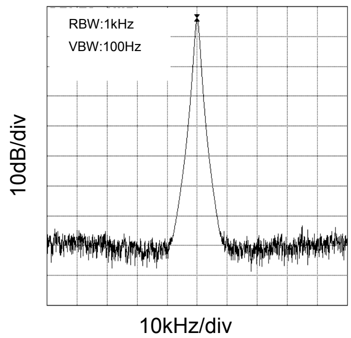


Fig.6 27MHz spectrum
(VDD=3.3V,CL=15pF,Ta=25℃)

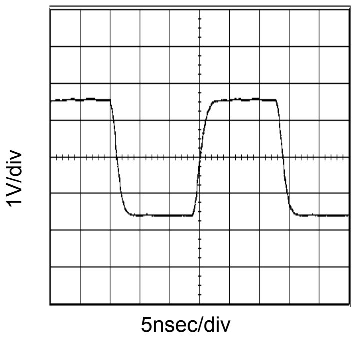


Fig.7 36MHz output waveform
(VDD=3.3V,CL=15pF,Ta=25℃)

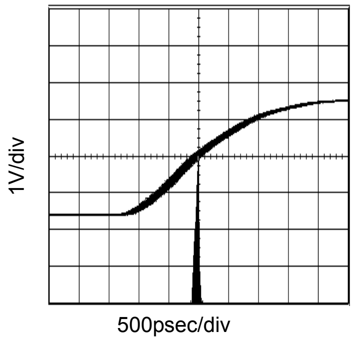


Fig.8 36MHz Period-Jitter
(VDD=3.3V,CL=15pF,Ta=25℃)

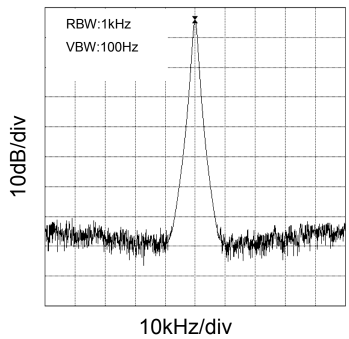
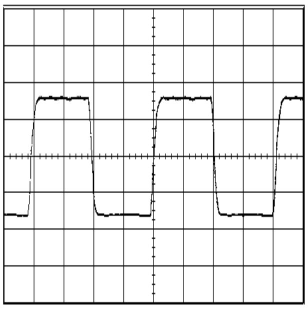


Fig.9 36MHz spectrum
(VDD=3.3V,CL=15pF,Ta=25℃)

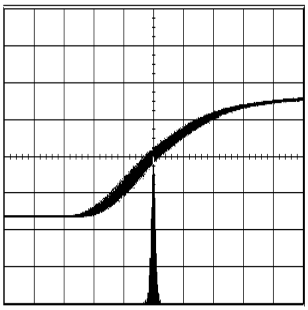
●Reference data (BU3073HFV basic data)



1V/div

10nsec/div

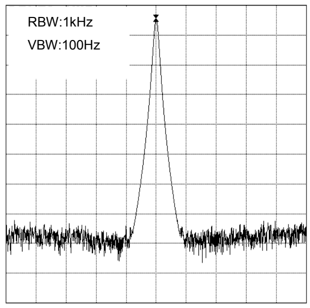
Fig.10 24.375MHz output waveform
(VDD=3.3V,CL=15pF,Ta=25℃)



1V/div

500psec/div

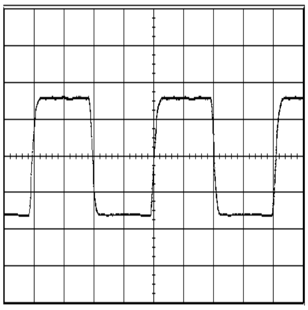
Fig.11 24.375MHz Period-Jitter
(VDD=3.3V,CL=15pF,Ta=25℃)



10dB/div

10kHz/div

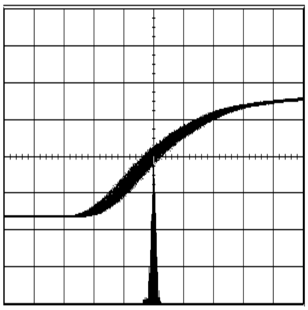
Fig.12 24.375MHz spectrum
(VDD=3.3V,CL=15pF,Ta=25℃)



1V/div

10nsec/div

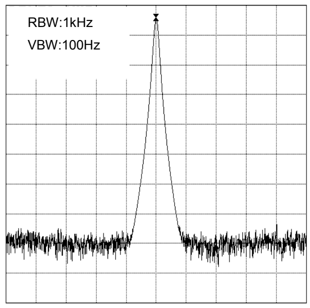
Fig.13 24.5454MHz output waveform
(VDD=3.3V,CL=15pF,Ta=25℃)



1V/div

500psec/div

Fig.14 24.5454MHz Period-Jitter
(VDD=3.3V,CL=15pF,Ta=25℃)

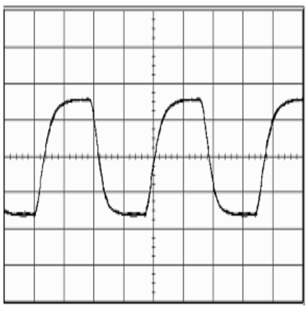


10dB/div

10kHz/div

Fig.15 24.5454MHz spectrum
(VDD=3.3V,CL=15pF,Ta=25℃)

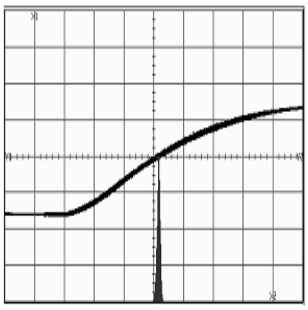
●Reference data (BU3076HFV basic data)



1V/div

5nsec/div

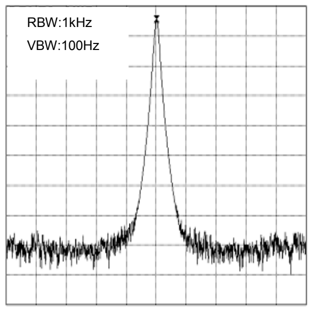
Fig.16 54MHz output waveform
(VDD=3.3V,CL=15pF,Ta=25℃)



1V/div

500psec/div

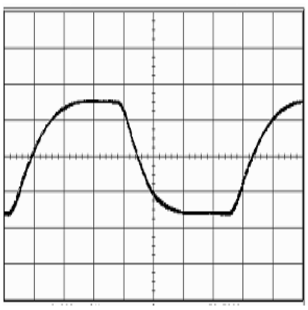
Fig.17 54MHz Period-Jitter
(VDD=3.3V,CL=15pF,Ta=25℃)



10dB/div

10kHz/div

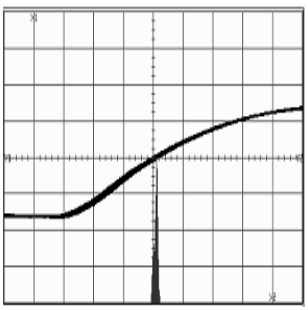
Fig.18 54MHz spectrum
(VDD=3.3V,CL=15pF,Ta=25℃)



1V/div

2nsec/div

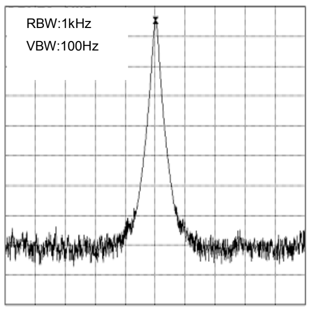
Fig.19 67.5MHz output waveform
(VDD=3.3V,CL=15pF,Ta=25℃)



1V/div

500psec/div

Fig.20 67.5MHz Period-Jitter
(VDD=3.3V,CL=15pF,Ta=25℃)



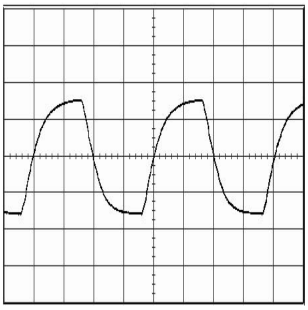
10dB/div

10kHz/div

Fig.21 67.5MHz spectrum
(VDD=3.3V,CL=15pF,Ta=25℃)

●Reference data (BU7322HFV basic data)

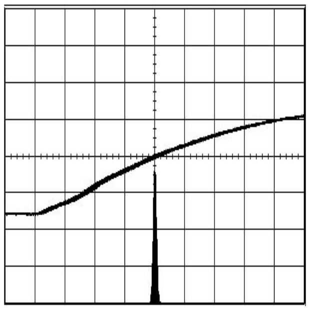
1V/div



5nsec/div

Fig.22 49.5MHz output waveform
(VDD=3.3V,CL=15pF,Ta=25℃)

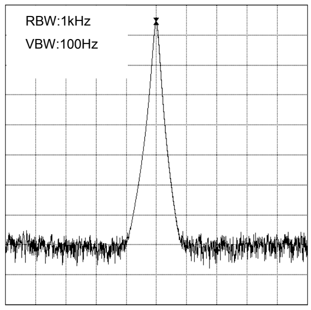
1V/div



500psec/div

Fig.23 49.5MHz Period-Jitter
(VDD=3.3V,CL=15pF,Ta=25℃)

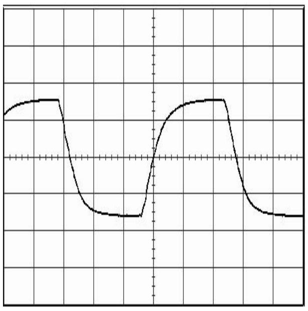
10dB/div



10kHz/div

Fig.24 49.5MHz spectrum
(VDD=3.3V,CL=15pF,Ta=25℃)

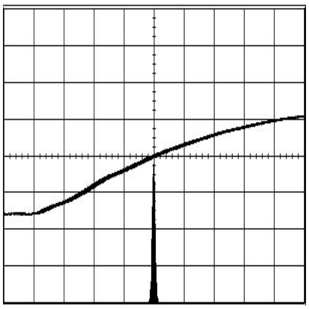
1V/div



10nsec/div

Fig.25 36MHz output waveform
(VDD=3.3V,CL=15pF,Ta=25℃)

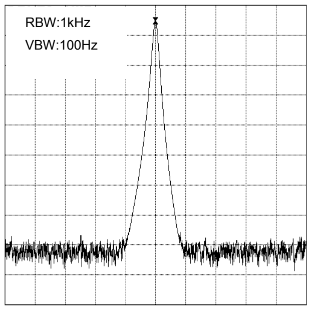
1V/div



500psec/div

Fig.26 36MHz Period-Jitter
(VDD=3.3V,CL=15pF,Ta=25℃)

10dB/div

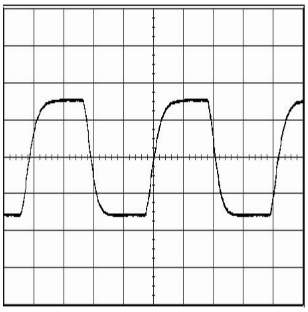


10kHz/div

Fig.27 36MHz spectrum
(VDD=3.3V,CL=15pF,Ta=25℃)

●Reference data (BU7325HFV basic data)

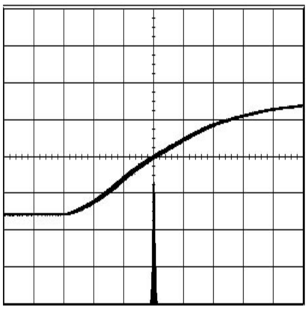
1V/div



5nsec/div

Fig.28 48MHz output waveform
(VDD=3.3V,CL=15pF,Ta=25℃)

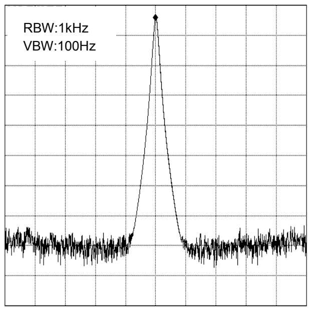
1V/div



500psec/div

Fig.29 48MHz Period-Jitter
(VDD=3.3V,CL=15pF,Ta=25℃)

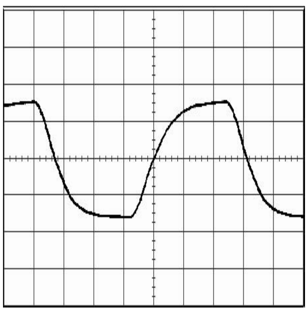
10dB/div



10kHz/div

Fig.30 48MHz spectrum
(VDD=3.3V,CL=15pF,Ta=25℃)

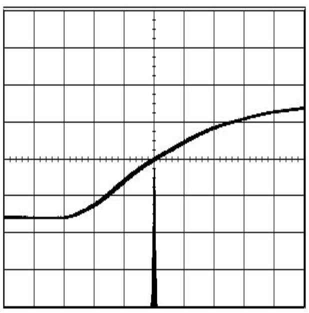
1V/div



10nsec/div

Fig.31 78MHz output waveform
(VDD=3.3V,CL=15pF,Ta=25℃)

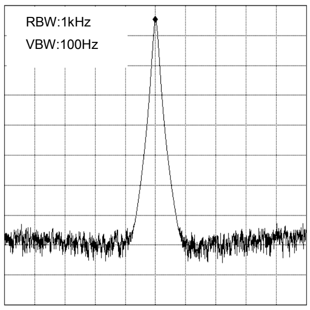
1V/div



500psec/div

Fig.32 78MHz Period-Jitter
(VDD=3.3V,CL=15pF,Ta=25℃)

10dB/div



10kHz/div

Fig.33 78MHz spectrum
(VDD=3.3V,CL=15pF,Ta=25℃)

●Reference data (BU3071HFV Temperature and Supply voltage variations data)

查询"BU3072HFV"供应商

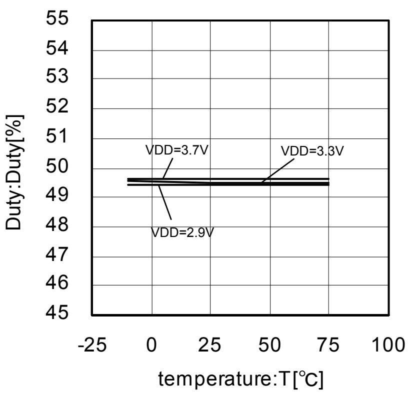


Fig.34 54MHz
Duty temperature characteristics

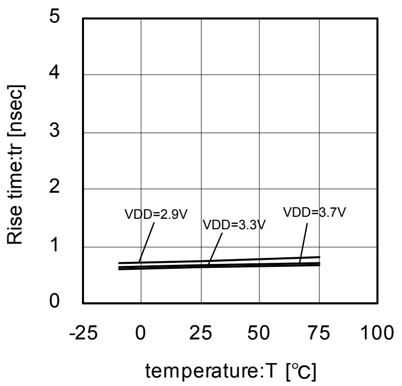


Fig.35 54MHz
Rise-time temperature characteristics

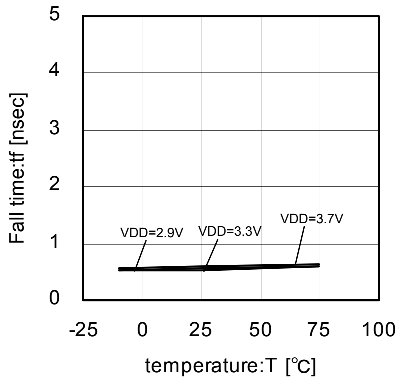


Fig.36 54MHz
Fall-time temperature characteristics

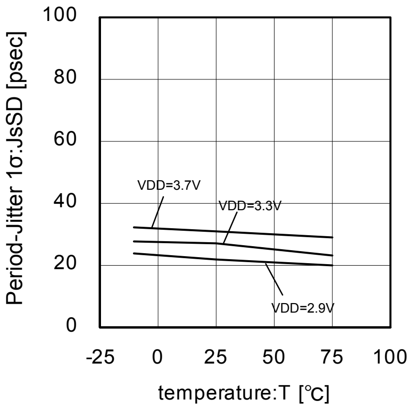


Fig.37 54MHz
Period-Jitter 1 σ temperature characteristics

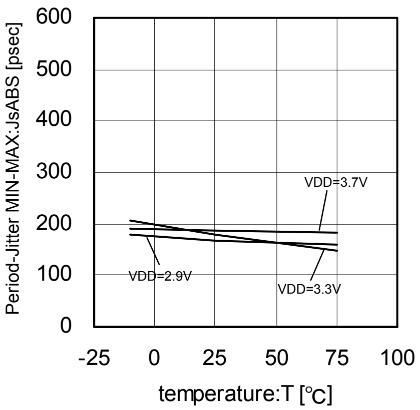


Fig.38 54MHz
Jitter-MinMax temperature characteristics

●Reference data (BU3072HFV Temperature and Supply voltage variations data)

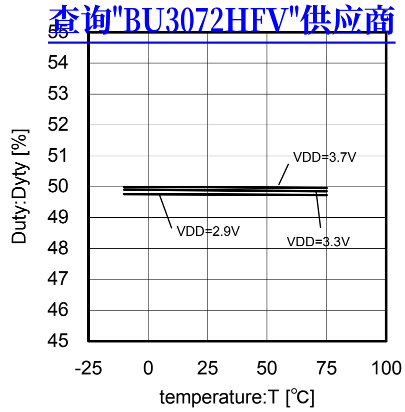


Fig.39 27MHz
Duty temperature characteristics

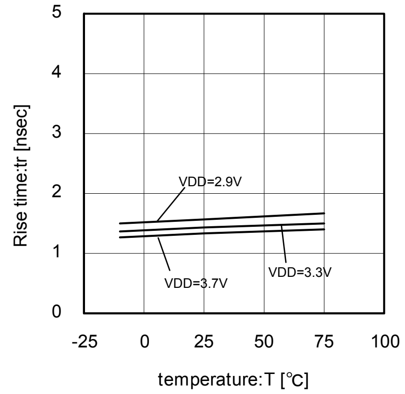


Fig.40 27MHz
Rise-time temperature characteristics

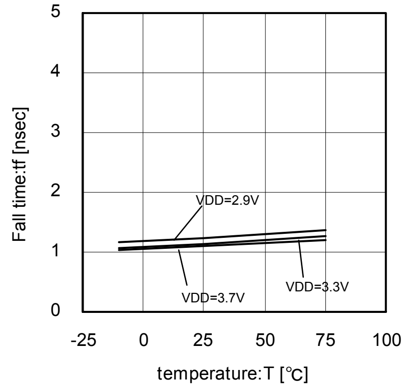


Fig.41 27MHz
Fall-time temperature characteristics

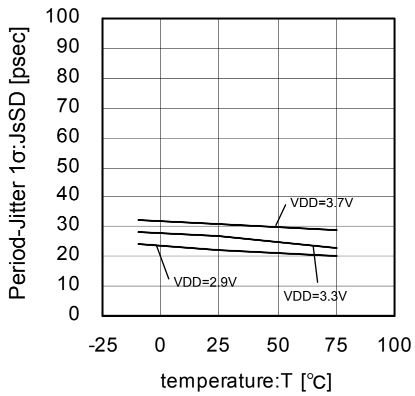


Fig.42 27MHz
Period-Jitter 1 σ temperature characteristics

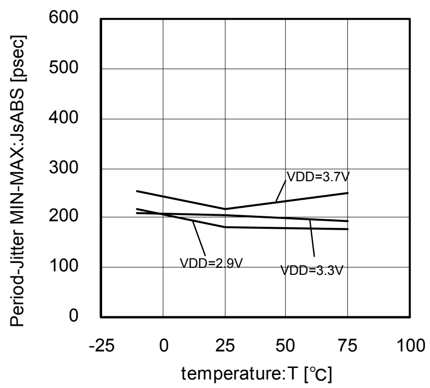


Fig.43 27MHz
Jitter-MinMax temperature characteristics

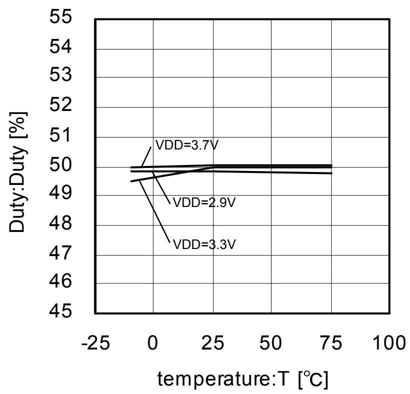


Fig.44 36MHz
Duty temperature characteristics

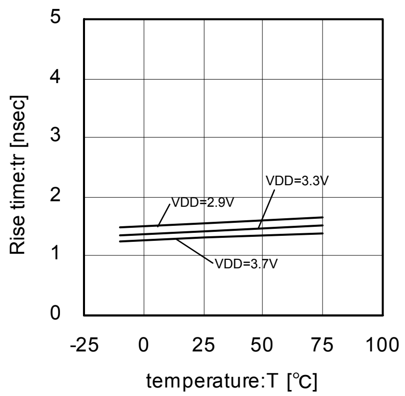


Fig.45 36MHz
Rise-time temperature characteristics

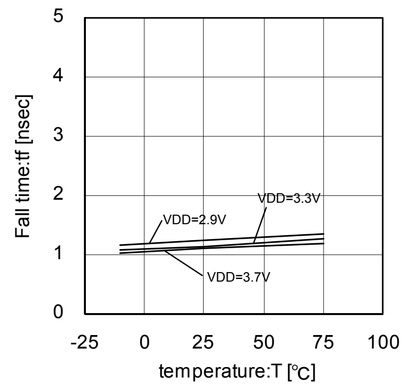


Fig.46 36MHz
Fall-time temperature characteristics

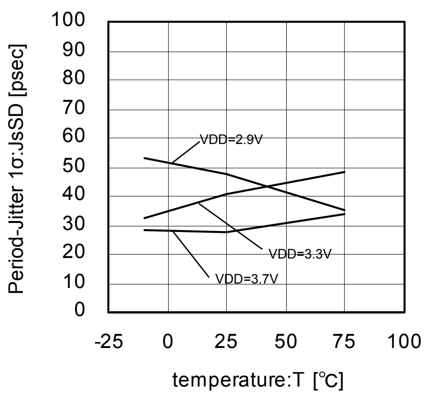


Fig.47 36MHz
Period-Jitter 1 σ temperature characteristics

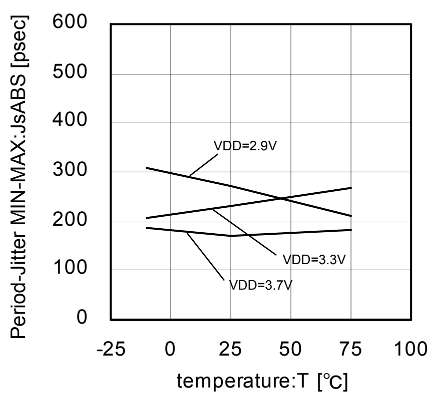


Fig.48 36MHz
Jitter-MinMax temperature characteristics

●Reference data (BU3073HFV Temperature and Supply voltage variations data)

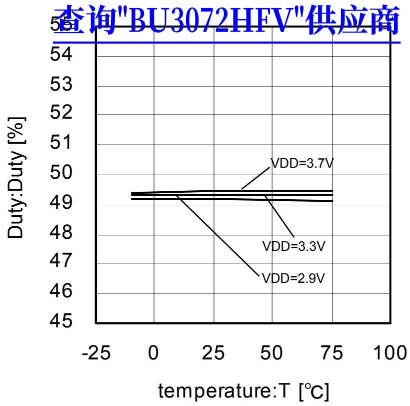


Fig.49 24.375MHz
Duty temperature characteristics

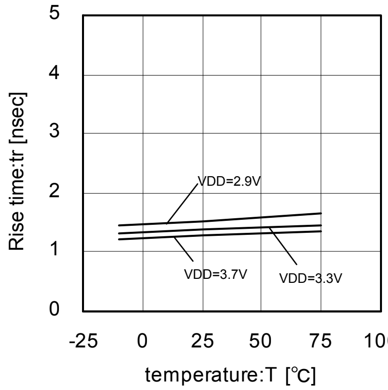


Fig.50 24.375MHz
Rise-time temperature characteristics

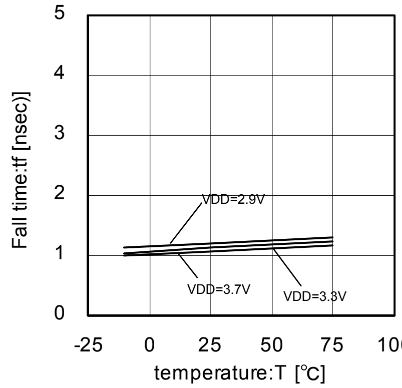


Fig.51 24.375MHz
Fall-time temperature characteristics

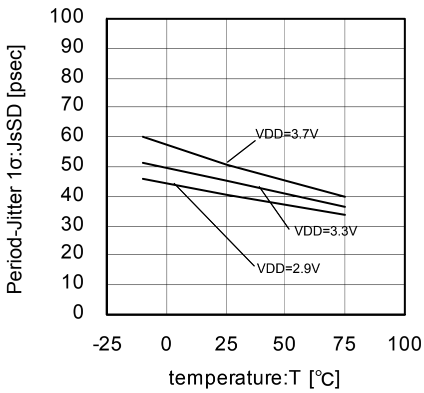


Fig.52 24.375MHz
Period-Jitter 1σ temperature characteristics

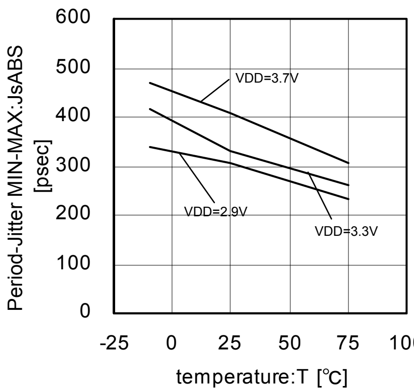


Fig.53 24.375MHz
Jitter-MinMax temperature characteristics

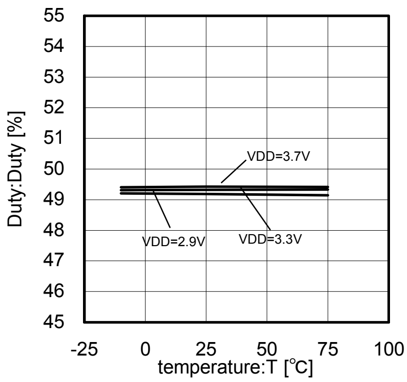


Fig.54 24.5454MHz
Duty temperature characteristics

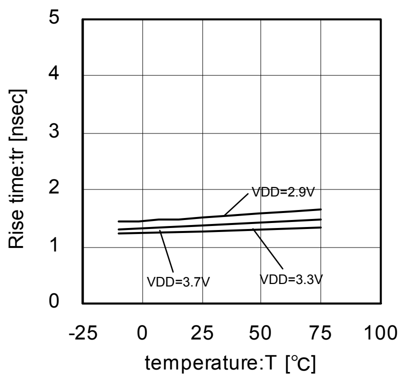


Fig.55 24.5454MHz
Rise-time temperature characteristics

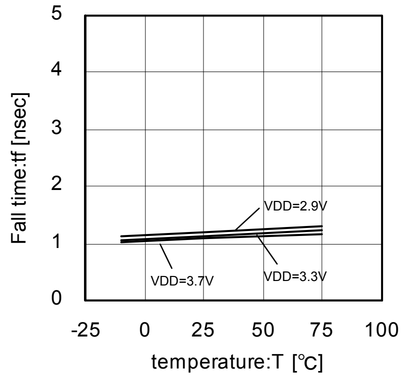


Fig.56 24.5454MHz
Fall-time temperature characteristics

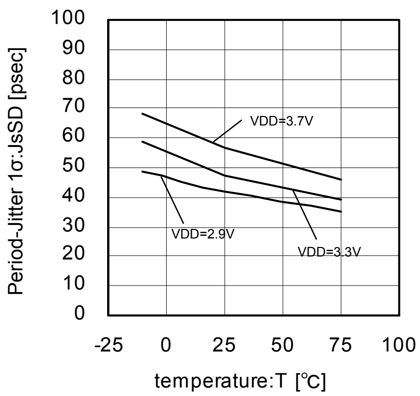


Fig.57 24.5454MHz
Period-Jitter 1σ temperature characteristics

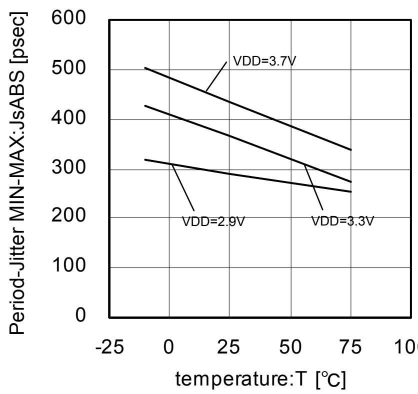


Fig.58 24.5454MHz
Jitter-MinMax temperature characteristics

●Reference data (BU3076HFV Temperature and Supply voltage variations data)

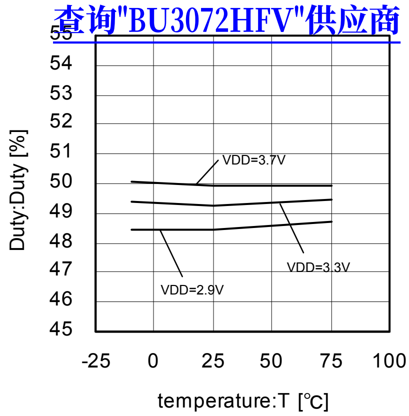


Fig.59 54MHz
Duty temperature characteristics

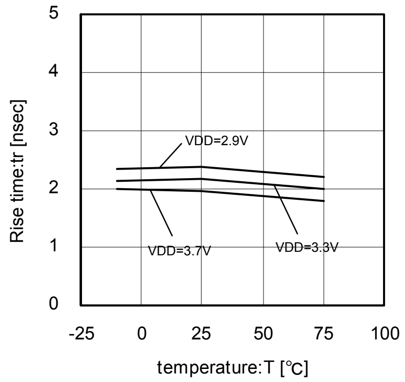


Fig.60 54MHz
Rise-time temperature characteristics

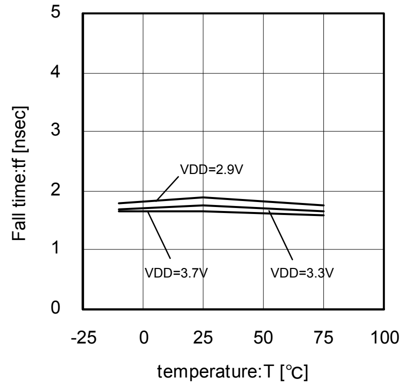


Fig.61 54MHz
Fall-time temperature characteristics

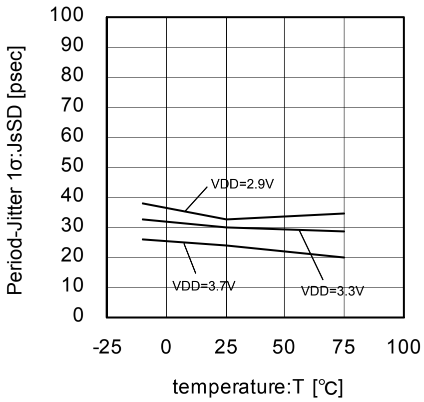


Fig.62 54MHz
Period-Jitter 1 σ temperature characteristics

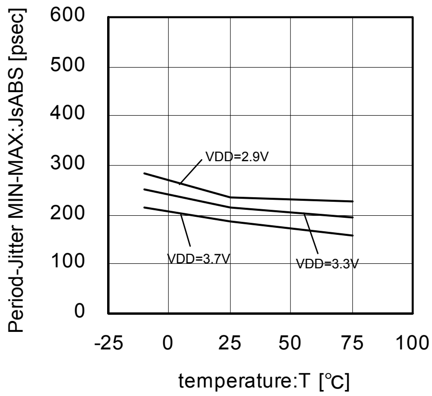


Fig.63 54MHz
Jitter-MinMax temperature characteristics

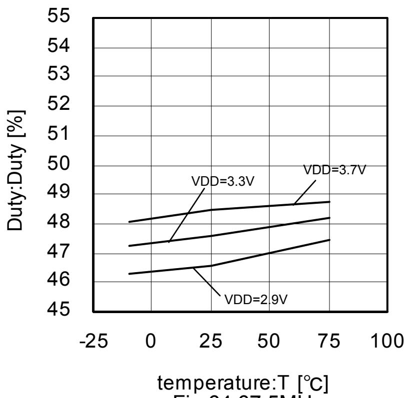


Fig.64 67.5MHz
Duty temperature characteristics

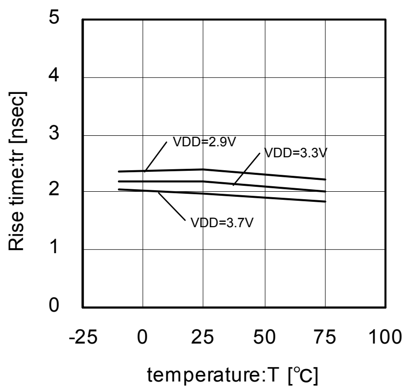


Fig.65 67.5MHz
Rise-time temperature characteristics

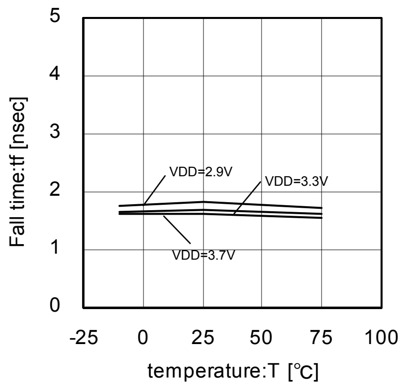


Fig.66 67.5MHz
Fall-time temperature characteristics

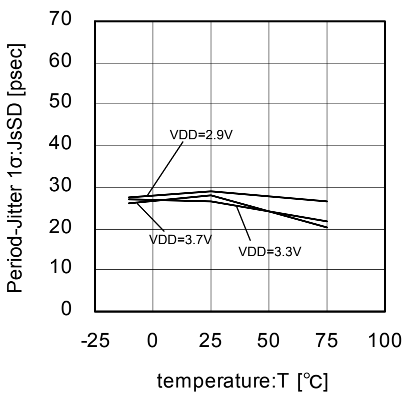


Fig.67 67.5MHz
Period-Jitter 1 σ temperature characteristics

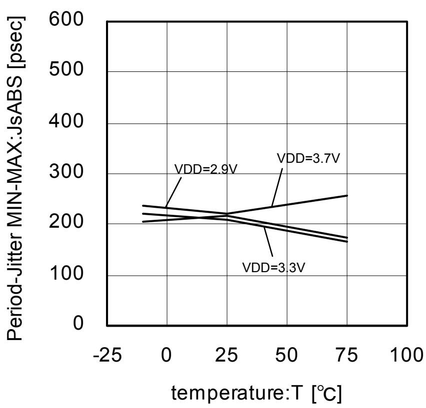


Fig.68 67.5MHz
Jitter-MinMax temperature characteristics

●Reference data (BU7322HFV Temperature and Supply voltage variations data)

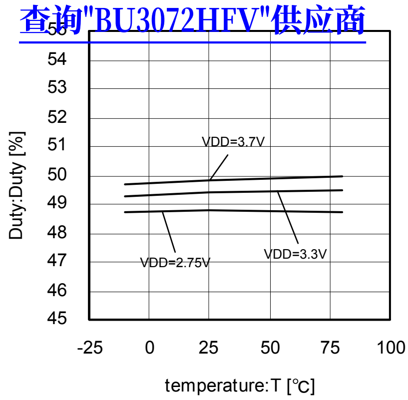


Fig.69 49.5MHz
Duty temperature characteristics

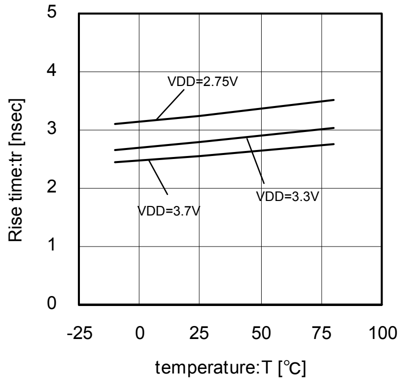


Fig.70 49.5MHz
Rise-time temperature characteristics

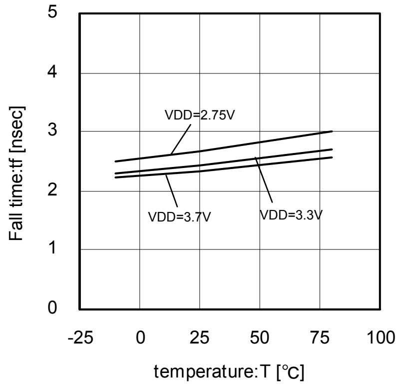


Fig.71 49.5MHz
Fall-time temperature characteristics

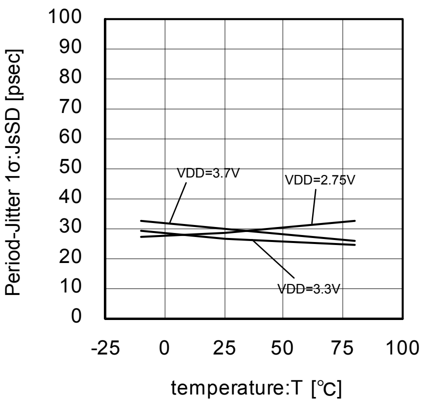


Fig.72 49.5MHz
Period-Jitter 1 σ temperature characteristics

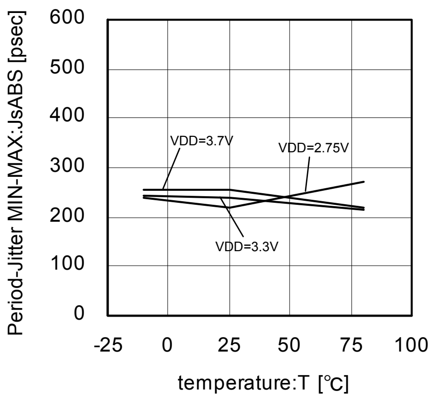


Fig.73 49.5MHz
Jitter-MinMax temperature characteristics

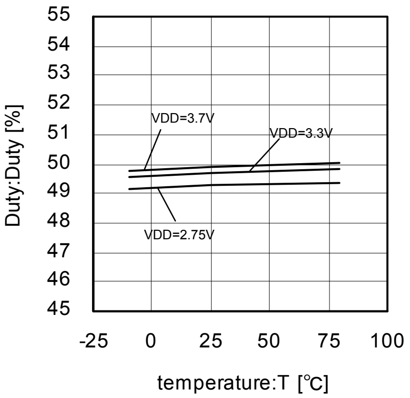


Fig.74 36MHz
Duty temperature characteristics

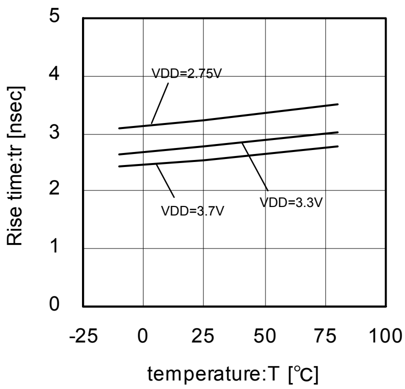


Fig.75 36MHz
Rise-time temperature characteristics

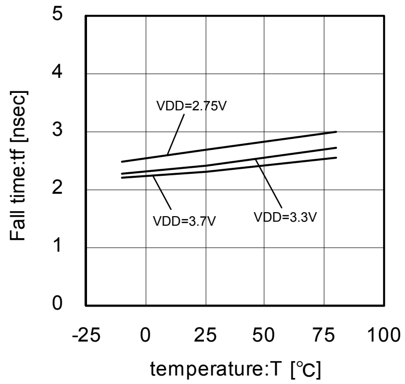


Fig.76 36MHz
Fall-time temperature characteristics

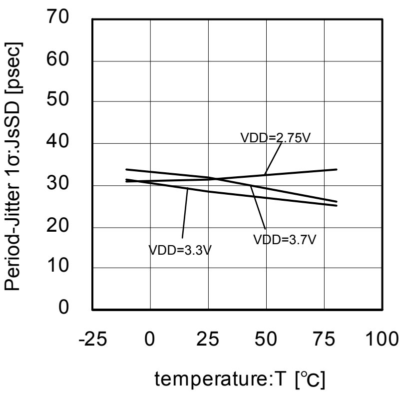


Fig.77 36MHz
Period-Jitter 1 σ temperature characteristics

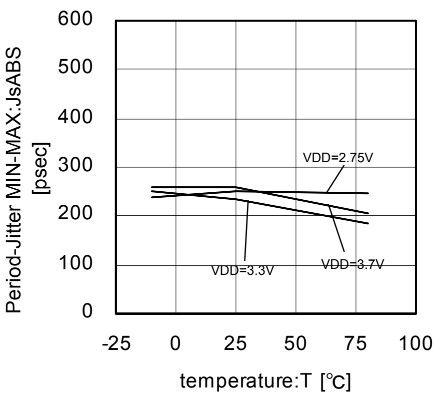


Fig.78 36MHz
Jitter-MinMax temperature characteristics

●Reference data (BU7325HFV Temperature and Supply voltage variations data)

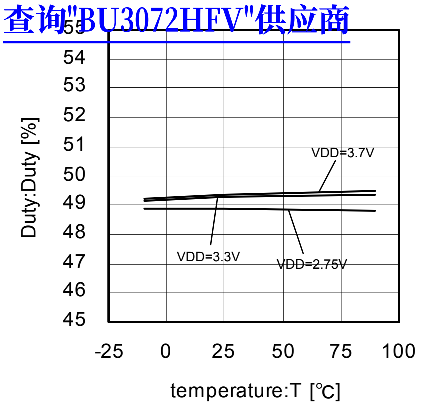


Fig.79 48MHz
Duty temperature characteristics

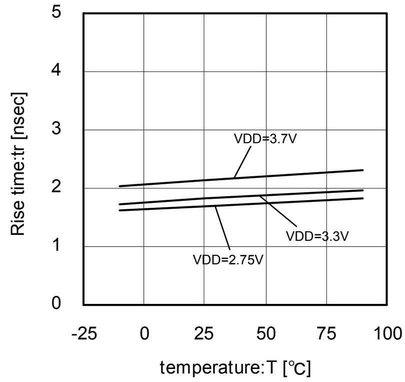


Fig.80 48MHz
Rise-time temperature characteristics

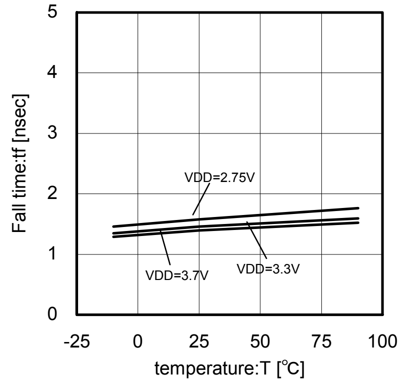


Fig.81 48MHz
Fall-time temperature characteristics

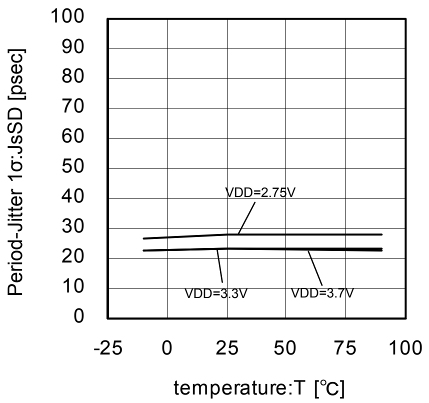


Fig.82 48MHz
Period-Jitter 1 σ temperature characteristics

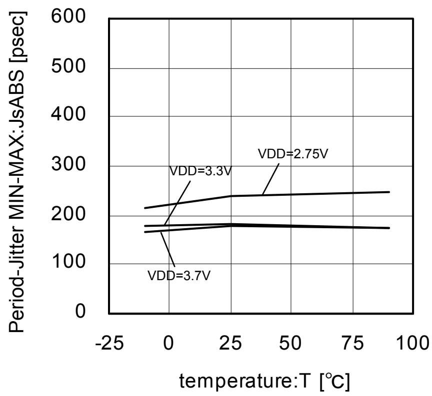


Fig.83 48MHz
Jitter-MinMax temperature characteristics

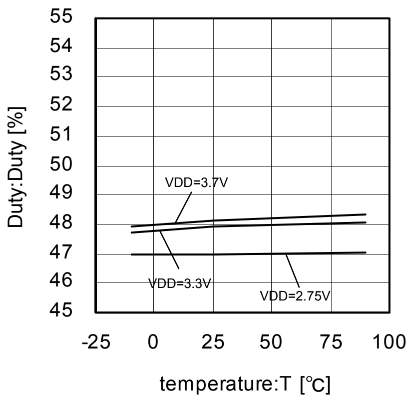


Fig.84 78MHz
Duty temperature characteristics

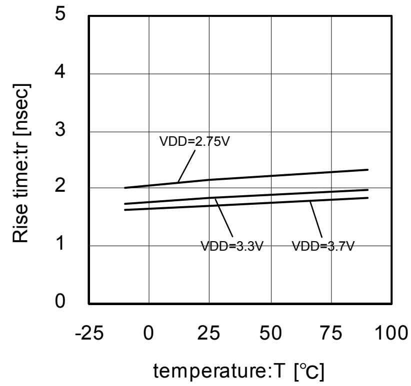


Fig.85 78MHz
Rise-time temperature characteristics

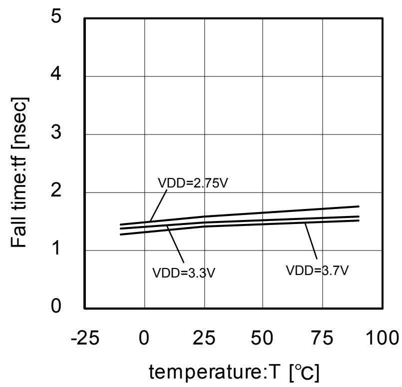


Fig.86 78MHz
Fall-time temperature characteristics

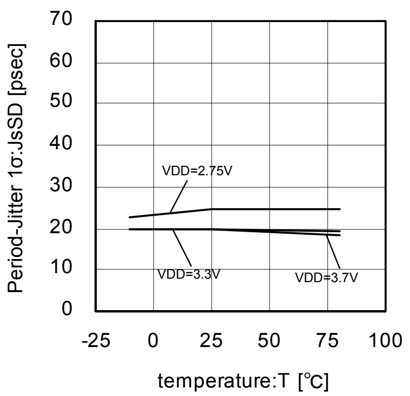


Fig.87 78MHz
Period-Jitter 1 σ temperature characteristics

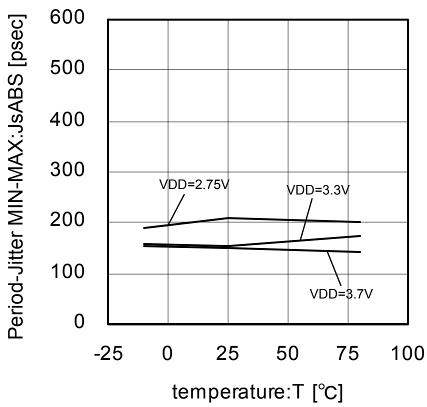


Fig.88 78MHz
Jitter-MinMax temperature characteristics

●Block diagram, pin assignment/functions

(BU3071HFV)

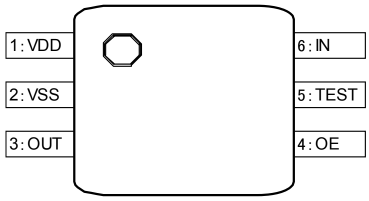


Fig.89

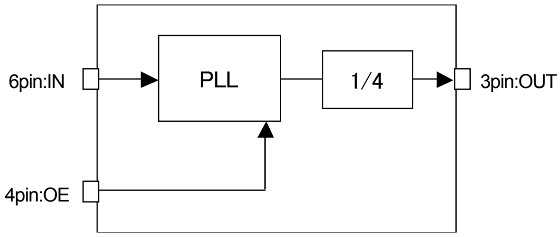


Fig.90

PIN NO.	PIN name	Function
1	VDD	Power supply
2	VSS	GND
3	OUT	Clock output terminal
4	OE	Output enable (L: disable, H: enable), equipped with Pull-down function, output fixed to L at disable
5	TEST	TEST pin, equipped with Pull-down function
6	IN	Clock input pin (28.6363 MHz input)

(BU3072HFV)

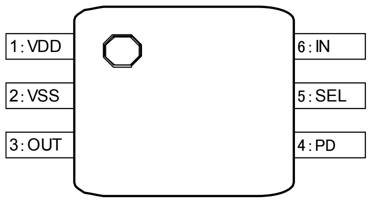


Fig.91

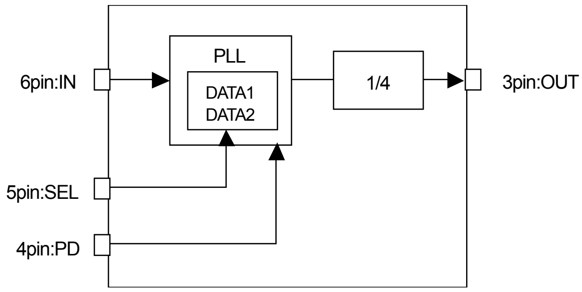


Fig.92

PIN NO.	PIN name	Function
1	VDD	Power supply
2	VSS	GND
3	OUT	Clock output terminal (L：27.0000MHz, H：36.0000MHz)
4	PD	Power-down (L: Hi-Z, H: enable), equipped with Pull-down function, output set to Hi-Z at disable
5	SEL	Output selection (L: 27.0000 MHz, H: 36.0000 MHz)
6	IN	Clock input pin (48.0000 MHz input)

(BU3073HFV)

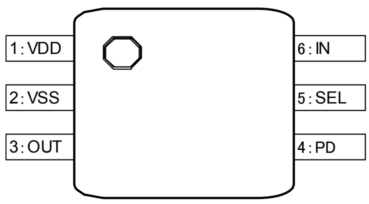


Fig.93

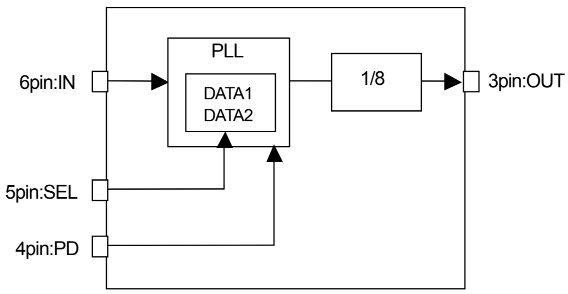


Fig.94

PIN NO.	PIN name	Function
1	VDD	Power supply
2	VSS	GND
3	OUT	Clock output terminal (L：24.3750MHz, H：24.5454MHz)
4	PD	Power-down (L: disable, H: enable), equipped with Pull-down function, output set to L at disable
5	SEL	Output selection (L：24.3750MHz, H：24.5454MHz)
6	IN	Clock input pin (48.0000MHz input)

(BU3076HFV)

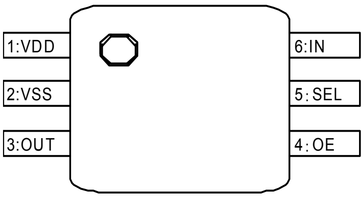


Fig.95

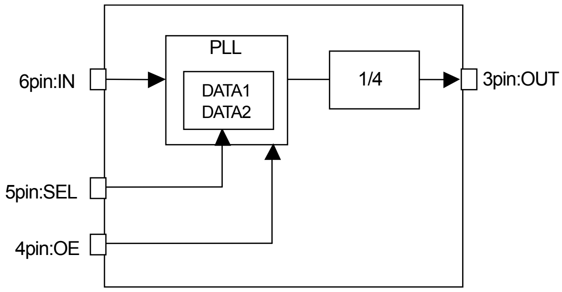


Fig.96

PIN NO.	PIN name	Function
1	VDD	Power supply
2	VSS	GND
3	OUT	Clock output terminal (L：54.0000MHz, H：67.5000MHz)
4	OE	Power-down (L: disable, H: enable), equipped with Pull-down function, output set to L at disable
5	SEL	Output selection (L：54.0000MHz, H：67.5000MHz)
6	IN	Clock input pin (27.0000MHz input)

(BU7322HFV)

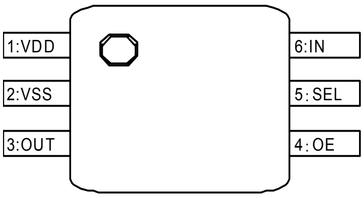


Fig.97

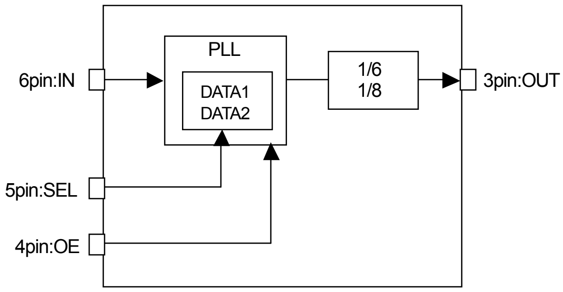


Fig.98

PIN NO.	PIN name	Function
1	VDD	Power supply
2	VSS	GND
3	OUT	Clock output terminal (L：49.5000MHz, H：36.0000MHz)
4	OE	Power-down (L：disable ,H：enable) equipped with Pull-down function, disable output set to L at disable
5	SEL	Output selection (L：49.5000MHz, H：36.0000MHz) equipped with Pull-down function
6	IN	Clock input pin (27.0000MHz input)

(BU7325HFV)

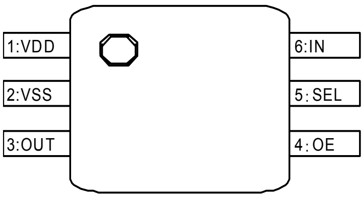


Fig.99

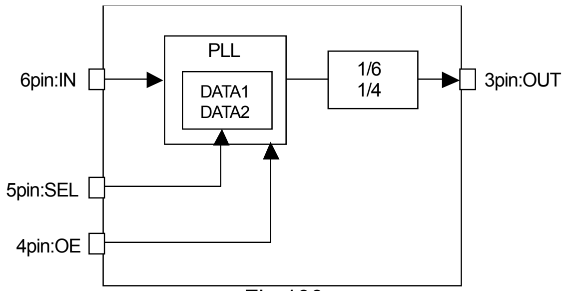


Fig.100

PIN NO.	PIN name	Function
1	VDD	Power supply
2	VSS	GND
3	OUT	Clock output terminal (L：48.0000MHz, H：78.0000MHz)
4	OE	Power-down (L：disable ,H：enable) equipped with Pull-down function, disable output set to L at disable
5	SEL	Output selection (L：48.0000MHz, H：78.0000MHz)
6	IN	Clock input pin (27.0000MHz input)

● Application circuit example

(BU3071HFV)

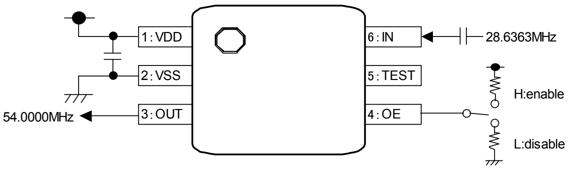


Fig.101

(BU3072HFV)

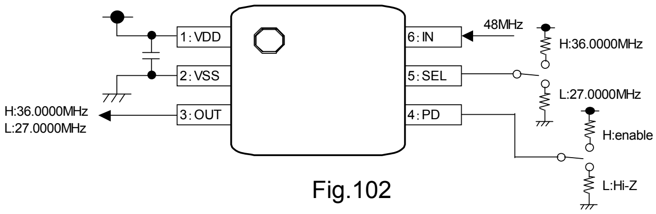


Fig.102

(BU3073HFV)

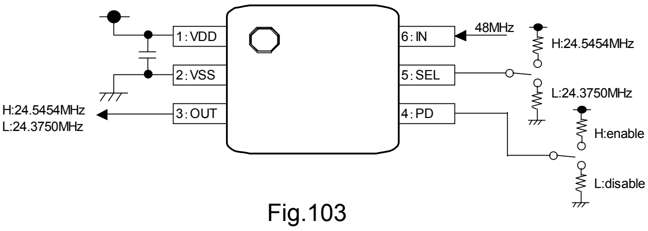


Fig.103

(BU3076HFV)

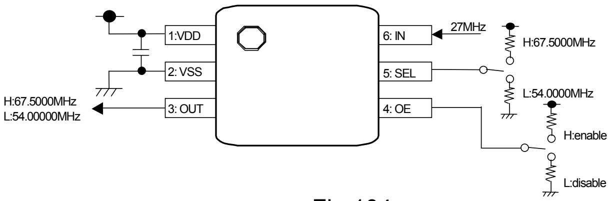


Fig.104

(BU7322HFV)

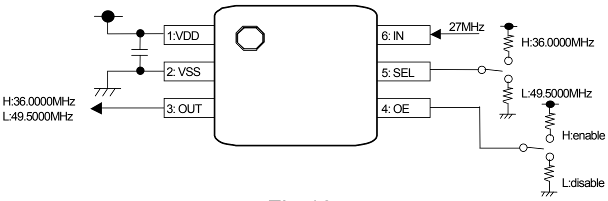


Fig.105

(BU7325HFV)

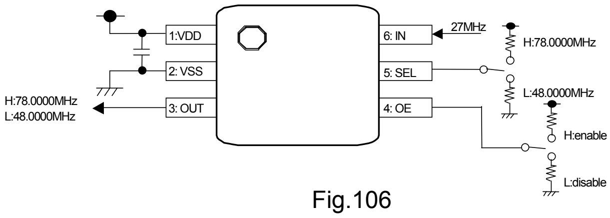


Fig.106

∗ For VDD and VSS, insert a bypass capacitor of approx. 0.1 μF as close as possible to the pin.

∗ Bypass capacitors with good high-frequency characteristics are recommended.

∗ Even though we believe that the typical application circuit is worth of a recommendation, please be sure to thoroughly recheck the characteristics before use.

●Equivalent circuit

3-pin (Output pin)

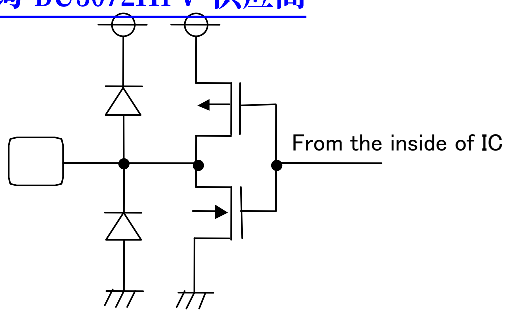


Fig.107

BU3071HFV, BU3073HFV, BU3076HFV

BU7322HFV, BU7325HFV

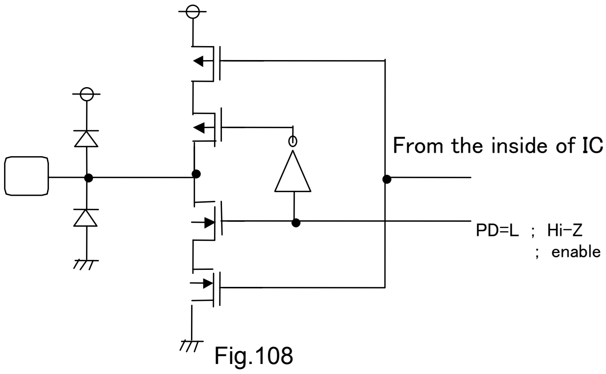


Fig.108

BU3072HFV

4-pin (Input pin)

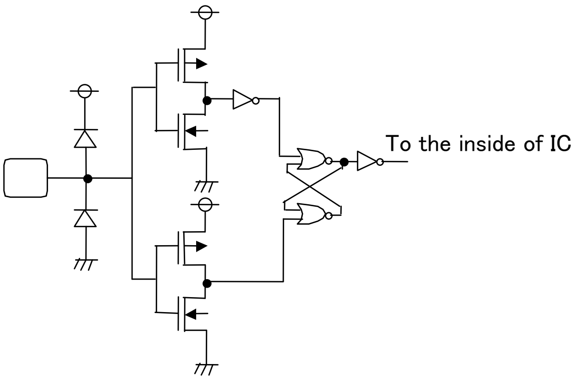


Fig.109

5-pin (Input pin)

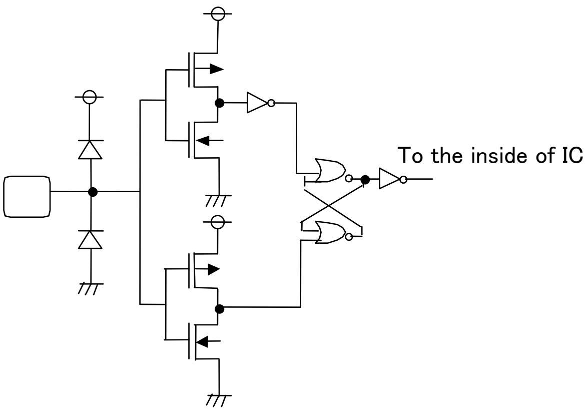


Fig.110

BU3072HFV, BU3073HFV, BU3076HFV

BU7322HFV, BU7325HFV

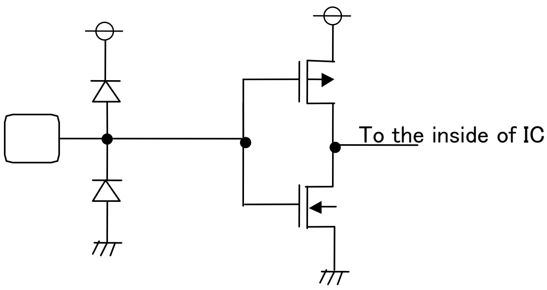


Fig.111

BU3071HFV

6-pin (Input pin)

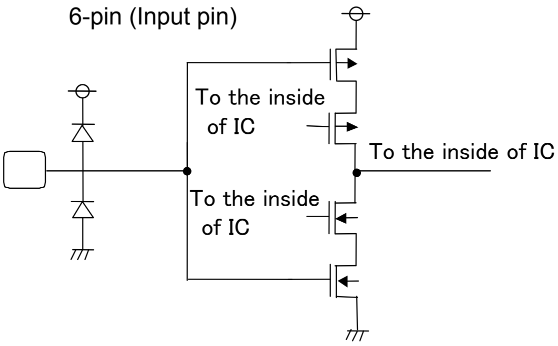


Fig.112

BU3072HFV, BU3073HFV, BU3076HFV

BU7322HFV, BU7325HFV

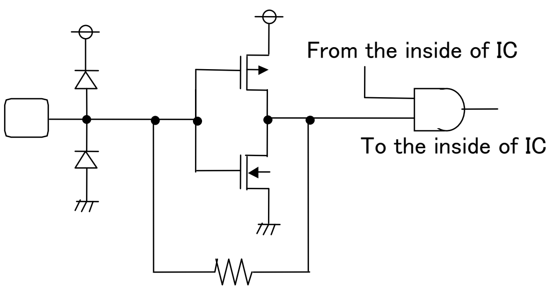


Fig.113

BU3071HFV

●Appearance of Marker

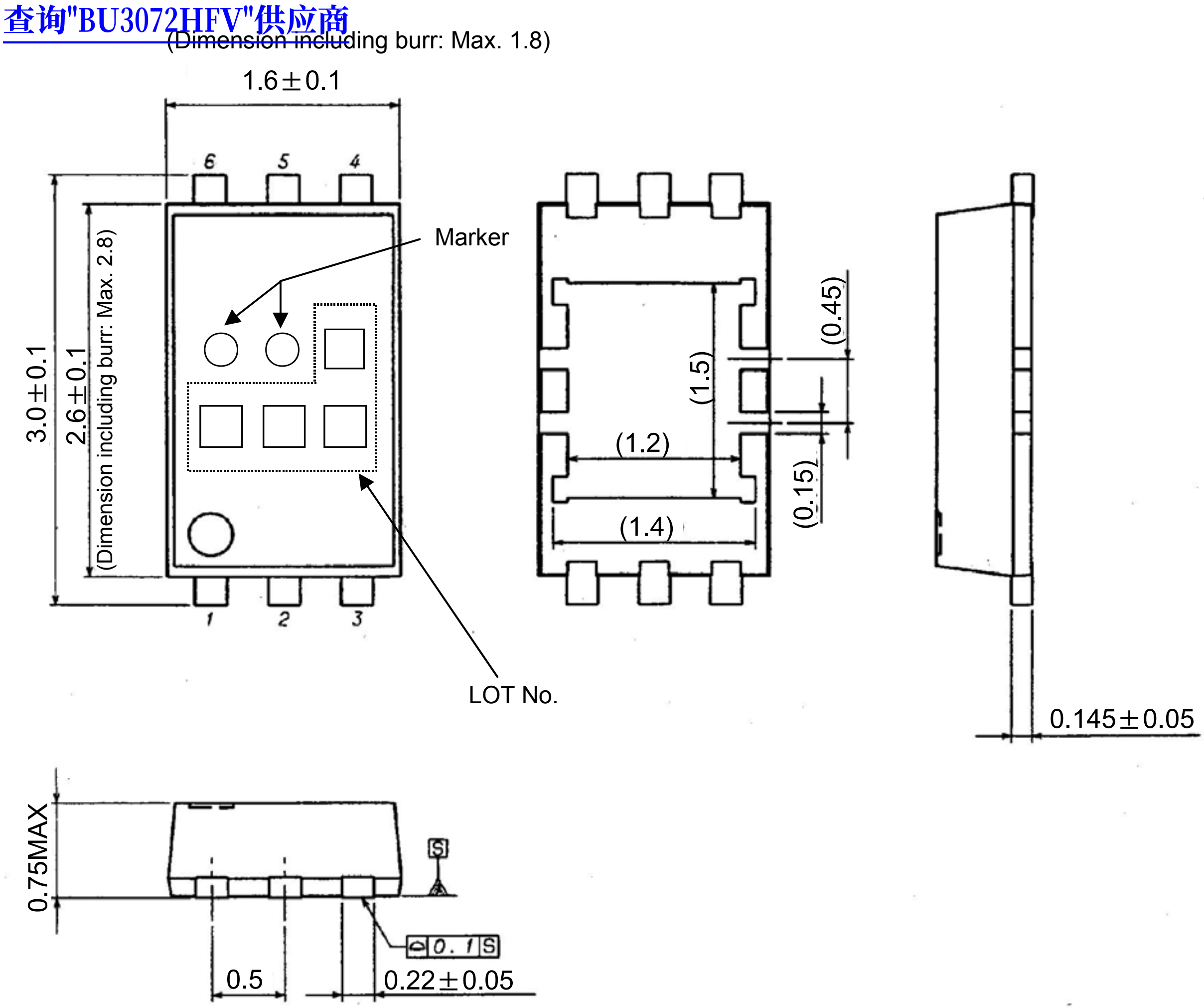


Fig.114 (UNIT : mm)

・List of markers

Model name	Marker
BU3071HFV	AB
BU3072HFV	AC
BU3073HFV	AD
BU3076HFV	AA
BU7322HFV	AE
BU7325HFV	AH

●Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as applied voltage (VDD or VIN), operating temperature range (Topr), etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Recommended operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.
In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

查询"BU3072HFV"供应商

●Product Designation

B	U		3	0	7	1		H	F	V	-	T	R

Part No.

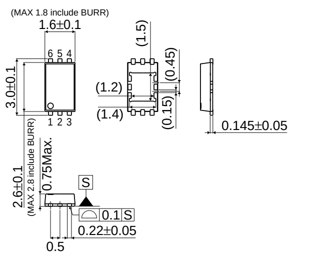
Type
3071
3072
3073
3076
7322
7325

Package Type
HFV : HVSOF6

Package and forming specification
TR: Embossed tape and reel

HVSOF6

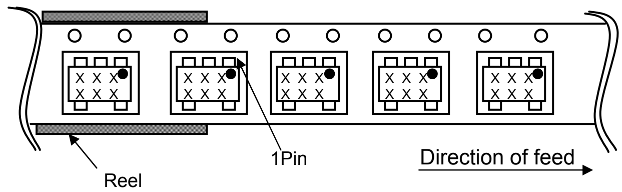
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper light when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

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