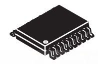


SWITCHMODE LEAD-ACID BATTERY CHARGER

Check for Samples: UC2909-EP

FEATURES

- **Accurate and Efficient Control of Battery Charging**
- **Average Current Mode Control from Trickle to Overcharge**
- **Resistor Programmable Charge Currents**
- **Thermistor Interface Tracks Battery Requirements Over Temperature**
- **Output Status Bits Report on Four Internal Charge States**
- **Undervoltage Lockout Monitors VCC and VREF**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

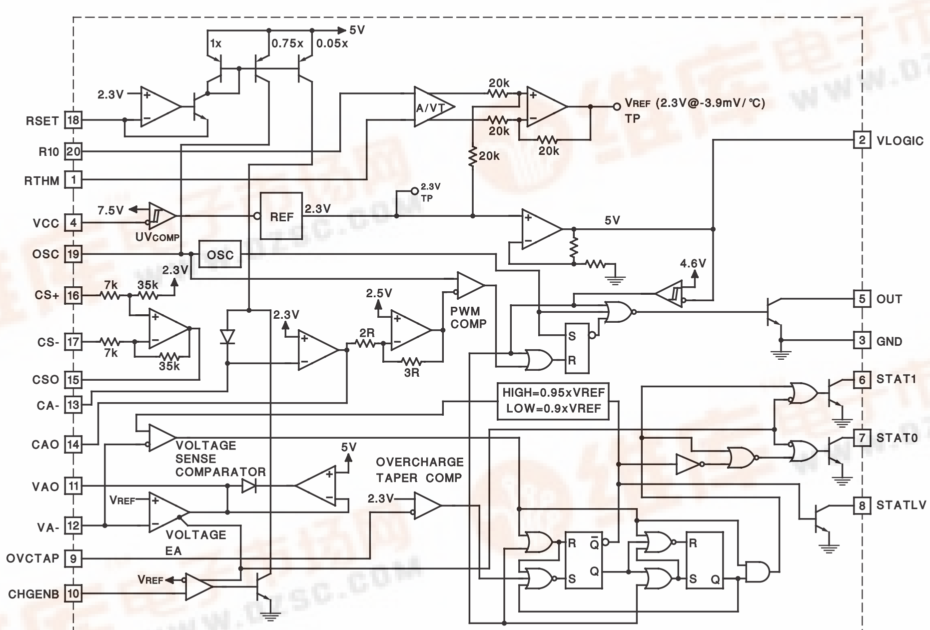
- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**
- **Not to Exceed 185.35-KHz Oscillation Frequency at 125°C**

(1) Additional temperature ranges available - contact factory

DESCRIPTION

The UC2909 controls lead acid battery charging with a highly efficient average current mode control loop. This chip combines charge state logic with average current PWM control circuitry. Charge state logic commands current or voltage control depending on the charge state. The chip includes undervoltage lockout circuitry to insure sufficient supply voltage is present before output switching starts. Additional circuit blocks include a differential current sense amplifier, a 1.5% voltage reference, a –3.9-mV/°C thermistor linearization circuit, voltage and current error amplifiers, a PWM oscillator, a PWM comparator, a PWM latch, charge state decode bits, and a 100-mA open collector output driver.

FUNCTION BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	DW	UC2909MDWREP	UC2909EP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

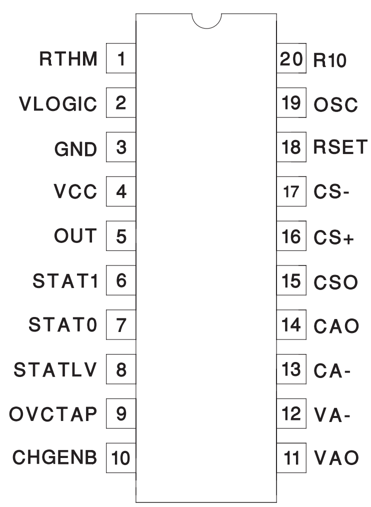
ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range unless otherwise noted

				UNITS
VCC	Supply voltage	OUT, STAT0, STAT1	40	V
	Output current sink		0.1	A
	CS+, CS-		–0.4 to V_{CC}(3)	V
	Remaining pin voltages		–0.3 to 9	V
T_{stg}	Storage temperature		-55 to 150	°C
T_J	Junction temperature range		-55 to 150	°C
	Lead temperature (soldering, 10 seconds)		300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.
(2) All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.
(3) Voltages more negative than -0.4 V can be tolerated if current is limited to 50 mA.

DW PACKAGE
(TOP VIEW)



ELECTRICAL CHARACTERISTICS

T_A = –55°C to 125°C; C_T = 430 pF, R_{SET} = 11.5 KΩ, R10 = 10 KΩ, R_{THM} = 10 KΩ, V_{CC} = 15 V, Output no load, R_{STAT0} = R_{STAT1} = 10 KΩ, CHGENB = OVCTAP = VLOGIC, T_A = T_J (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE AMPLIFIER (CSA) (V_{ID} = CS+ - CS-)						
	DC gain	CS- = 0 V, CS+ = -50 mV; CS+ = –200 mV	4.8	5	5.7	V/V
		CS+ = 0 V, CS- = 50 mV; CS- = 250 mV	4.8	5	5.1	
V_{OFFSET}	Offset voltage (V_{CSO} - V_{CAO})	CS+ = CS- = 2.3 V, CAO = CA-			45	mV
CMRR		V_{CM} = -0.2 V to V_{CC} - 2, 8.8 V < V_{CC} < 14 V	50			dB
		V_{CM} = -0.2 V to V_{CC}, 14 V < V_{CC} < 35 V	50			
V_{OL}		V_{ID} = -550 mV, -0.2 V < V_{CM} < V_{CC} - 2, I_O = 500 µA		0.3	0.6	V
V_{OH}		V_{ID} = 700 mV, -0.2 V < V_{CM} < V_{CC} - 2, I_O = -250 µA	5.2	5.7	6.2	V
	Output source current	V_{ID} = 700 mV, CSO = 4 V		-1	-0.5	mA
	Output sink current	V_{ID} = -55 0mV, CSO = 1 V	3	4.5		mA
	3dB bandwidth(1)	V_{ID} = 90 mV, V_{CM} = 0 V		200		KHz
CURRENT ERROR AMPLIFIER (CEA)						
I_B		8.8 V < V_{CC} < 35 V, V_{CHGENB} = V_{LOGIC}		0.1	0.8	µA
V_{IO}(2)		8.8 V < V_{CC} < 35 V, CAO = CA-		10		mV
A_{VO}		1 V < V_{AO} < 4 V	60	90		dB
GBW		T_J = 25°C, f = 100 KHz	1	1.5		MHz
V_{OL}		I_O = 250 µA		0.4	0.6	V
V_{OH}		I_O = –5 mA	4.5	5		V
	Output source current	CAO = 4 V		-25	-12	mA
	Output sink current	CAO = 1 V	2	3		mA
I_{CA-}, $I_{TRCK\_CONTROL}$		V_{CHGENB} = GND	8.5	10	11.5	µA
VOLTAGE AMPLIFIER (CEA)						
I_B		Total bias current; regulating level		0.1	1	µA
V_{IO}(2)		8.8 V < V_{CC} < 35 V, V_{CM} = 2.3 V, V_{AO} = V_{A-}		1.2		mV
A_{VO}		1 V < CAO < 4 V	60	90		dB
GBW		T_J = 25°C, f = 100 KHz	0.25	0.5		MHz
V_{OL}		I_O = 500 µA		0.4	0.6	V
V_{OH}		I_O = -500 µA	4.75	5	5.25	V
	Output source current	CAO = 4 V	-2	-1		mA
	Output sink current	CAO = 1 V	2	2.5		mA
	VAO leakage: high impedance state	V_{CHGENB} = GND, STAT0 = 0 and STAT1 = 0, V_{AO} = 2.3 V	-1		1	µA

(1) Not tested in production.
(2) V_{IO} is measured prior to packaging with internal probe pad.

ELECTRICAL CHARACTERISTICS (continued)

T_A = –55°C to 125°C; C_T = 430 pF, R_{SET} = 11.5 KΩ, R10 = 10 KΩ, R_{THM} = 10 KΩ, V_{CC} = 15 V, Output no load, R_{STAT0} = R_{STAT1} = 10 KΩ, CHGENB = OVCTAP = VLOGIC, T_A = T_J (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PULSE WIDTH MODULATOR					
Maximum duty cycle	CAO = 0.6 V	90	95	100	%
Modulator gain	CAO = 2.5 V, 3.2 V	63	71	80	%/V
OSC peak			3		V
OSC valley			1		V
OSCILLATOR					
Frequency	8.8 V < V_{CC} < 35 V	151.65	168.50	185.35	KHz
THERMISTOR DERIVED (V_{ID} = V_{RTHM} - V_{R10})					
Initial accuracy, V_{AO} (R_{THM} = 10 KΩ)	V_{ID} = 0 V, R10 = R_{THM} = 10 KΩ[3]	2.250	2.300	2.350	V
Line regulation	V_{CC} = 8.8 V to 35 V		3	10	mV
V_{AO}	R_{THM} = 138 KΩ, R10 = 10 KΩ	2.435	2.495	2.545	V
	R_{THM} = 33.63 KΩ, R10 = 10 KΩ	2.340	2.398	2.446	
	R_{THM} = 1.014 KΩ, R10 = 10 KΩ	2.015	2.066	2.107	
CHARGE ENABLE COMPARATOR (CEC)					
Threshold voltage	As a function of V_{A-}	0.99	1	1.01	V/V
Input bias current	CHGENB = 2.3 V	-0.5	-0.1		µA
VOLTAGE SENSE COMPARATOR (VSC)					
Threshold voltage	STAT0 = 0, STAT1 = 0, Function of V_{REF}	0.944	0.95	0.955	V/V
	STAT0 = 1, STAT1 = 0, Function of V_{REF}	0.895	0.9	0.905	
OVER CHARGE TAPER CURRENT COMPARATOR (OCTIC)					
Threshold voltage	Function of 2.3 V REF, CA- = CAO	0.99	1	1.01	V/V
Input bias current	OVCTAP = 2.3 V	-0.5	-0.1		µA
LOGIC 5 V (VLOGIC)					
VLOGIC	V_{CC} = 15 V	4.875	5	5.125	V
Line regulation	8.8 V < V_{CC} < 35 V		3	15	mV
Load regulation	0 A < I_O < 10 mA		3	15	mV
Reference comparator turn-on threshold			4.3	4.85	V
Short circuit current	V_{REF} = 0 V	30	50	80	mA
OUTPUT STAGE					
I_{SINK} continuous			50		mA
I_{PEAK}			100		mA
V_{OL}	I_O = 50 mA		1	1.4	V
Leakage current	V_{OUT} = 35 V			25	µA

(3) Thermistor initial accuracy is measured and trimmed with respect to V_{AO}; V_{AO} = V_{A-}.

ELECTRICAL CHARACTERISTICS (continued)

T_A = –55°C to 125°C; C_T = 430 pF, R_{SET} = 11.5 KΩ, R10 = 10 KΩ, R_{THM} = 10 KΩ, V_{CC} = 15 V, Output no load, R_{STAT0} = R_{STAT1} = 10 KΩ, CHGENB = OVCTAP = VLOGIC, T_A = T_J (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STAT0 AND STAT1 OPEN COLLECTOR OUTPUTS					
Maximum sink current	V_{OUT} = 8.8 V	5	10		mA
Saturation voltage	I_{OUT} = 5 mA		0.1	0.45	V
Leakage current	V_{OUT} = 35 V			25	µA
STATLV OPEN COLLECTOR OUTPUTS					
Maximum sink current	V_{OUT} = 5 V	2	5		mA
Saturation voltage	I_{OUT} = 2 mA		0.1	0.45	V
Leakage current	V_{OUT} = 5 V			3	µA
UVLO					
Turn-on Threshold		6.8	7.8	8.8	V
Hysteresis		100	300	500	mV
I_{CC}					
I_{CC} (run)	See Figure 1		13	19	mA
I_{CC} (off)	V_{CC} = 6.5 V		2		mA

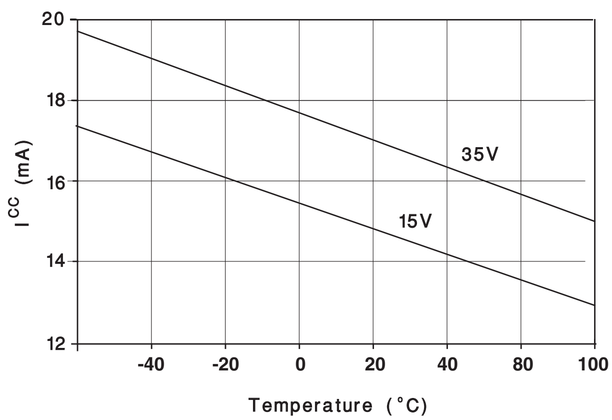
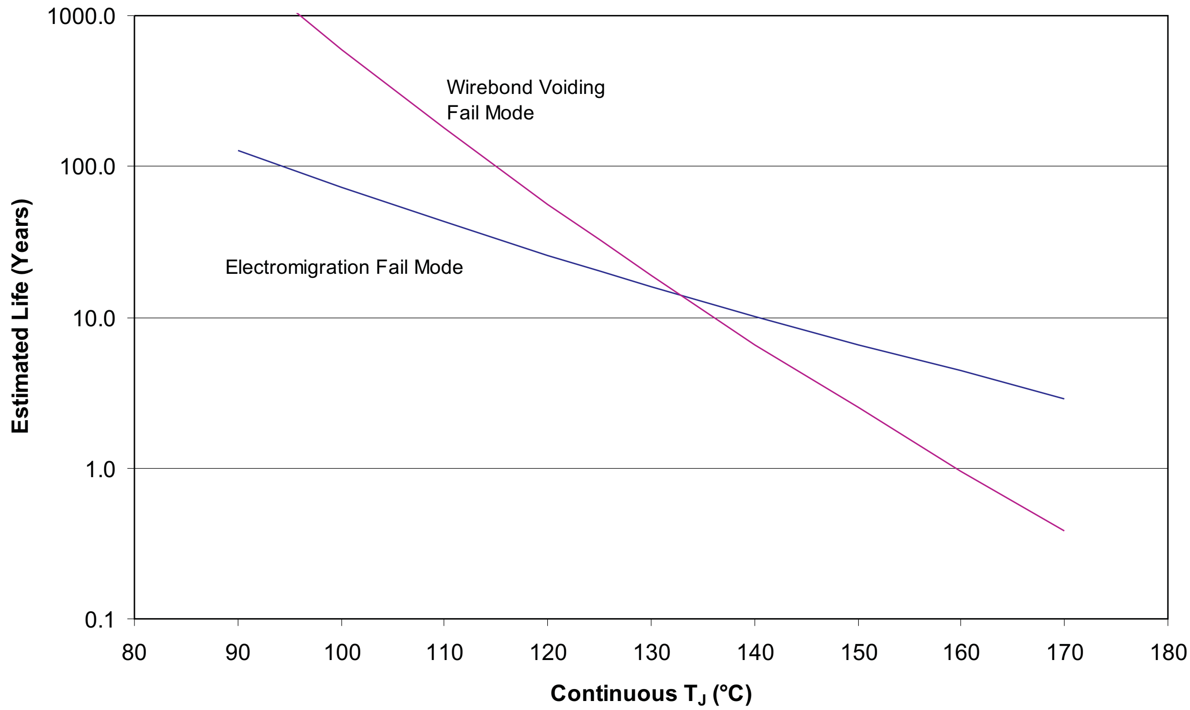


Figure 1. I_{CC} vs Temperature



Notes:

1. See datasheet for absolute maximum and minimum recommended operating conditions.
2. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
3. Enhanced plastic product disclaimer applies.

Figure 2. UC2909-EP Operating Life Derating Chart

DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
CA-	13	The inverting input to the current error amplifier.
CAO	14	The output of the current error amplifier which is internally clamped to approximately 4 V. It is internally connected to the inverting input of the PWM comparator.
CS-, CS+	17, 16	The inverting and non-inverting inputs to the current sense amplifier. This amplifier has a fixed gain of five and a common-mode voltage range of from –250 mV to V_{CC}.
CSO	15	The output of the current sense amplifier which is internally clamped to approximately 5.7 V.
CHGENB	10	The input to a comparator that detects when battery voltage is low and places the charger in a trickle charge state. The charge enable comparator makes the output of the voltage error amplifier a high impedance while forcing a fixed 10 mA into CA- to set the trickle charge current.
GND	3	The reference point for the internal reference, all thresholds, and the return for the remainder of the device. The output sink transistor is wired directly to this pin.
OVCTAP	9	The overcharge current taper pin detects when the output current has tapered to the float threshold in the overcharge state.
OSC	19	The oscillator ramp pin which has a capacitor (C_T) to ground. The ramp oscillates between approximately 1 V to 3 V and the frequency is approximated by: $$frequency = \frac{1}{1.2 \bullet C_T \bullet R_{SET}} \quad (1)$$
OUT	5	The output of the PWM driver which consists of an open collector output transistor with 100-mA sink capability.
R10	20	Input used to establish a differential voltage corresponding to the temperature of the thermistor. Connect a 10-KΩ resistor to ground from this point.
RSET	18	A resistor to ground programs the oscillator charge current and the trickle control current for the oscillator ramp. The oscillator charge current is approximately: $$\frac{1.75}{R_{SET}} \quad (2)$$ The trickle control current ($I_{TRCK\_CONTROL}$) is approximately: $$\frac{0.115}{R_{SET}} \quad (3)$$
RTHM	1	A 10-KΩ thermistor is connected to ground and is thermally connected to the battery. The resistance will vary exponentially over temperature and its change is used to vary the internal 2.3-V reference by -3.9 mV/°C. The recommended thermistor for this function is part number L1005-5744-103-D1, Keystone Carbon Company, St. Marys, PA.
STAT0	7	This open collector pin is the first decode bit used to decode the charge states.
STAT1	6	This open collector pin is the second decode bit used to decode the charge states.
STATLV	8	This bit is high when the charger is in the float state.
VA-	12	The inverting input to the voltage error amplifier.
VAO	11	The output of the voltage error amplifier. The upper output clamp voltage of this amplifier is 5 V.
VCC	4	The input voltage to the chip. The chip is operational between 7.5 V and 40 V and should be bypassed with a 1-µF capacitor. A typical I_{CC} vs. temperature is shown in Figure 1.
VLOGIC	2	The precision reference voltage. It should be bypassed with a 0.1-µF capacitor.

CHARGE STATE DECODE CHART

STAT0 and STAT1 are open collector outputs. The output is approximately 0.2 V for a logic 0.

	STAT1	STAT0
Trickle charge	0	0
Bulk charge	0	1
Over charge	1	0
Float charge	1	1

APPLICATION INFORMATION

A block diagram of the UC2909 is shown on the first page, while a typical application circuit is shown in Figure 3. The circuit in Figure 3 requires a DC input voltage between 12 V and 40 V.

The UC2909 uses a voltage control loop with average current limiting to precisely control the charge rate of a lead-acid battery. The small increase in complexity of average current limiting is offset by the relative simplicity of the control loop design.

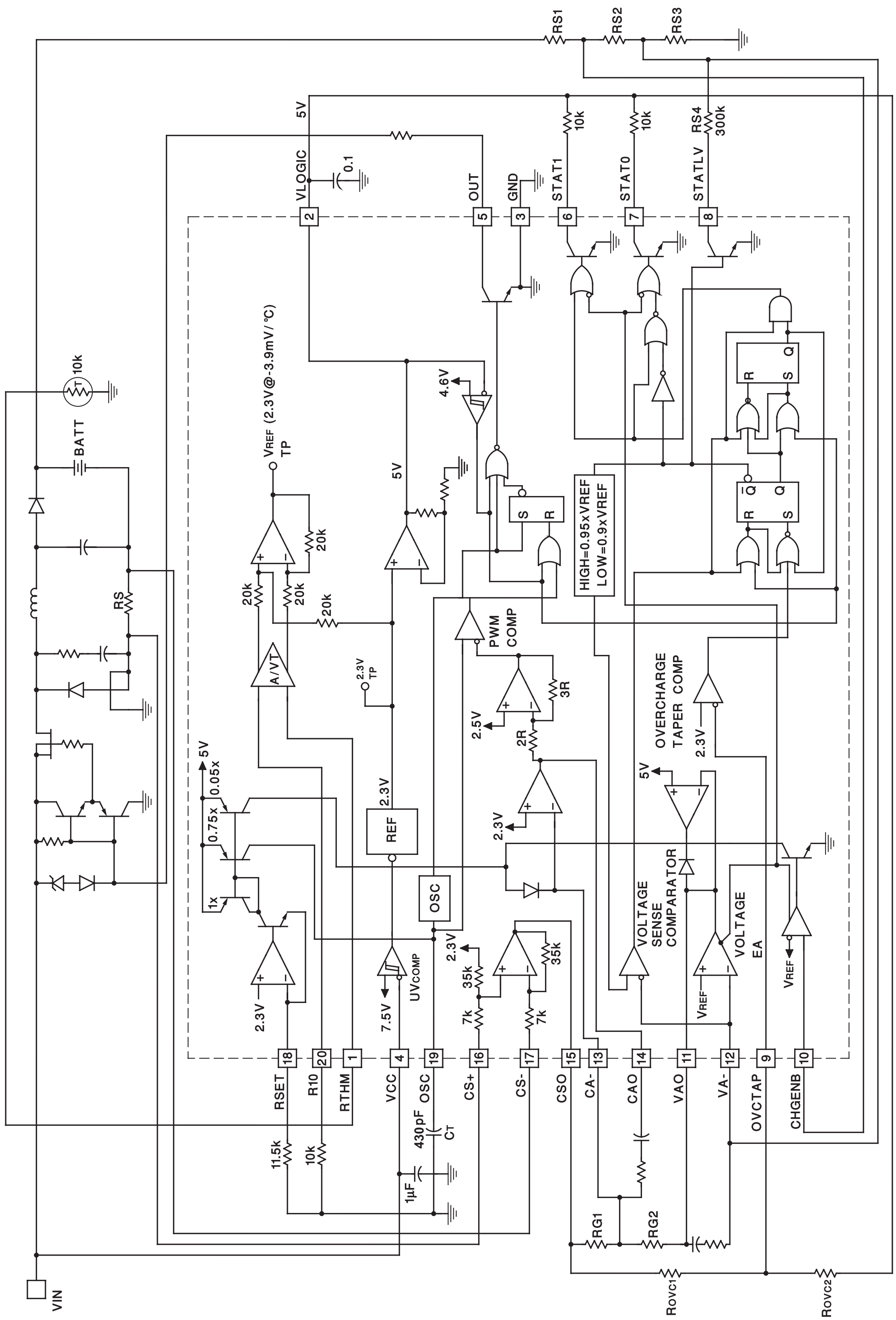


Figure 3. Typical Application Circuit

Control Loop

Current Sense Amplifier

This amplifier measures the voltage across the sense resistor RS with a fixed gain of five and an offset voltage of 2.3 V. This voltage is proportional to the battery current. The most positive voltage end of RS is connected to CSensuring the correct polarity going into the PWM comparator.

CSO = 2.3 V when there is zero battery current.

RS is chosen by dividing 350 mV by the maximum allowable load current. A smaller value for RS can be chosen to reduce power dissipation.

Maximum charge current, I_{bulk}, is set by knowing the maximum voltage error amplifier output, V_{OH} = 5 V, the maximum allowable drop across RS, and setting the resistors RG1 and RG2 such that:

$$\frac{RG1}{RG2} = \frac{5 \bullet V_{RS}}{VLOGIC - CA-} = \frac{5 \bullet V_{RS}}{5\ V - 2.3\ V} = \frac{5 \bullet V_{RS}}{2.7\ V} = 1.852 \bullet I_{BULK} \bullet RS \tag{4}$$

The maximum allowable drop across RS is specified to limit the maximum swing at CSO to approximately 2 V to keep the CSO amplifier output from saturating.

No charge/load current: V_{CSO} = 2.3 V

Max charge/load current: $V_{max(CSO)}$ = 2.3 V - 2 V = 0.3 V

Voltage Error Amplifier

The voltage error amplifier (VEA) senses the battery voltage and compares it to the 2.3-V - 3.9-mV/°C thermistor generated reference. Its output becomes the current command signal and is summed with the current sense amplifier output. A 5-V voltage error amplifier upper clamp limits maximum load current. During the trickle charge state, the voltage amplifier output is opened (high impedance output) by the charge enable comparator. A trickle bias current is summed into the CA- input which sets the maximum trickle charge current.

The VEA, V_{OH} = 5 V clamp saturates the voltage loop and consequently limits the charge current as stated in Equation 4.

During the trickle bias state the maximum allowable charge current (ITC) is similarly determined:

$$ITC = \frac{I_{TRCK\_CONTROL} \bullet RG1}{RS \bullet 5} \tag{5}$$

$I_{TRCK\_CONTROL}$ is the fixed control current into CA-. $I_{TRCK\_CONTROL}$ is 10 µA when R_{SET} = 11.5 KΩ. See RSET pin description for equation.

Current Error Amplifier

The current error amplifier (CA) compares the output of the current sense amplifier to the output of the voltage error amplifier. The output of the CA forces a PWM duty cycle which results in the correct average battery current. With integral compensation, the CA will have a very high DC current gain, resulting in effectively no average DC current error. For stability purposes, the high frequency gain of the CA must be designed such that the magnitude of the down slope of the CA output signal is less than or equal to the magnitude of the up slope of the PWM ramp.

Charge Algorithm

Trickle Charge State
STAT0 = STAT1 = STATLV = logic 0

When CHGNB is less than VREF (2.3 V - 3.9 mV/°C), STATLV is forced low. This decreases the sense voltage divider ratio, forcing the battery to overcharge (V_{OC}).

$$V_{OC} = (V_{REF}) \bullet \frac{(RS1 + RS2 + RS3 \parallel RS4)}{(RS3 \parallel RS4)} \tag{6}$$

During the trickle charge state, the output of the voltage error amplifier is high impedance. The trickle control current is directed into the CA- pin setting the maximum trickle charge current. The trickle charge current is defined in Equation 5.

Bulk Charge State
STAT1 = STATLV = logic 0, STAT0 = logic 1

As the battery charges, the UC2909 will transition from trickle to bulk charge when CHGENB becomes greater than 2.3 V. The transition equation is:

$$V_T = (V_{REF}) \bullet \frac{(RS1 + RS2 + RS3 \parallel RS4)}{(RS2 + RS3 \parallel RS4)} \tag{7}$$

STATLV is still driven low.

During the bulk charge state, the voltage error amplifier is now operational and is commanding maximum charge current (I_{BULK}) set by Equation 4. The voltage loop attempts to force the battery to VOC.

Overcharge State
STAT0 = STATLV = logic 0, STAT1 = logic 1

The battery voltage surpasses 95% of VOC indicating the UC2909 is in its overcharge state.

During the overcharge charge state, the voltage loop becomes stable and the charge current begins to taper off. As the charge current tapers off, the voltage at CSO increases toward its null point of 2.3 V. The center connection of the two resistors between CSO and VLOGIC sets the overcurrent taper threshold (OVCTAP). Knowing the desired overcharge terminate current (I_{OCT}), the resistors R_{OVC1} and R_{OVC2} can be calculated by choosing a value of R_{OVC2} and using the following equation:

$$R_{OVC1} = (1.8518) \bullet I_{OCT} \bullet RS \bullet R_{OVC2} \tag{8}$$

Float State
STAT0 = STAT1 = STATLV = logic 1

The battery charge current tapers below its OVCTAP threshold, and forces STATLV high increasing the voltage sense divider ratio. The voltage loop now forces the battery charger to regulate at its float state voltage (V_F).

$$V_F = (V_{REF}) \bullet \frac{(RS1 + RS2 + RS3)}{RS3} \tag{9}$$

If the load drains the battery to less than 90% of V_F, the charger goes back to the bulk charge state, STATE 1.

Off Line Applications

For off line charge applications, either Figure 4 or Figure 5 can be used as a baseline. Figure 4 has the advantage of high frequency operation resulting in a small isolation transformer. Figure 5 is a simpler design, but at the expense of larger magnetics.

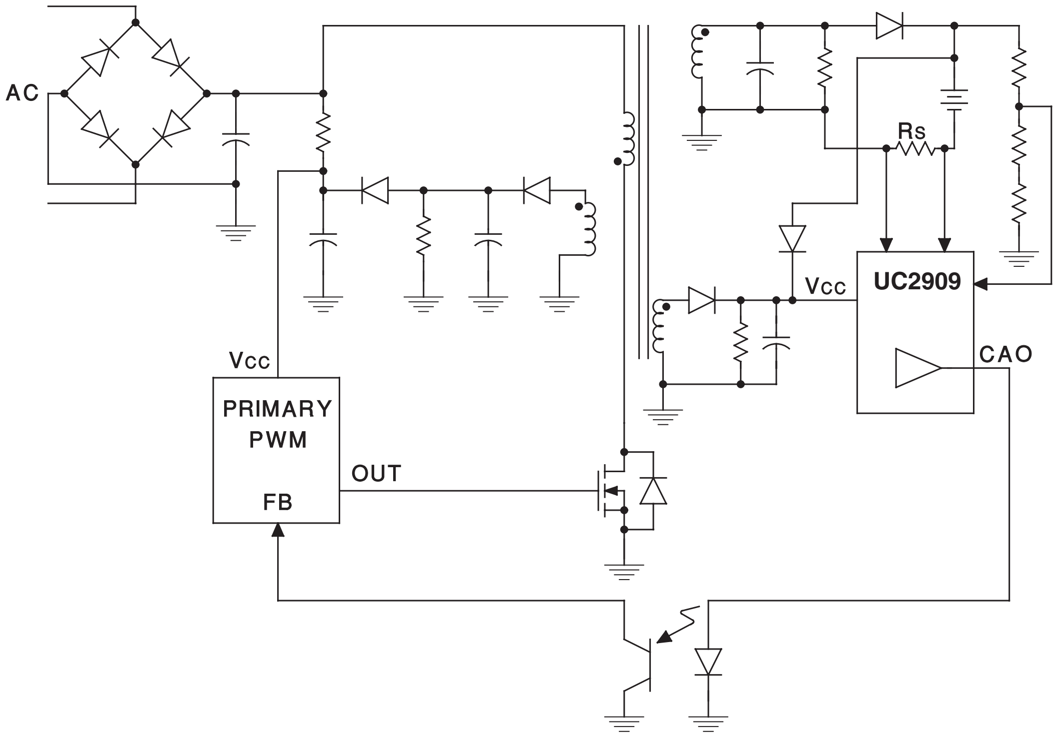


Figure 4. Off Line Charger With Primary Side PWM

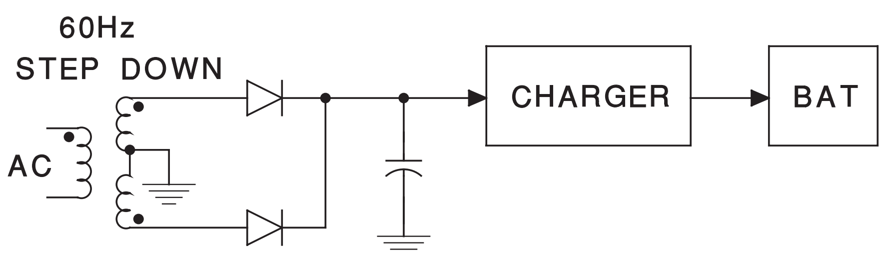


Figure 5. Isolated Off Line Charger

[查询"UC2909-EP"供应商]

www.ti.com

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
UC2909MDWREP	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.t
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical an
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OTHER QUALIFIED VERSIONS OF UC2909-EP :

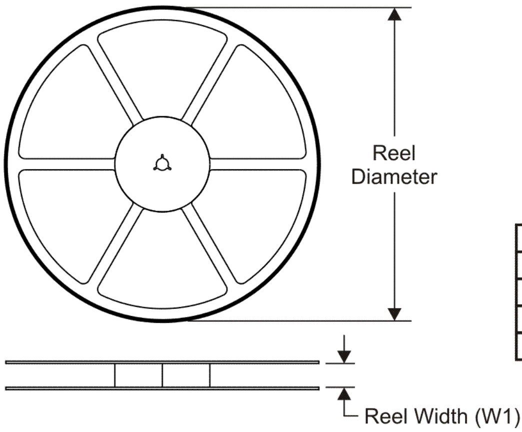
- Catalog: UC2909

NOTE: Qualified Version Definitions:

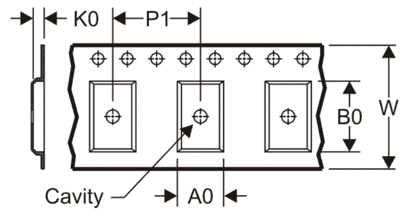
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

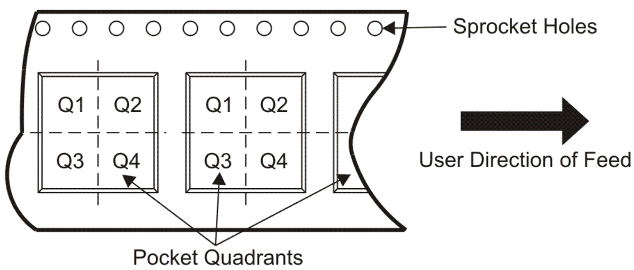


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

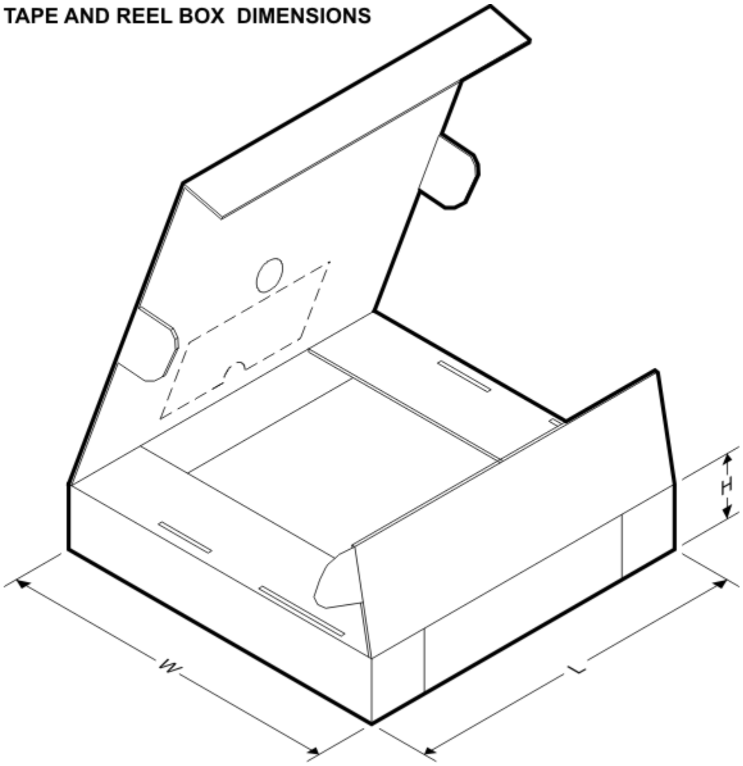
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2909MDWREP	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

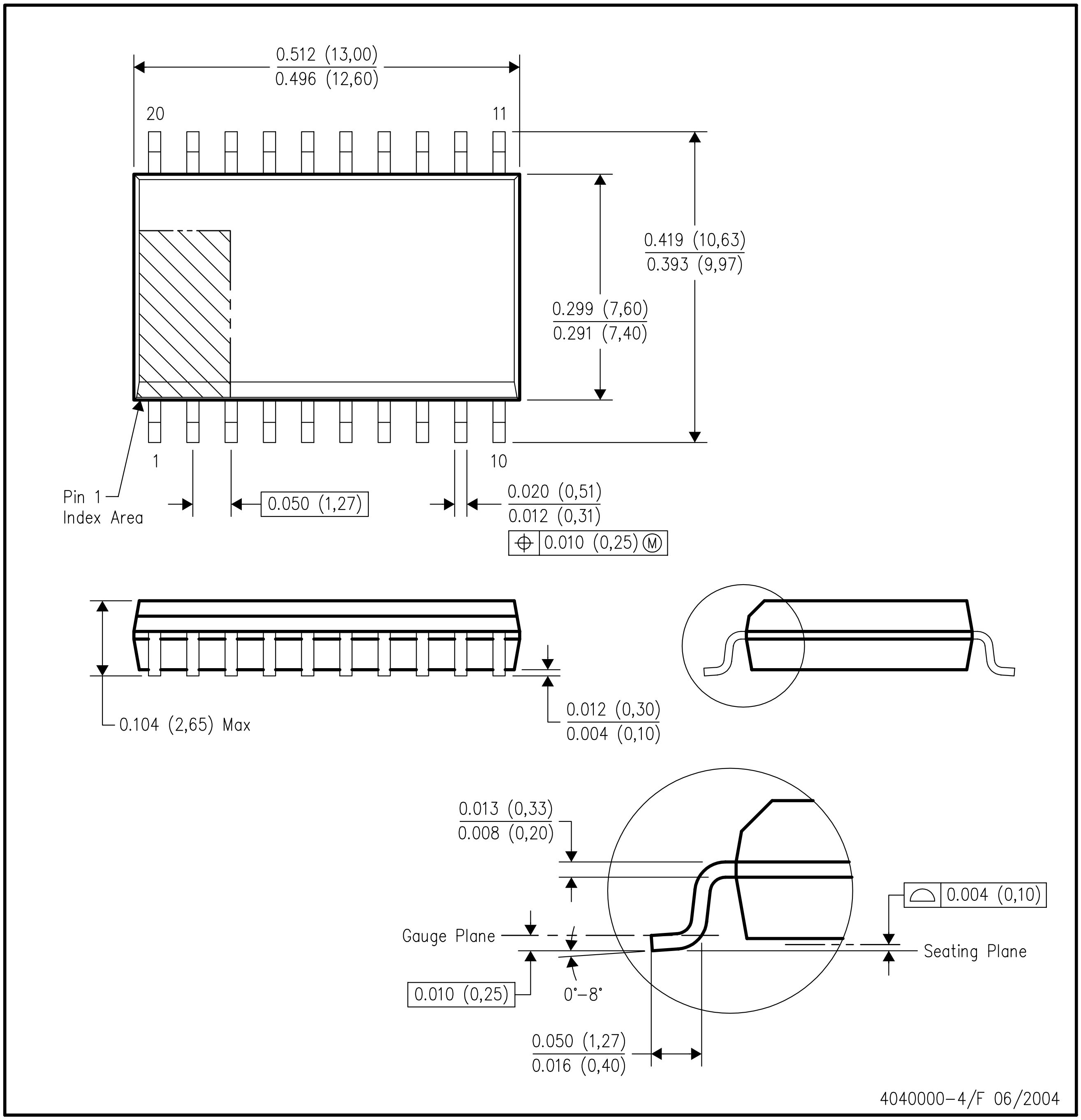
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2909MDWREP	SOIC	DW	20	2000	346.0	346.0	41.0

DW (R-PDSO-G20) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.

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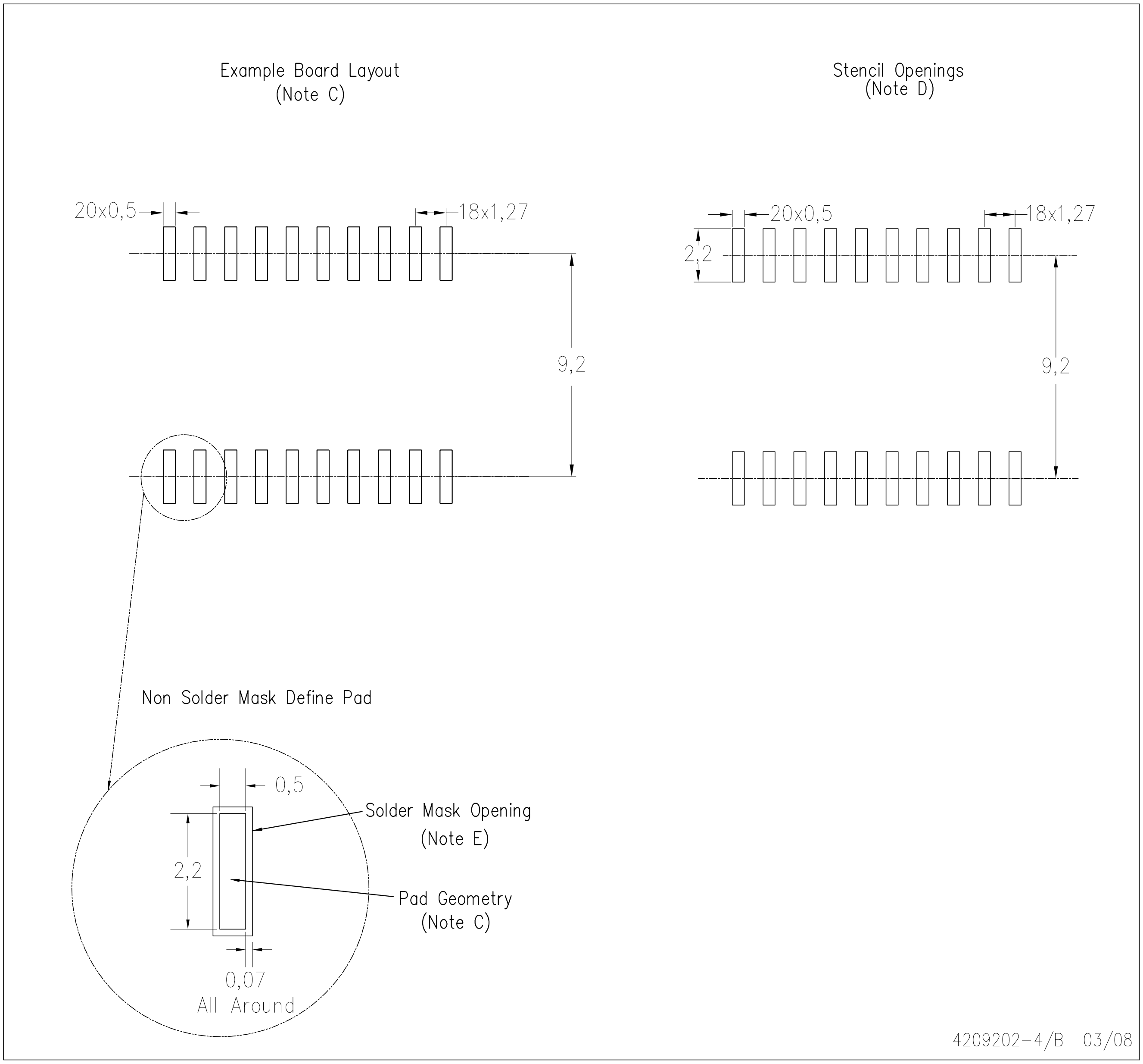
DW (R–PDSO–G20)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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