

August 1995

54F/74F181 4-Bit Arithmetic Logic Unit

General Description

The 'F181 is a 4-bit Arithmetic logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations. It is 40% faster than the Schottky ALU and only consumes 30% as much power.

Features

- Full lookahead for high-speed arithmetic operation on long words
- Guaranteed 4000V minimum ESD protection

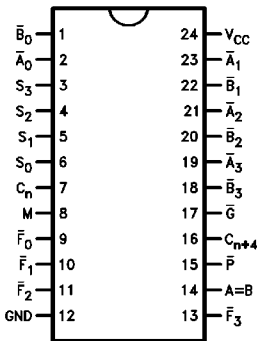
Commercial	Military	Package Number	Package Description
74F181PC		N24A	24-Lead (0.600" Wide) Molded Dual-In-Line
74F181SPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
	54F181DM (Note 2)	J24A	24-Lead Ceramic Dual-In-Line
	54F181SDM (Note 2)	J24F	24-Lead (0.300") Ceramic Dual-In-Line
74F181SC (Note 1)		M24B	24-Lead (0.300") Molded Small Outline, JEDEC
	54F181FM (Note 2)	W24C	24-Lead Cerpack
	54F181LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMOB, FMQB and LMQB.

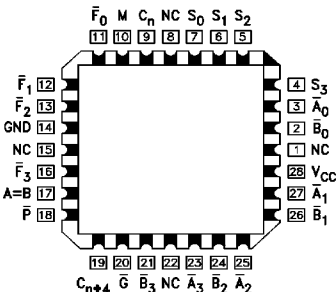
Connection Diagrams

Pin Assignment
for DIP, SOIC and Flatpak



TL/F/9491-1

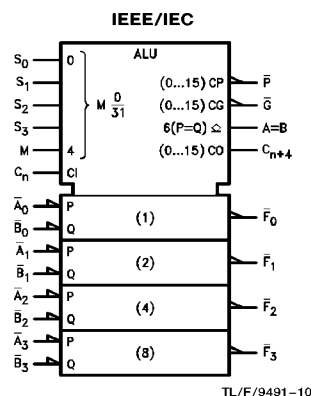
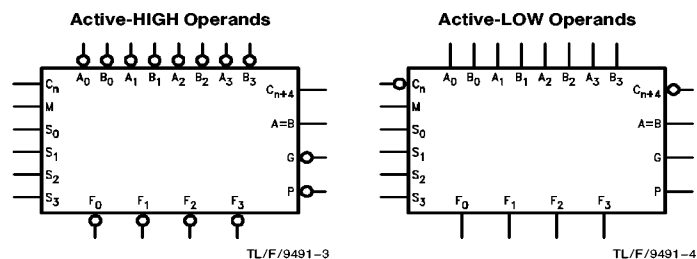
Pin Assignment
for LCC



TL/F/9491-2

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Logic Symbols



Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\bar{A}_0-\bar{A}_3$	A Operand Inputs (Active LOW)	1.0/3.0	20 μ A/ -1.8 mA
$\bar{B}_0-\bar{B}_3$	B Operand Inputs (Active LOW)	1.0/3.0	20 μ A/ -1.8 mA
S_0-S_3	Function Select Inputs	1.0/4.0	20 μ A/ -2.4 mA
M	Mode Control Input	1.0/1.0	20 μ A/ -0.6 mA
C_n	Carry Input	1.0/5.0	20 μ A/ -3.0 mA
$\bar{F}_0-\bar{F}_3$	Function Outputs (Active LOW)	50/33.3	-1 mA/20 mA
A = B	Comparator Output	OC*/33.3	*/20 mA
$\bar{G}$	Carry Generate Output (Active LOW)	50/33.3	-1 mA/20 mA
$\bar{P}$	Carry Propagate Output (Active LOW)	50/33.3	-1 mA/20 mA
$C_n + 4$	Carry Output	50/33.3	-1 mA/20 mA

*OC-Open Collector

Functional Description

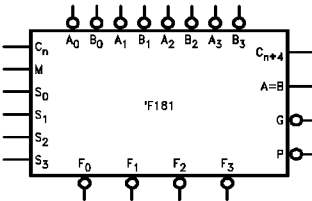
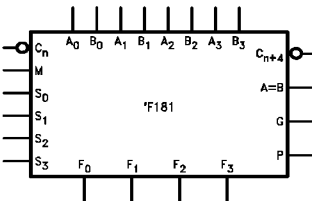
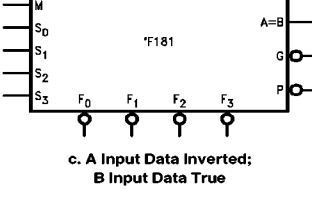
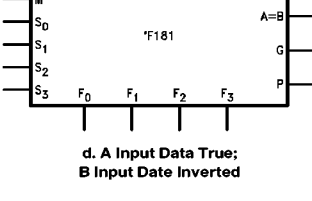
The 'F181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S_0-S_3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on Active HIGH or Active LOW operands. The Function Table lists these operations.

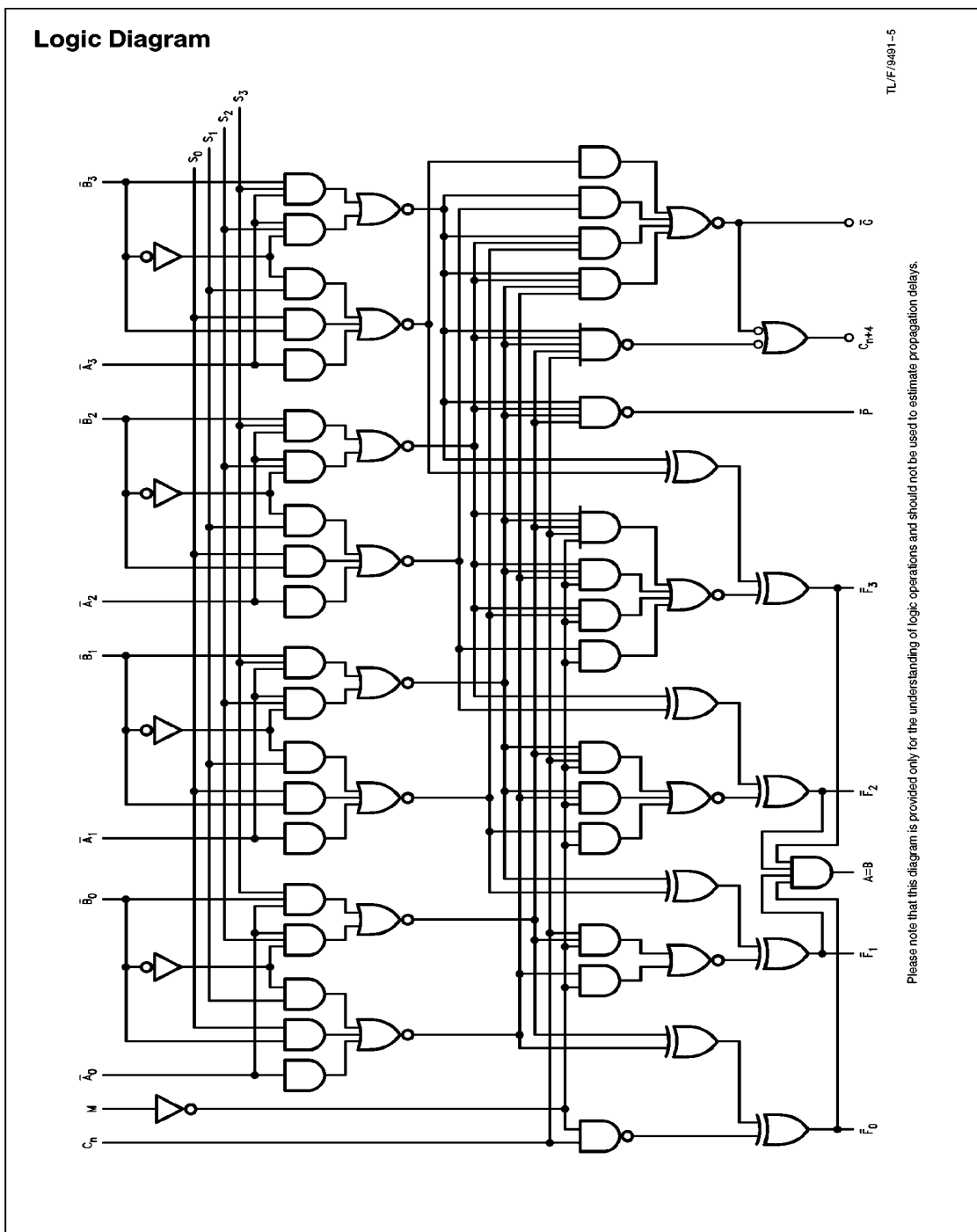
When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the $C_n + 4$ output, or for carry lookahead between packages using the signals $\bar{P}$ (Carry Propagate) and $\bar{G}$ (Carry Generate). In the Add mode, $\bar{P}$ indicates that $\bar{F}$ is 15 or more, while $\bar{G}$ indicates that $\bar{F}$ is 16 or more. In the Subtract mode $\bar{P}$ indicates that $\bar{F}$ is zero or less, while $\bar{G}$ indicates that $\bar{F}$ is less than zero. $\bar{P}$ and $\bar{G}$ are not affected by carry in. When speed requirements are not stringent, the 'F181 can be used in a simple Ripple Carry mode by connecting the Carry output ($C_n + 4$) signal to the Carry input (C_n) of the next unit. For high speed operation the device is used in conjunction with a carry lookahead circuit. One carry lookahead package is required for

each group of four 'F181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four $\bar{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the Subtract mode. The A = B output is open collector and can be wired AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the $C_n + 4$ signal to indicate $A > B$ and $A < B$.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

'F181 Operation Table						
	S ₀	S ₁	S ₂	S ₃	Logic (M=H)	Arithmetic (M=L, C ₀ =Inactive)
 a. All Input Data Inverted	L	L	L	L	$\bar{A}$	A minus 1
	H	L	L	L	$\bar{A} \cdot \bar{B}$	A • B minus 1
	L	H	L	L	$\bar{A} + \bar{B}$	A • B minus 1
	H	H	L	L	Logic "1"	minus 1 (2s comp.)
	L	L	H	L	$\bar{A} + \bar{B}$	A plus (A + B)
	H	L	H	L	$\bar{B}$	A • B plus (A + B)
	L	H	H	L	$\bar{A} \oplus \bar{B}$	A minus B minus 1
	H	H	H	L	$A + \bar{B}$	A + B
	L	L	L	H	$\bar{A} \cdot B$	A plus (A + B)
	H	L	L	H	$A \oplus B$	A plus B
	L	H	L	H	B	A • B plus (A + B)
	H	H	L	H	$A + B$	A + B
	L	L	H	H	Logic "0"	A plus A (2 × A)
	H	L	H	H	$A \cdot \bar{B}$	A plus A • B
	L	H	H	H	$A \cdot B$	A plus A • B
	H	H	H	H	A	A
 b. All Input Data True	L	L	L	L	$\bar{A}$	A
	H	L	L	L	$\bar{A} + \bar{B}$	A + B
	L	H	L	L	$\bar{A} \cdot B$	A + B
	H	H	L	L	Logic "0"	minus 1 (2s comp.)
	L	L	H	L	$\bar{A} \cdot \bar{B}$	A plus (A • B)
	H	L	H	L	$\bar{B}$	A • B plus (A + B)
	L	H	H	L	$A \oplus B$	A minus B minus 1
	H	H	H	L	$A \cdot \bar{B}$	A • B minus 1
	L	L	L	H	$\bar{A} + B$	A plus A • B
	H	L	L	H	$\bar{A} \oplus B$	A plus B
	L	H	L	H	B	A • B plus (A + B)
	H	H	L	H	$A \cdot B$	A • B minus 1
	L	L	H	H	Logic "1"	A plus A (2 × A)
	H	L	H	H	$A + \bar{B}$	A plus (A + B)
	L	H	H	H	$A + B$	A plus (A + B)
	H	H	H	H	A	A minus 1
 c. A Input Data Inverted; B Input Data True	L	L	L	L	$\bar{A}$	A minus 1
	H	L	L	L	$\bar{A} + B$	A • B minus 1
	L	H	L	L	$\bar{A} \cdot \bar{B}$	A • B minus 1
	H	H	L	L	Logic "1"	minus 1 (2s comp.)
	L	L	H	L	$\bar{A} \cdot B$	A plus (A + B)
	H	L	H	L	B	A • B plus (A + B)
	L	H	H	L	$A \oplus B$	A plus B
	H	H	H	L	$A + B$	A + B
	L	L	L	H	$\bar{A} + \bar{B}$	A plus (A + B)
	H	L	L	H	$\bar{A} \oplus \bar{B}$	A minus B minus 1
	L	H	L	H	$\bar{B}$	A • B plus (A + B)
	H	H	L	H	$A + \bar{B}$	A + B
	L	L	H	H	Logic "0"	A plus A (2 × A)
	H	L	H	H	$A \cdot B$	A plus A • B
	L	H	H	H	$A \cdot \bar{B}$	A plus A • B
	H	H	H	H	A	A
 d. A Input Data True; B Input Data Inverted	L	L	L	L	$\bar{A}$	A
	H	L	L	L	$\bar{A} \cdot B$	A + B
	L	H	L	L	$\bar{A} + \bar{B}$	A + B
	H	H	L	L	Logic "0"	minus 1 (2s comp.)
	L	L	H	L	$\bar{A} + B$	A plus A • B
	H	L	H	L	$\bar{B}$	A • B plus (A + B)
	L	H	H	L	$\bar{A} \oplus \bar{B}$	A plus B
	H	H	H	L	$A \cdot B$	A • B minus 1
	L	L	L	H	$\bar{A} \cdot \bar{B}$	A plus A • B
	H	L	L	H	$A \oplus B$	A minus B minus 1
	L	H	L	H	$\bar{B}$	A • B plus (A + B)
	H	H	L	H	$A \cdot \bar{B}$	A • B minus 1
	L	L	H	H	Logic "1"	A plus A (2 × A)
	H	L	H	H	$A + B$	A plus (A + B)
	L	H	H	H	$A + \bar{B}$	A plus (A + B)
	H	H	H	H	A	A minus 1



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	−0.5V to V _{CC}
TRI-STATE® Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

ESD Last Passing Voltage (Min) 4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

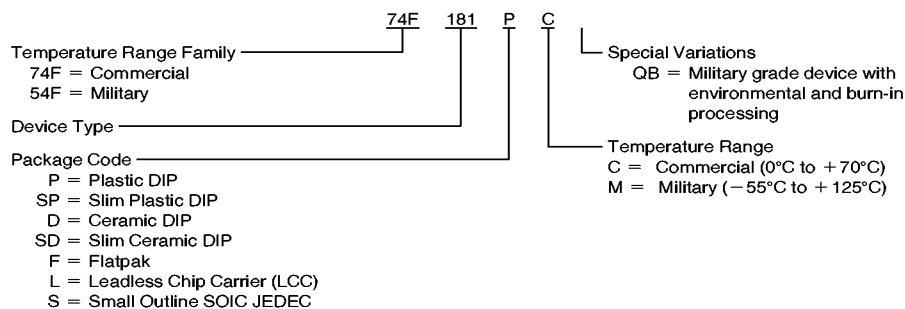
Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC}	2.5 2.5 2.7		V	Min	I _{OH} = −1 mA I _{OH} = −1 mA I _{OH} = −1 mA
V _{OL}	Output LOW Voltage	54F 10% V _{CC} 74F 10% V _{CC}		0.5 0.5	V	Min	I _{OL} = 20 mA I _{OL} = 20 mA
I _{IH}	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V _{IN} = 2.7V
I _{BI}	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V _{OUT} = V _{CC} ($\overline{F}_n, \overline{G}, \overline{P}, C_{n+4}$)
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			−0.6 −1.8 −2.4 −3.0	mA	Max	V _{IN} = 0.5V (M) V _{IN} = 0.5V ($\overline{A}_0, \overline{A}_1, \overline{A}_3, \overline{B}_0, \overline{B}_1, \overline{B}_3$) V _{IN} = 0.5V ($\overline{S}_n, \overline{A}_2, \overline{B}_2$) V _{IN} = 0.5V (C _n)
I _{OS}	Output Short-Circuit Current	−60	−150		mA	Max	V _{OUT} = 0V ($\overline{F}_n, \overline{G}, \overline{P}, C_{n+4}$)
I _{OHC}	Open Collector, Output OFF Leakage Test		250		μA	Min	V _O = V _{CC} (A = B)
I _{CCH}	Power Supply Current		43	65.0	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current		43	65.0	mA	Max	V _O = LOW

AC Electrical Characteristics

Symbol	Parameter		74F			54F		74F		Units
			$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
	Path	Mode	Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay C_n to $C_n + 4$		3.0 3.0	6.4 6.1	8.5 8.0	3.0 3.0	10.0 9.5	3.0 3.0	9.5 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\bar{A}$ or $\bar{B}$ to $C_n + 4$	Sum	5.0 4.0	10.0 9.4	13.0 12.0	5.0 3.5	15.5 16.5	5.0 4.0	14.0 13.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\bar{A}$ or $\bar{B}$ to $C_n + 4$	Dif	5.0 5.0	10.8 10.0	14.0 13.0	5.0 4.0	17.0 15.0	5.0 5.0	15.0 14.0	ns
t_{PLH} t_{PHL}	Propagation Delay C_n to $\bar{F}$	Any	3.0 3.0	6.7 6.5	8.5 8.5	2.5 2.5	16.0 12.0	3.0 3.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\bar{A}$ or $\bar{B}$ or $\bar{G}$	Sum	3.0 3.0	5.7 5.8	7.5 7.5	2.5 2.5	9.0 9.5	3.0 3.0	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\bar{A}$ or $\bar{B}$ to $\bar{G}$	Dif	3.0 3.0	6.5 7.3	8.5 9.5	2.5 2.5	11.5 11.0	3.0 3.0	9.5 10.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\bar{A}$ or $\bar{B}$ to $\bar{P}$	Sum	3.0 3.0	5.0 5.5	7.0 7.5	2.5 3.0	8.5 9.5	3.0 3.0	8.0 8.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\bar{A}$ or $\bar{B}$ to $\bar{P}$	Dif	3.0 4.0	5.8 6.5	7.5 8.5	2.5 3.0	11.0 11.0	3.0 4.0	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\bar{A}_i$ or $\bar{B}_i$ to F_i	Sum	3.0 3.0	7.0 7.2	9.0 10.0	3.0 3.0	14.5 14.5	3.0 3.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\bar{A}_i$ or $\bar{B}_i$ to F_i	Dif	3.0 3.0	8.2 5.0	11.0 11.0	3.0 3.0	17.5 14.5	3.0 3.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation Delay Any $\bar{A}$ or $\bar{B}$ to Any $\bar{F}$	Sum	4.0 4.0	8.0 7.8	10.5 10.0	3.5 4.0	16.5 13.5	4.0 4.0	11.5 11.0	ns
t_{PLH} t_{PHL}	Propagation Delay Any $\bar{A}$ or $\bar{B}$ to Any $\bar{F}$	Dif	4.5 3.5	9.4 9.4	12.0 12.0	3.5 3.0	17.5 14.0	4.5 3.5	13.0 13.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\bar{A}$ or $\bar{B}$ to $\bar{F}$	Logic	4.0 4.0	6.0 6.0	9.0 10.0	3.5 3.0	14.5 15.5	4.0 4.0	10.0 11.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\bar{A}$ or $\bar{B}$ to $A = B$	Dif	11.0 6.0	18.5 9.8	27.0 12.5	8.0 5.5	35.0 21.0	11.0 6.0	29.0 13.5	ns

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



The drawing shows a 28-Lead Ceramic Leadless Chip Carrier (L) with the following dimensions and features:

- TOP VIEW:** Overall width is 0.450 ± 0.008 .
- BOTTOM VIEW:**
 - Lead pitch: 0.015 MIN TYP.
 - Lead width: 0.300 ± 0.005 TYP.
 - Lead angle: $45^\circ \times 0.015 \pm 0.010$.
 - Lead radius: $R 0.011$ TYP.
 - Lead thickness: 0.028 TYP.
 - Lead spacing: 0.022 TYP.
 - Lead height: 0.055 TYP.
 - Lead width: 0.045 TYP.
 - Lead angle: $45^\circ \times 0.040 \pm 0.010$ 3 PLCS.
 - Lead thickness: 0.083 TYP.
 - Lead width: 0.067 TYP.
 - Lead height: 0.055 TYP.
 - Lead width: 0.045 TYP.
 - Lead angle: $45^\circ \times 0.040 \pm 0.010$ 3 PLCS.
 - Lead thickness: 0.083 TYP.
 - Lead width: 0.067 TYP.
 - Lead height: 0.055 TYP.
 - Lead width: 0.045 TYP.
- SIDE VIEW:**
 - Lead height: 0.075 TYP.
 - Lead width: 0.063 TYP.
 - Lead thickness: 0.003 MIN TYP.
 - Lead width: 0.015 MAX TYP.
 - Lead spacing: 0.022 MAX TYP.
 - Lead width: 0.006 MIN TYP.
- DETAIL A:** Shows a cross-section of the lead.

28-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E28A

E28A (REV D)



The drawing illustrates the mechanical specifications of a 24-Lead (0.300" Wide) Ceramic Dual-In-Line Package (SD) in NS Package Number J24F. It includes three views: a top view, a side view, and an end view.

Top View Dimensions:

- Overall width: 1.290 (32.77) MAX
- Lead pitch: 0.025 (0.635) RAD
- Lead width: 0.315 (8.001) MAX GLASS
- Lead spacing: 0.295 (7.493) MAX
- Lead thickness: 0.030-0.055 (0.762-1.397) RAD TYP

Side View Dimensions:

- Package height: 0.180 (4.572) MAX
- Lead height: 0.225 (5.715) MAX
- Lead thickness: 0.018 ±0.003 (0.457 ±0.076) TYP
- Lead width: 0.125 (3.175) MIN
- Lead spacing: 0.100 ±0.010 (2.54 ±0.254) TYP
- Lead thickness: 0.060 ±0.005 (1.524 ±0.127) TYP
- Lead width: 0.020-0.070 (0.508-1.778)
- Lead thickness: 0.290-0.320 (7.366-8.128)
- Lead angle: 95° ±5°
- Lead width: 0.008-0.012 (0.203-0.305) TYP
- Lead spacing: 0.310-0.410 (7.874-10.41)

End View Dimensions:

- Package width: 0.095 MAX BOTH ENDS (2.413)
- Lead angle: 86°-94° TYP

Material and Finish:

- GLASS SEALANT

Package Identification:

- 24-Lead (0.300" Wide) Ceramic Dual-In-Line Package (SD)
- NS Package Number J24F

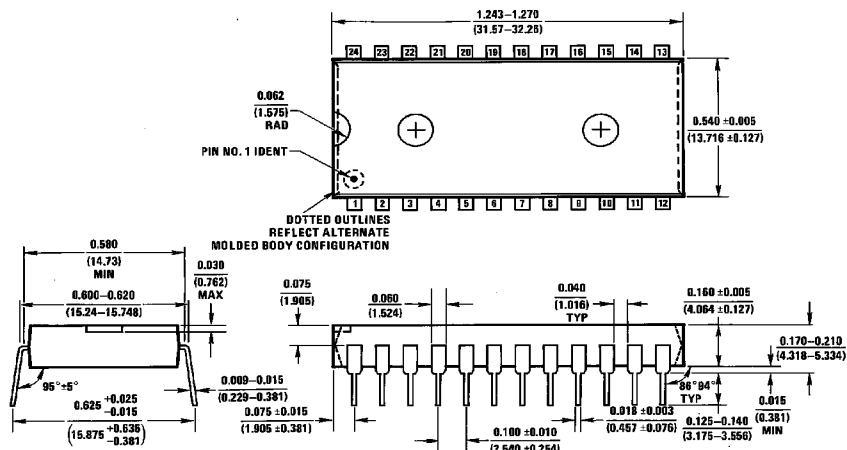
Revision:

- J24F (REV 6)

**24-Lead (0.300" Wide) Ceramic Dual-In-Line Package (SD)
NS Package Number J24F**

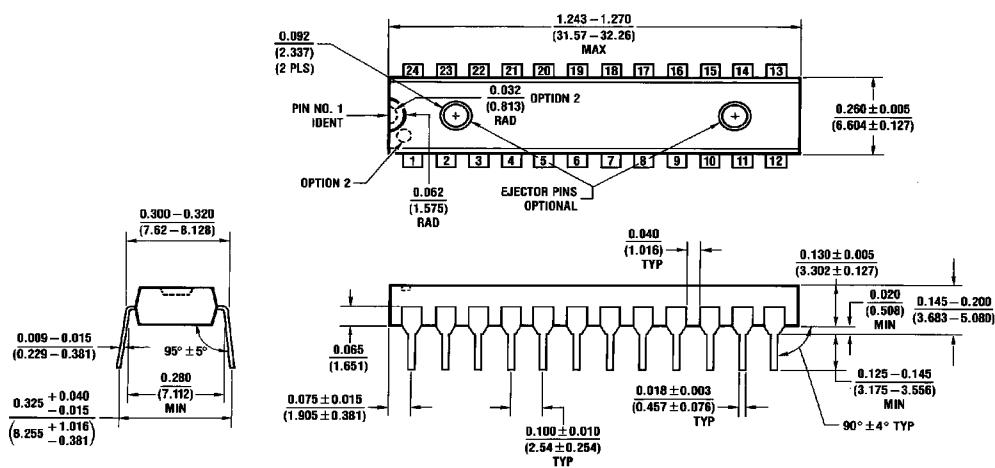


Physical Dimensions inches (millimeters) (Continued)



24-Lead (0.600" Wide) Molded Dual-In-Line Package (P)
NS Package Number N24A

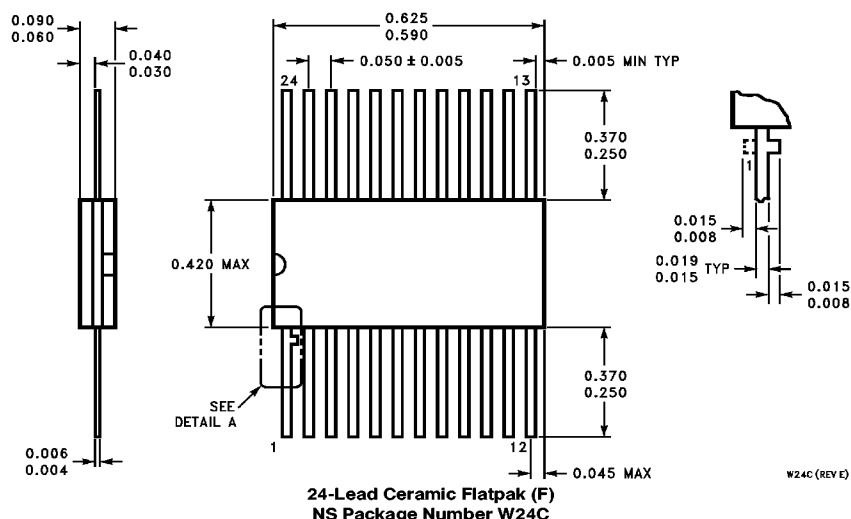
N24A (REV E)



24-Lead (0.300" Wide) Molded Dual-In-Line Package (SP)
NS Package Number N24C

N24C (REV F)

Physical Dimensions inches (millimeters) (Continued)



LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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