

16-bit inverting buffer/driver (3-State)
[查询 74ABT16240ADL-T 供应商](#)

74ABT16240A
74ABTH16240A

FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- 74ABTH16240A incorporates bus hold data inputs which eliminate the need for external pull up resistors to hold unused inputs
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16240A is a high-performance BiCMOS device which combines low static and dynamic power dissipation with high speed and high output drive.

This device is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$), each controlling four of the 3-State outputs.

Two options are available, 74ABT16240A which does not have the bus hold feature and 74ABTH16240A which incorporates the bus hold feature.

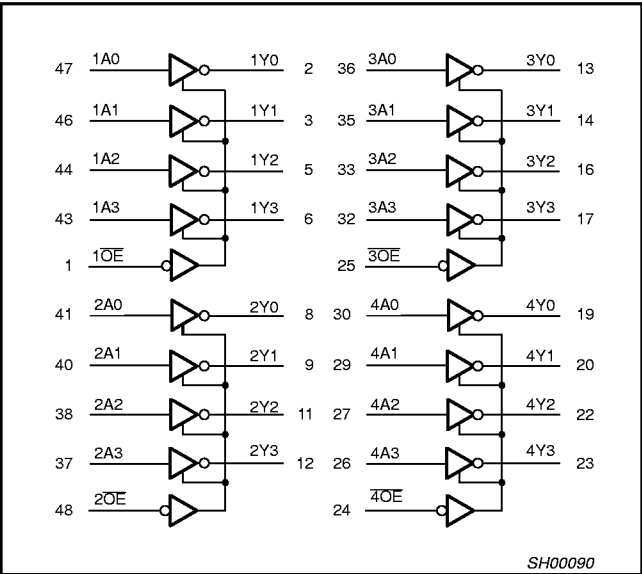
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}C$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	$C_L = 50pF$; $V_{CC} =$	2.0 1.8	ns
C_{IN}	Input capacitance n $\overline{OE}$	$V_I = 0V$ or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; $V_O = 0V$ or	6	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; $V_{CC} =$	500	μA
I_{CCL}		Outputs low; $V_{CC} = 5.5V$	9	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	-40°C to +85°C	74ABT16240A DL	BT16240A DL	SOT370-1
48-Pin Plastic TSSOP Type II	-40°C to +85°C	74ABT16240A DGG	BT16240A DGG	SOT362-1
48-Pin Plastic SSOP Type III	-40°C to +85°C	74ABTH16240A DL	BH16240A DL	SOT370-1
48-Pin Plastic TSSOP Type II	-40°C to +85°C	74ABTH16240A DGG	BH16240A DGG	SOT362-1

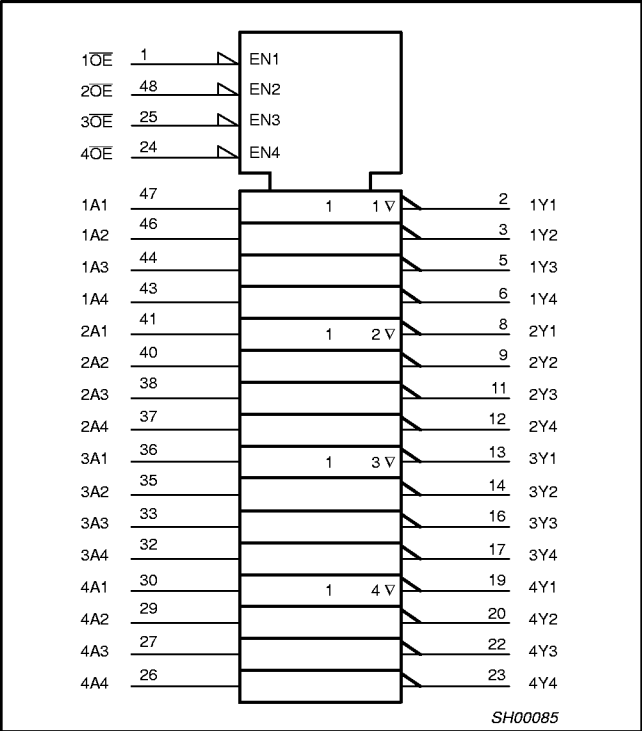
LOGIC SYMBOL



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LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

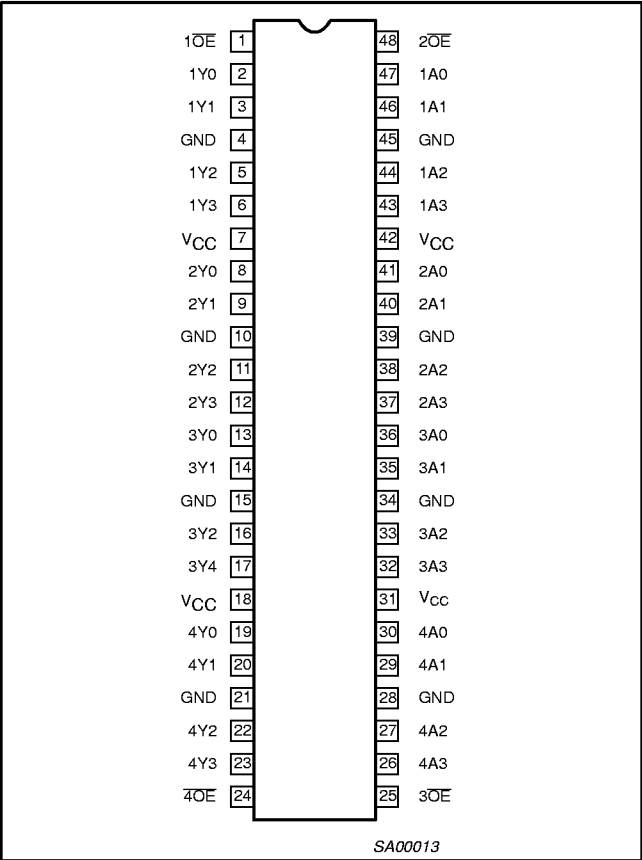
PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0-1A3 2A0-2A3 3A0-3A3 4A0-4A3	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Y0-1Y3 2Y0-2Y3 3Y0-3Y3 4Y0-4Y3	Data outputs
1, 48, 25, 24	1OE, 2OE, 3OE, 4OE	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	VCC	Positive supply voltage

FUNCTION TABLE

Inputs		Outputs
nOE	nAx	nYx
L	L	H
L	H	L
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

PIN CONFIGURATION



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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage ³		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage ³	Output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle $\leq 50\%$; $f \geq 1\text{kHz}$		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = -18mA			-0.9	-1.2		-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 4.5V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}		2.5	2.9		2.5		V
		V _{CC} = 5.0V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}		3.0	3.4		3.0		V
		V _{CC} = 4.5V; I _{OH} = -32mA; V _I = V _{IL} or V _{IH}		2.0	2.4		2.0		V
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}			0.42	0.55		0.55	V
I _I	Input leakage current	V _{CC} = 5.5V; V _I = GND or 5.5V			±0.01	±1.0		±1.0	µA
I _I	Input leakage current 74ABTH16240A	V _{CC} = 5.5V; V _I = V _{CC} or GND	Control pins		±0.01	±1		±1	µA
		V _{CC} = 5.5V; V _I = V _{CC}	Data pins		0.01	1		1	µA
		V _{CC} = 5.5V; V _I = 0			-2	-3		-5	µA
I _{HOLD}	Bus Hold current A inputs 74ABTH16240A ³	V _{CC} = 4.5V; V _I = 0.8V		50			50		µA
		V _{CC} = 4.5V; V _I = 2.0V		-75			-75		
		V _{CC} = 5.5V; V _I = 0 to 5.5V		±500					
I _{OFF}	Power-off leakage current	V _{CC} = 0.0V; V _O or V _I ≤ 4.5V			±5.0	±100		±100	µA
I _{PU} /I _{PD}	Power-up/down 3-State output current	V _{CC} = 2.0V; V _O = 0.5V; V _I = GND or V _{CC} ; V _{OE} = V _{CC}			±5.0	±50		±50	µA
I _{OZH}	3-State output High current	V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH}			1.0	10		10	µA
I _{OZL}	3-State output Low current	V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH}			-1.0	-10		-10	µA
I _{CEX}	Output high leakage current	V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}			1.0	50		50	µA
I _O	Output current ¹	V _{CC} = 5.5V; V _O = 2.5V		-50	-70	-180	-50	-180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}			0.5	1.0		1.0	mA
I _{CCL}		V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}			8	19		19	mA
I _{CCZ}		V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}			0.5	1.0		1.0	mA
ΔI _{CC}	Additional supply current per input pin ² 74ABT16240A	Outputs enabled, one input at 3.4V, other inputs at V _{CC} or GND; V _{CC} = 5.5V			10	200		200	µA
ΔI _{CC}	Additional supply current per input pin ² 74ABTH16240A	Outputs enabled, one input at 3.4V, other inputs at V _{CC} or GND; V _{CC} = 5.5V			0.2	1.0		1.0	mA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = -40°C to +85°C.

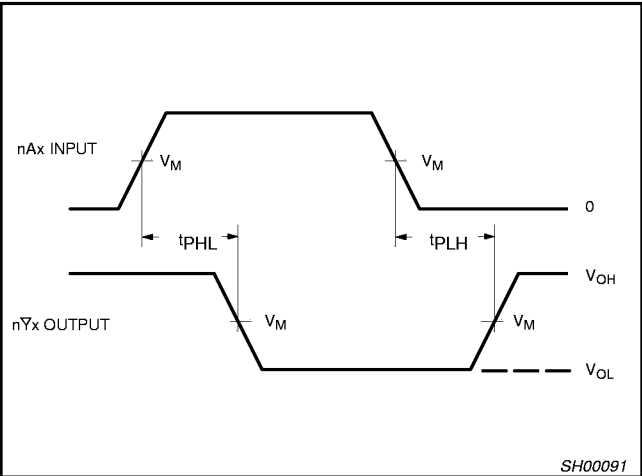
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = −40°C to +85°C V _{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay nAx to nYx	1	1.0 1.0	2.0 1.5	3.0 3.0	1.0 1.0	3.7 3.5	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	1.2 1.2	2.4 2.3	3.3 3.2	1.2 1.0	4.2 4.2	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	2	1.3 1.3	2.7 2.5	4.1 3.6	1.6 1.4	4.7 4.1	ns

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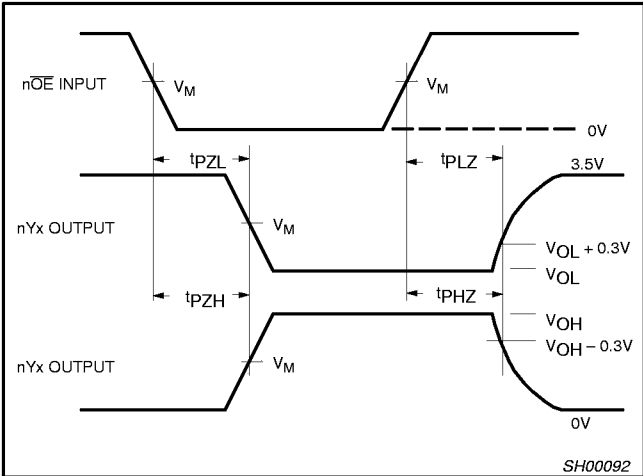
74ABT16240A
74ABTH16240A

AC WAVEFORMS

$V_M = 1.5V$, $V_{IN} = GND$ to $2.7V$



Waveform 1. Input (nAx) to Output (nYx) Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS

Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	7V
All other	open

Input Pulse Definition

$V_M = 1.5V$

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT16	3.0V	1MHz	500ns	2.5ns	2.5ns

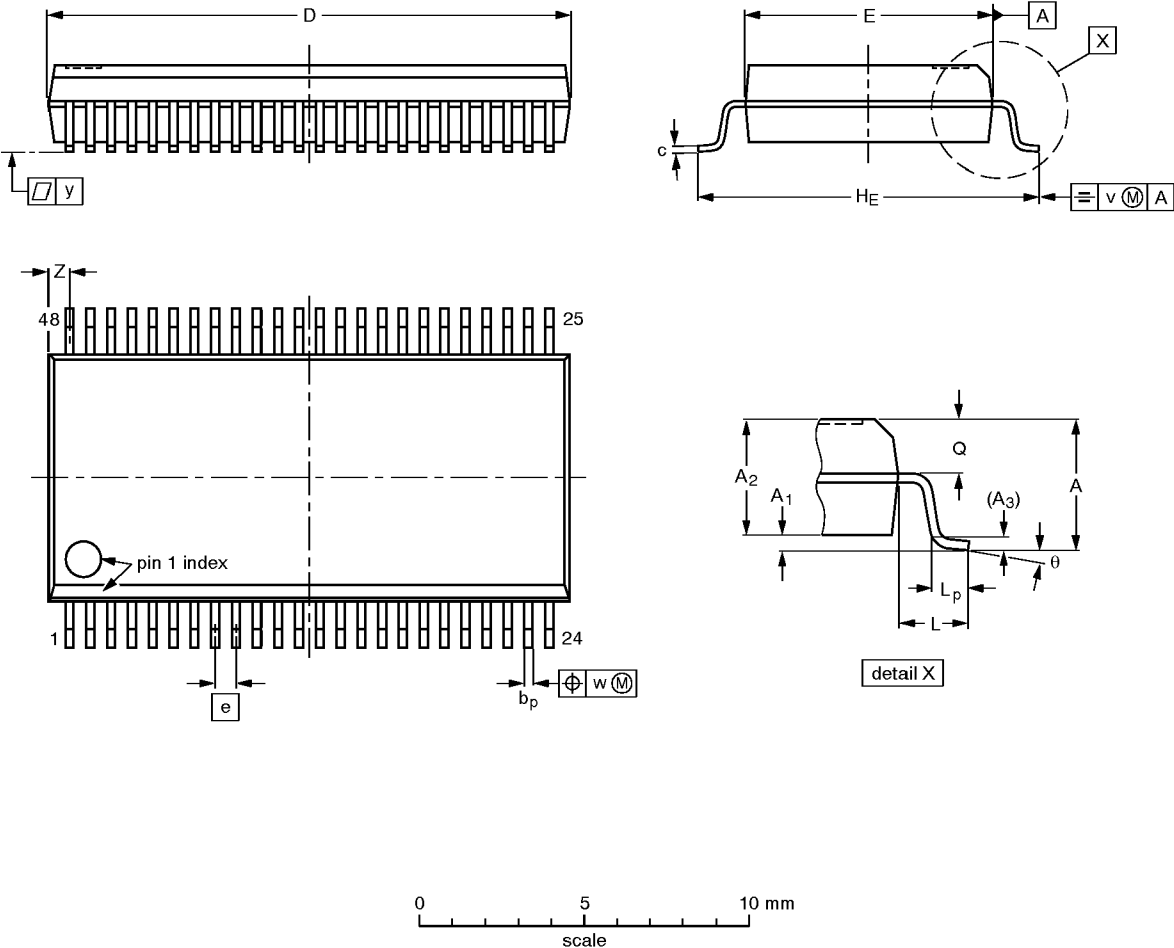
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SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				93-11-02 95-02-04

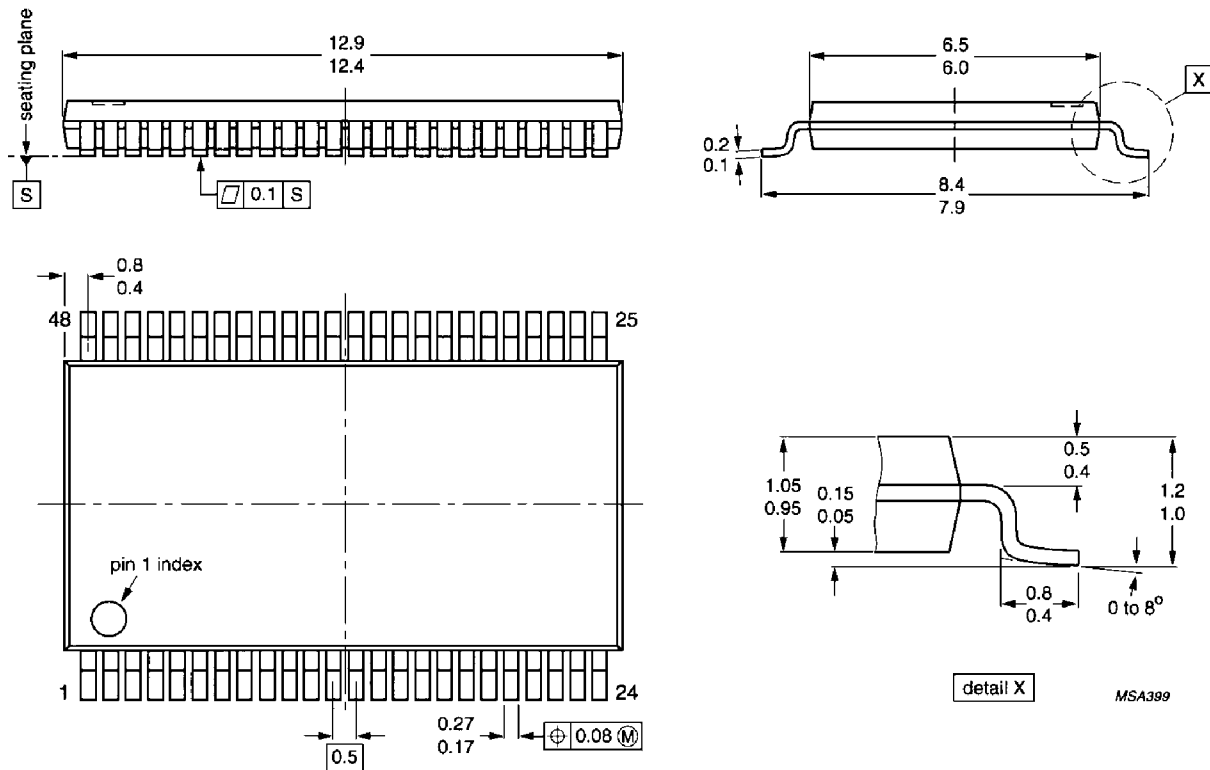
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74ABT16240A
74ABTH16240A

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm

SOT362-1



Dimensions in mm.