REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28						
REV STATUS OF SHEETS				REV																
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Thomas M. Hess

CHECKED BY
Thomas M. Hess

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
96-01-28

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, 16-BIT MICROPROCESSOR, RADIATION HARDENED, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-95722
A	67268	

SHEET 1 OF 28

DESC FORM 193
JUL 94

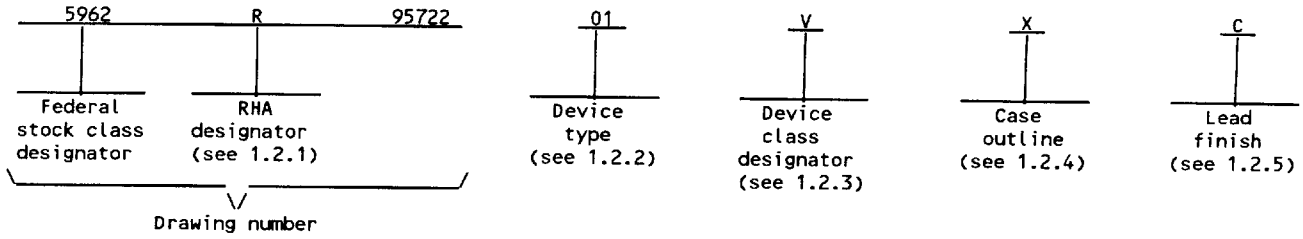
5962-E260-95

DISTRIBUTION STATEMENT A. Approved for public release: distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	80C86RH	16-Bit CMOS microprocessor radiation hardened

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	CDIP2-T40	40	Dual-in-line package
X	See figure 1	42	Flatpack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{CC})	+7.0 V dc
Input voltage range	V_{SS} -0.3 V dc to V_{DD} +0.3 V dc
Storage temperature range (T_{STG})	-65°C to +150°C
Junction temperature (T_J)	+175°C
Lead temperature (soldering 10 seconds) (T_S)	+300 °C
Thermal resistance junction-to-case (θ_{JC}):	
Case outline Q	8.6°C/W
Case outline X	9.7°C/W
Thermal resistance junction-to-ambient (θ_{JA}):	
Case outline Q	40°C/W
Case outline X	72.1°C/W
Maximum package power dissipation at T_A = +125°C (P_D) 2/	
Case outline Q	1.25 W
Case outline X	0.69 W

1.4 Recommended operating conditions.

Operating supply voltage range (V_{DD})	4.75 V dc to +5.25 V dc
Operating temperature range (T_A)	-35°C to +125°C
Input low voltage range (V_{IL})	0 V dc to +0.8 V dc
Input high voltage range (V_{IH})	3.5 V dc to V_{DD}
Clock input low voltage range (V_{ILC})	0 V dc to +0.8 V dc
CLK and MS/MX input high range (V_{ILH})	V_{DD} - 0.8 V dc to V_{DD}
Radiation features:	
Total dose	> 100k Rads(SI)
Transient upset	> 10^8 RAD (SI)/sec 3/
Single event upset	6 MeV/(mg/cm^2) 3/
Single event latchup	75 MeV/(mg/cm^2) 3/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ If device power exceeds package dissipation capability provide heat sinking or derate linearly (the derating is based on θ_{JA}) at a rate of 25 mW/°C for case Q and 13.9 mW/°C for case X.
3/ Guaranteed by process or design, but not tested.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Switching waveforms. The switching waveforms shall be as specified in figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified in figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-I-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-35°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TTL high level output voltage	V_{OH1}	V_{DD} = 4.75 V, I_O = -2.5 mA V_{IN} = 0 V or V_{DD}	1,2,3	All	3.0		V
Output high voltage (CMOS)	V_{OH2}	V_{DD} = 4.75 V, I_{OH} = -100 µA V_{IN} = 0 V or V_{DD}	1,2,3	All	V_{DD}-0.4		V
Output low voltage	V_{OL}	V_{IN} = 0 V or V_{DD} V_{DD} = 4.75 V, I_{OL} = +2.5 mA	1,2,3	All		0.4	V
Input leakage current	I_{IL} I_{IH}	V_{DD} = 5.25 V, V_{IN} = GND or V_{DD} DIP pins: 17-19, 21-23, 33 2/	1,2,3	All	-1.0	+1.0	µA
Output leakage current	I_{OZL} I_{OZH}	2/ V_{DD} = 5.25 V, V_{OUT} = 0 V or V_{DD} DIP pins: 2-16,26-29,32,34-39	1,2,3	All	-10	+10	µA
Input current bus hold high	I_{BHH}	Pins: 2-16,26-32,34-39 2/ V_{IN} = 3.0 V, V_{DD} = 4.75 V and 5.25 V 3/	1,2,3	All	-600	-40	µA
Input current bus hold low	I_{BHL}	Pins: 2-16, 34-39 V_{IN} = 0.8 V, V_{DD} = 4.75 V and 5.25 V 4/ 2/	1,2,3	All	40	600	µA
Standby power supply current	I_{DDSB}	I_O = 0 mA V_{IN} = V_{DD} or V_{SS} V_{DD} = 5.25 V 5/	1,2,3	All		500	µA
Operating power supply current	I_{DDOP}	V_{DD} = 5.25 V, V_{IN} = V_{DD} or V_{SS} I_O = 0 mA , f= 1 MHz	1,2,3	All		12	mA/MHz
Functional tests		See 4.4.1b V_{DD} = 4.75 V and 5.25 V f = 1 Mhz, V_{IN} = V_{DD} or V_{SS}	7,8	All			
Noise immunity Functional tests		See 4.4.1b 6/ V_{DD} = 4.75 V and 5.25 V V_{IN} = 0.8 V or 3.5V	7,8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-35°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input capacitance	C_{IN}	See 4.4.1c f = 1 MHz All measurements are referenced device GND. V_{DD} = open	4	All		15	pF
Output capacitance	C_{OUT}		4	All		15	pF
I/O capacitance	$C_{I/O}$		4	All		20	pF
CLK cycle period	t_{CLCL}	2/ V_{DD} = 4.75 V and 5.25 V	9,10,11	All	200		ns
CLK low time	t_{CLCH}	2/ V_{DD} = 4.75 V	9,10,11	All	118		ns
CLK high time	t_{CHCL}	2/ V_{DD} = 4.75 V and 5.25 V	9,10,11	All	69		ns
Data in setup time	t_{DVCL}	2/ V_{DD} = 4.75 V	9,10,11	All	30		ns
Data in hold time	t_{CLDX1}	2/ V_{DD} = 4.75 V	9,10,11	All	10		ns
Ready setup time into device	t_{RYHCH}	2/ V_{DD} = 4.75 V	9,10,11	All	113		ns
Ready hold time into device	t_{CHRYX}	2/ V_{DD} = 4.75 V	9,10,11	All	30		ns
Ready inactive to CLK	t_{RYLCL}	2/ 8/ V_{DD} = 4.75 V	9,10,11	All	-8		ns
Hold setup time	t_{HVCH}	2/ V_{DD} = 4.75 V	9,10,11	All	35		ns
INTR, NMI, $\overline{\text{TEST}}$ setup time	t_{INVCH}	2/ V_{DD} = 4.75 V	9,10,11	All	30		ns
MINIMUM MODE TIMING RESPONSE (C_L = 100 pF)							
Address valid delay	t_{CLAV}	V_{DD} = 4.75 V	9,10,11	All	10	110	ns
ALE width	t_{LHLL}	V_{DD} = 4.75 V	9,10,11	All	t_{CLCH}-20		ns
ALE active delay	t_{CLLH}	V_{DD} = 4.75 V	9,10,11	All		80	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-35°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
MINIMUM MODE TIMING RESPONSE - CONTINUED.							
ALE inactive delay	t_{CHLL}	V_{DD} = 4.75 V	9,10,11	All		85	ns
Address hold time to ALE inactive	t_{LLAX}	V_{DD} = 4.75 V	9,10,11	All	t_{CLCH}-10		ns
Control active delay 1	t_{CVCTV}	V_{DD} = 4.75 V	9,10,11	All	10	110	ns
Control active delay 2	t_{CHCTV}	V_{DD} = 4.75 V	9,10,11	All	10	110	ns
Control inactive delay	t_{CVCTX}	V_{DD} = 4.75 V	9,10,11	All	10	110	ns
$\overline{RD}$ active delay	t_{CLRL}	V_{DD} = 4.75 V	9,10,11	All	10	165	ns
$\overline{RD}$ inactive delay	t_{CLRH}	V_{DD} = 4.75 V	9,10,11	All	10	50	ns
$\overline{RD}$ inactive to next address active	t_{RHAV}	V_{DD} = 4.75 V	9,10,11	All	t_{CLCH}-15		ns
HLDA valid delay	t_{CLHAV}	V_{DD} = 4.75 V	9,10,11	All	10	160	ns
$\overline{RD}$ width	t_{RLRH}	V_{DD} = 4.75 V	9,10,11	All	$2t_{CLCL}$-75		ns
$\overline{WR}$ width	t_{WLWH}	V_{DD} = 4.75 V	9,10,11	All	2tCLCH-60		ns
Address valid to ALE low	t_{AVLL}	V_{DD} = 4.75 V	9,10,11	All	t_{CLCH}-60		ns
Output rise time	t_{OLOH}	From 0.8 V to 2.0 V V_{DD} = 4.75 V	9,10,11	All		20	ns
Output fall time	t_{OHOL}	From 2.0 V to 0.8 V V_{DD} = 4.75 V	9,10,11	All		20	ns
TIMING REQUIREMENT							
CLK cycle period	t_{CLCL}	VDD = 5.25 V V_{DD} = 4.75 V	9,10,11	All	200		ns
CLK low time	t_{CLCH}	V_{DD} = 4.75 V	9,10,11	All	118		ns
CLK high time	t_{CHCL}	V_{DD} = 5.25 V V_{DD} = 4.75 V	9,10,11	All	69		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-35°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data in setup time	t_{DVCL}	V_{DD} = 4.75 V	9,10,11	All	30		ns
Data in hold time	t_{CLDX1}	V_{DD} = 4.75 V	9,10,11	All	10		ns
RDY setup time into device	t_{RYHCH}	V_{DD} = 4.75 V	9,10,11	All	113		ns
RDY hold time into device	t_{CHRYX}	V_{DD} = 4.75 V	9,10,11	All	30		ns
Ready inactive to CLK	t_{RYLCL}	8/ V_{DD} = 4.75 V	9,10,11	All	-8		ns
INTR, NMI, test setup time	t_{INVCH}	V_{DD} = 4.75 V	9,10,11	All	30		ns
$\overline{RQ}/\overline{GT}$ setup time	t_{GVCH}	V_{DD} = 4.75 V	9,10,11	All	20		ns
$\overline{RQ}$ hold time into device	t_{CHGX}	9/ V_{DD} = 4.75 V	9,10,11	All	40	t_{CHCL} +10	ns
CLK rise time	t_{CH1CH2}	10/ Min and Max mode from 1.0 V to 3.5 V V_{DD} = 4.75 V and 5.25 V	9,10,11	All		15	ns
CLK fall time	t_{CL2CL1}	10/ Min and Max mode from 3.5 V to 1.0 V V_{DD} = 4.75 V and 5.25 V	9,10,11	All		15	ns
Input rise time	t_{ILIH}	Min and Max mode from 0.8 V to 2.0 V 10/ V_{DD} = 4.75 V and 5.25 V	9,10,11	All		25	ns
Input fall time	t_{IHIL}	Min and Max mode from 2.0 V to 0.8 V V_{DD} = 4.75 V and 5.25 V 10/	9,10,11	All		25	ns
MAXIMUM MODE TIMING RESPONSE (C_L = 100 pF)							
Address float delay	t_{CLAZ}	V_{DD} = 4.5 V and 5.25 V 10/ 11/ Max mode only	9,10,11	All	tCLAX	80	ns
Status float delay	t_{CHSZ}	V_{DD} = 4.5 V and 5.25 V Max mode only, 10/, 11/	9,10,11	All		80	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-35°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data hold time after WR	t_{WHDX}	10/ V_{DD} = 4.75 V and 5.25 V minimum mode	9,10,11	All	t_{CLCL}-30		ns
Data hold time	t_{CLDX2}	10/ Min/Max mode V_{DD} = 4.75 V and 5.25 V	9,10,11	All	10		ns
Address hold time	t_{CLAX}	Min/Max mode 10/ V_{DD} = 4.75 V and 5.25 V	9,10,11	All	10		ns
Data valid delay	t_{CLDV}	Min/Max mode 10/ V_{DD} = 4.75 V and 5.25 V	9,10,11	All	10	110	ns
Address float to read active	t_{AZRL}	Min/Max mode 10/ V_{DD} = 4.75 V and 5.25 V 11/	9,10,11	All	0		ns
MINIMUM COMPLEXITY SYSTEM TIMING.							
Ready active to status passive	t_{RYHSH}	8/ 12/ V_{DD} = 4.75 V	9,10,11	All		110	ns
Status active delay	t_{CHSV}	V_{DD} = 4.75 V	9,10,11	All	10	110	ns
Status inactive delay	t_{CLSH}	12/ V_{DD} = 4.75 V	9,10,11	All	10	130	ns
Address valid delay	t_{CLAV}	V_{DD} = 4.75 V	9,10,11	All	10	110	ns
$\overline{RD}$ active delay	t_{CLRL}	V_{DD} = 4.75 V	9,10,11	All	10	165	ns
$\overline{RD}$ inactive delay	t_{CLRH}	V_{DD} = 4.75 V	9,10,11	All	10	150	ns
$\overline{RD}$ inactive to next address	t_{RHAV}	V_{DD} = 4.75 V	9,10,11	All	t_{CLCL}-45		ns
$\overline{GT}$ active delay	t_{CLGL}	V_{DD} = 4.75 V	9,10,11	All	0	85	ns
$\overline{GT}$ inactive delay	t_{CLGH}	V_{DD} = 4.75 V	9,10,11	All	0	85	ns
$\overline{RD}$ width	t_{RLRH}	V_{DD} = 4.75 V	9,10,11	All	$2t_{CLCL}$-75		ns
Output rise time	t_{OLOH}	From 0.8 V to 2.0 V V_{DD} = 4.75 V	9,10,11	All		20	ns
Output fall time	t_{OHOL}	From 2.0 V to 0.8 V V_{DD} = 4.75 V	9,10,11	All		20	ns

See footnotes at end of table.

1/ Devices supplied to this drawing will meet all levels M, D, L, R of irradiation. However, this device is only tested at the R level. Pre and post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ Pin numbers are for 40 pin dip. Use equivalent functions for 42 pin flat package.

3/ I_{BHH} should be measured after raising V_{IN} to V_{DD} and then lowering to valid input high level of 3.0 V on the following pins; 2-16, 26-32, 34-39.

4/ I_{BHL} should be measured after raising V_{IN} to GND and then raising to valid input low level of 0.3 V on the following: 2-16, 34-39.

5/ I_{DDSB} tested during clock high time after HALT instruction execution.

6/ CLK and MN/MX input high = VDD - 0.8 V.

7/ Setup requirement for asynchronous signal to guarantee recognition at next clock.

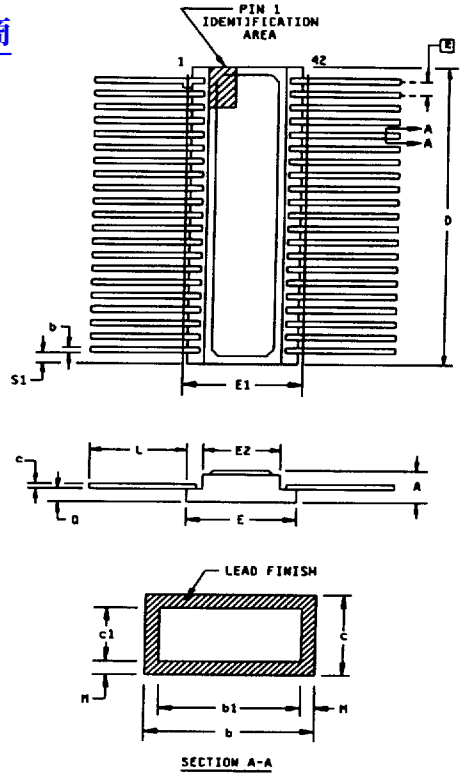
8/ Applies only to T2 state (8 ns into T3).

9/ The device actively pulls the RQ/GT pin to a logic one on the following clock low time.

10/ The parametersare controlled via design or process parameters and are not directly tested, These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

11/ Output drivers disabled. Bus hold circuitry still active.

12/ Status lines return to their inactive (logic one) state after CLK goes low and READY goes high.



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	-	2.54	-	0.100
b	0.43	0.64	0.017	0.025
b1	0.43	0.58	0.017	-.023
c	0.18	0.33	0.007	0.013
c1	0.18	0.25	0.007	0.010
D	26.54	27.31	1.045	1.075
E	16.00	16.51	0.630	0.650
E1	-	17.27	-	0.680
E2	13.46	13.97	0.530	0.550
e	1.27 BSC		0.050 BSC	
L	8.13	8.89	0.320	0.350
Q	1.14	1.65	0.045	0.065
S1	0	-	0	-
M	-	0.04	-	0.0015
N	42		42	

Figure 1. Case outline

Device type	01		
Case outline	Q		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	21	RESET
2	AD14	22	READY
3	AD13	23	$\overline{TEST}$
4	AD12	24	QS1 ($\overline{INTA}$)
5	AD11	25	QS0 (ALE)
6	AD10	26	$\overline{S0}$ ($\overline{DEN}$)
7	AD9	27	$\overline{S1}$ (DT/$\overline{R}$)
8	AD8	28	$\overline{S2}$ (M/$\overline{IO}$)
9	AD7	29	$\overline{LOCK}$ ($\overline{WR}$)
10	AD6	30	$\overline{RQ}$/GT1 (HLDA)
11	AD5	31	$\overline{RQ}$/GT0 (HOLD)
12	AD4	32	$\overline{RD}$
13	AD3	33	MN/$\overline{MX}$
14	AD2	34	$\overline{BHE}$/S7
15	AD1	35	A19/S6
16	AD0	36	A18/S5
17	NMI	37	A17/S4
18	INTR	38	AD16/S3
19	CLK	39	AD15
20	GND	40	V_{DD}

FIGURE 2. Terminal connection.

Case X			
Terminal Number	Terminal symbol	Terminal number	Terminal symbol
1	GND	22	RESET
2	AD14	23	READY
3	AD13	24	$\overline{TEST}$
4	AD12	25	QS1 ($\overline{INTA}$)
5	AD11	26	QS0 (ALE)
6	AD10	27	$\overline{S0}$ ($\overline{DEN}$)
7	AD9	28	$\overline{S1}$ (DT/$\overline{R}$)
8	AD8	29	$\overline{S2}$ (M/$\overline{IO}$)
9	AD7	30	$\overline{LOCK}$ ($\overline{WR}$)
10	AD6	31	$\overline{RQ}$/$\overline{GT1}$ (HLDA)
11	AD5	32	$\overline{RQ}$/$\overline{GT0}$ (HOLD)
12	AD4	33	$\overline{RD}$
13	AD3	34	MN/$\overline{MX}$
14	AD2	35	$\overline{BHE}$/S7
15	AD1	36	A19/S6
16	AD0	37	A18/S5
17	NC	38	A17/S4
18	NMI	39	AD16/S3
19	INTR	40	NC
20	CLK	41	VAD15
21	GND	42	V_{DD}

FIGURE 2. Terminal connections. - Continued

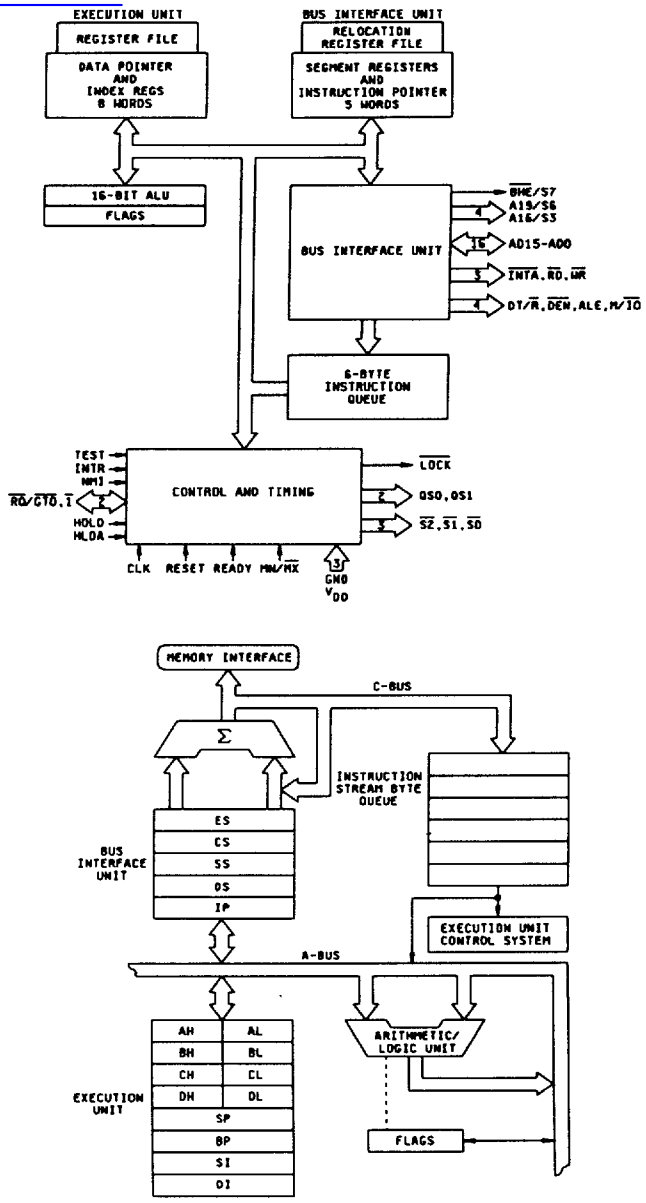
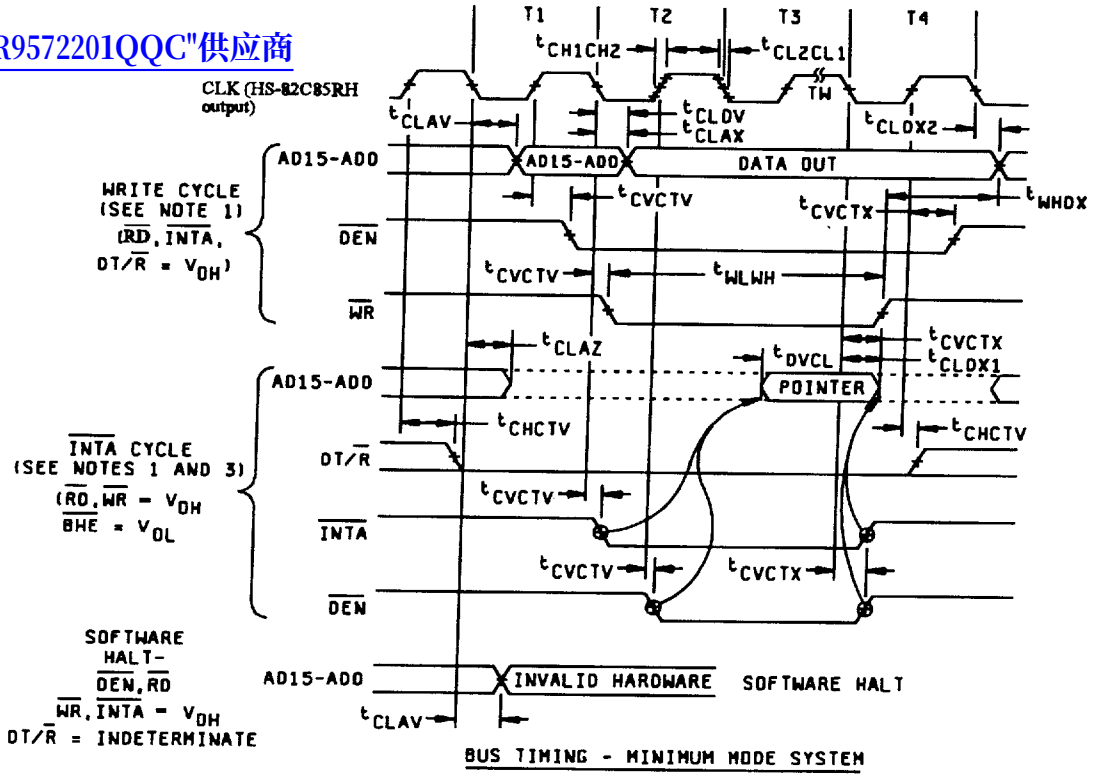
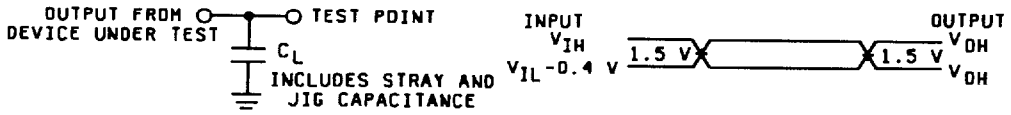


FIGURE 3. Functional diagram.



BUS TIMING - MINIMUM MODE SYSTEM

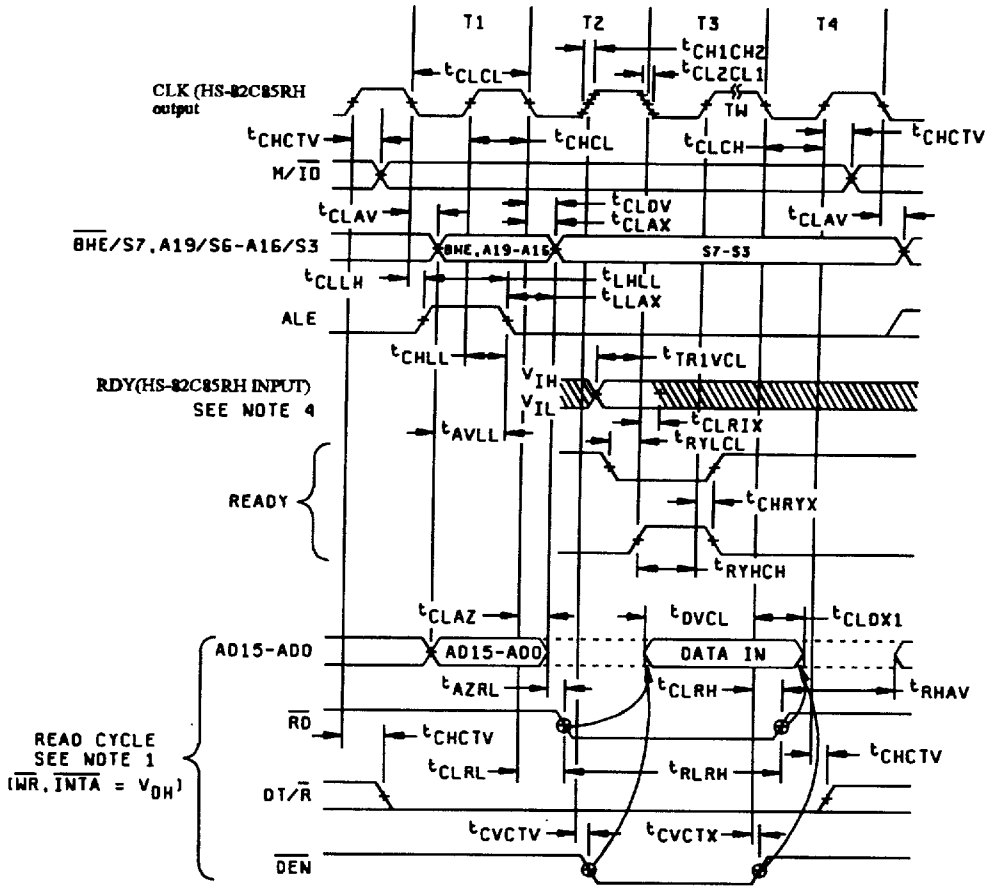


AC TEST CIRCUIT

AC TESTING INPUT, OUTPUT WAVEFORM

Notes:
1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T2, T3, TW to determine if TW machine states are to be inserted.
3. Two INTA kcycles run back-to-back. The device local ADDR/DATA bus is inactive during both INTA cycles. Control signals are shown for the second INTA CYCLE.
4. All timing measuremtns are made at 1.5 V unless otherwise noted.
5. All inputs signals (other than CLK) must be switched between $V_{IL(MAX)}$ - 0.4 V and $V_{IH(MIN)}$ + 0.4 V. CLK must switch between 0.4 V and V_{DD} - 0.4 V. t_r and t_f must be less than or equal to 15 ns. CLK, t_r and t_f must be less than or equal to 10 ns.

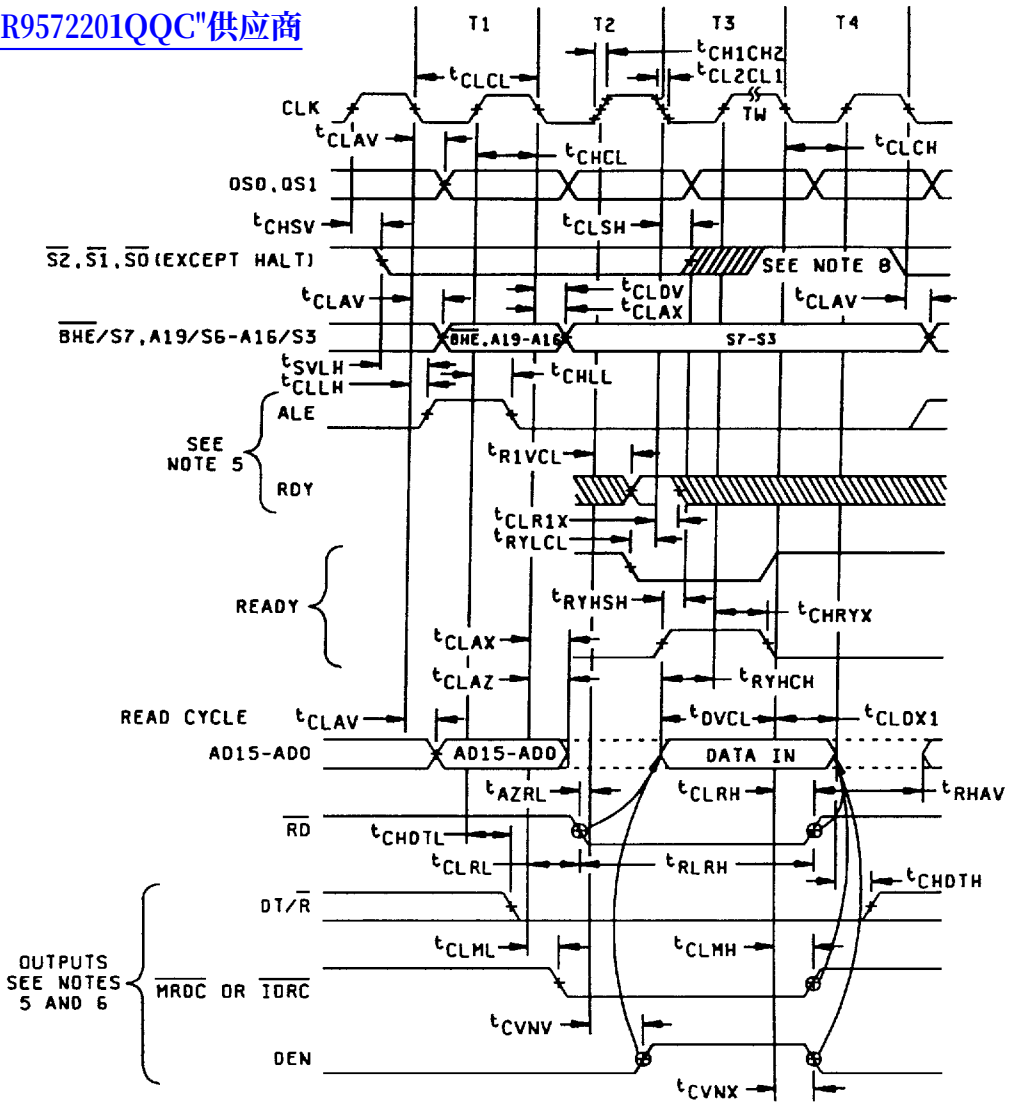
Figure 4. Timing waveform and load circuit.



BUS TIMING - MINIMUM MODE SYSTEM

NOTES:
1. Unless otherwise specified, all signals switch between V_{OH} and V_{OL}.
2. RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted.
3. Two INTA cycles run back-to-back. The device local ADDR/DATA bus is inactive during both INTA cycles. Control signals are shown for the second INTA cycle.
4. Signals at HS-82C85RH are shown for reference only.
5. Unless otherwise specified, all timing measurements are made at 1.5 V.

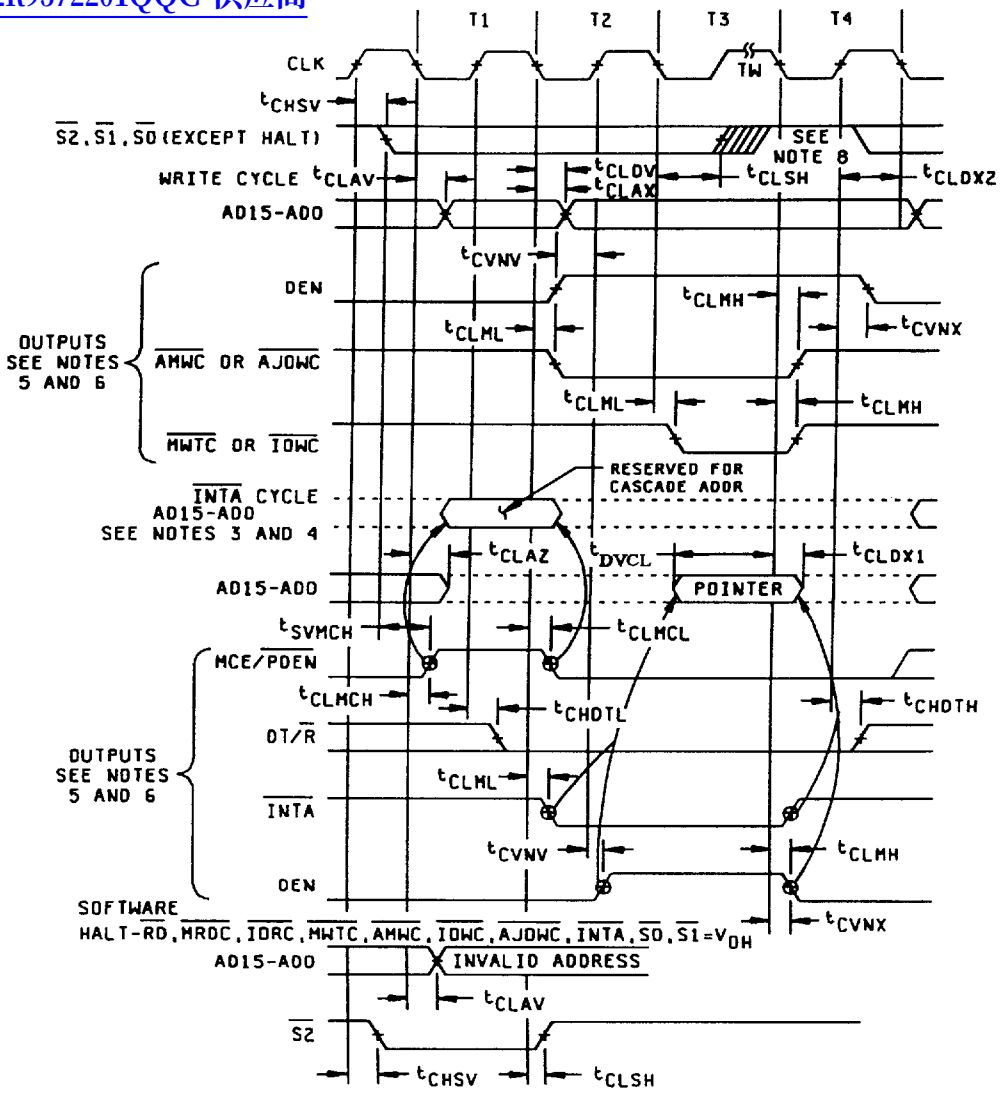
FIGURE 4. Timing waveform and load circuit - Continued.



BUS TIMING - MAXIMUM MODE SYSTEM

Notes:
1. Unless otherwise specified, all signals switch between V_{OH} and V_{OL}.
2. RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted.
3. Cascade address is valid between first and second INTA cycle.
4. Two INTA cycles run back to back. The device local addr/DATA bus is inactive during both $\overline{\text{INTA}}$ cycles. Control for pointer address is shown for the second INTA cycle.
5. Signals at 82C85 and 82C88 are shown for reference only.
6. The issuance of the device command and control signals ($\overline{\text{MRDC}}$, $\overline{\text{MWTC}}$, $\overline{\text{AMWC}}$, $\overline{\text{IORC}}$, $\overline{\text{IOWC}}$, $\overline{\text{AIOWC}}$, $\overline{\text{INTA}}$ and DEN) lags the active high of 82C88 CEN.
7. Unless otherwise specified, all timing measurements are made at 1.5 V.
8. Status inactive in state just prior to T4.

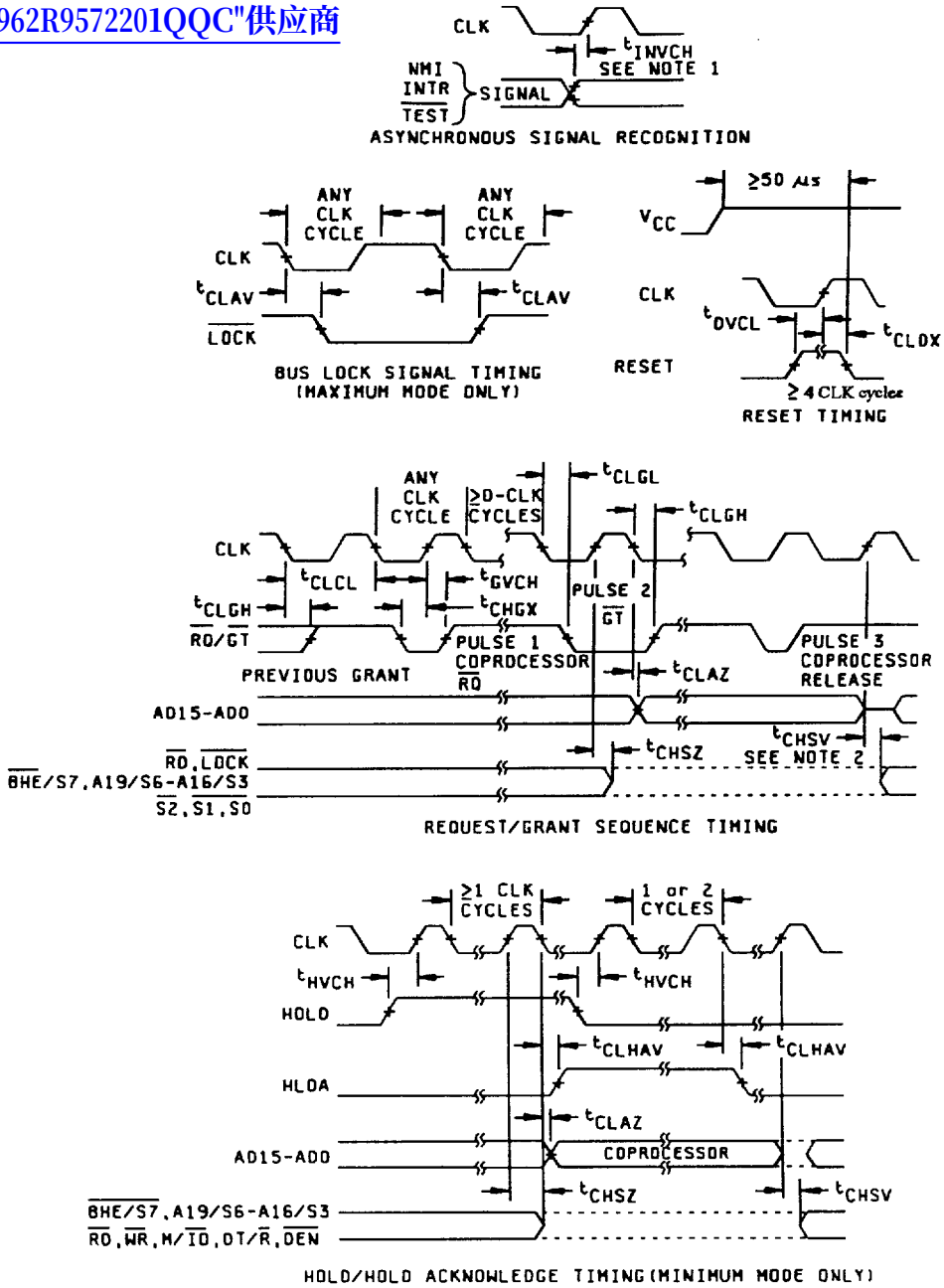
FIGURE 4. Timing waveform and load circuit - Continued.



BUS TIMING - MINIMUM MODE SYSTEM

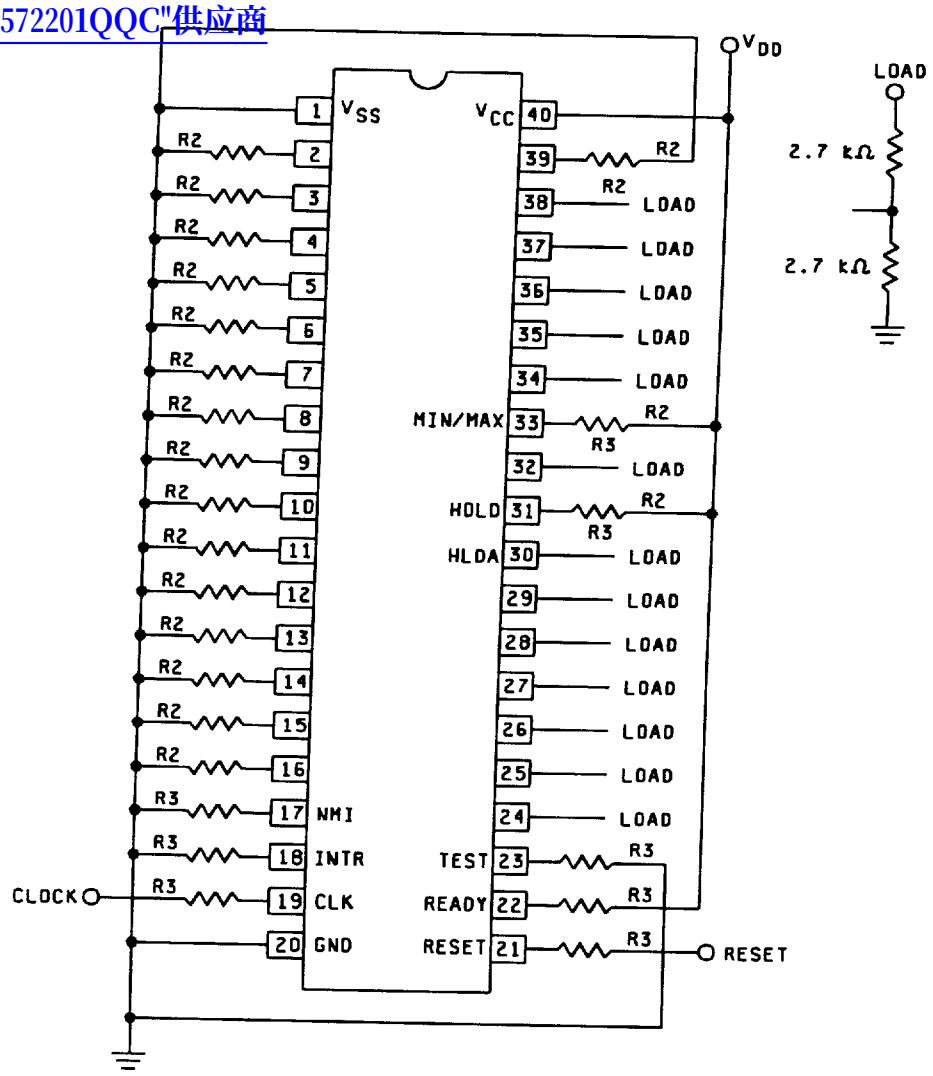
Notes:
1. Unless otherwise specified, all signals switch between V_{OH} and V_{OL}.
2. RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted.
3. Cascade address is valid between first and second INTA cycle.
4. Two INTA cycles run back to back. The device local addr/DATA bus is inactive during both $\overline{\text{INTA}}$ cycles. Control for pointer address is shown for the second INTA cycle.
5. Signals at 82C85 and 82C88 are shown for reference only.
6. The issuance of the device command and control signals ($\overline{\text{MRDC}}$, $\overline{\text{MWTC}}$, $\overline{\text{AMWC}}$, $\overline{\text{IORC}}$, $\overline{\text{IOWC}}$, $\overline{\text{AIOWC}}$, $\overline{\text{INTA}}$ and DEN) lags the active high of 82C88 CEN.
7. Unless otherwise specified, all timing measurements are made at 1.5 V.
8. Status inactive in state just prior to T4.

FIGURE 4. Timing waveform and load circuit - Continued.



Notes:
1. Setup requirements for asynchronous signals only to guarantee recognition at next CLK.
2. The coprocessor may not drive the busses outside the region shown without risking contention.

FIGURE 4. Timing waveform and load circuit - Continued.



NOTES:
1. V_{DD} = 5.0 V ± 0.5 V.
2. R2 = 3.3 kΩ. R3 = 47 kΩ.
3. Pins tied to GND: 1-18, 20, 23, 39.
   Pins tied to V_{DD}: 22, 31, 33,40.
   Pins with loads: 24-29, 30, 32, 34-38.
   Pins brought out 19 (clock), 21 (reset).
4. Clock and reset should be brought out separately so they can be toggled before irradiation.

FIGURE 5. Radiation exposure circuit.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535, or as modified in the device manufacturers approved Quality Management (QM) plan.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 or as modified in the device manufacturers QM plan including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

C. Subgroup 4 (C_{IN}, C_{OUT}, and $C_{I/O}$ measurements) shall be measured only for the initial qualification and after process or design changes which may affect capacitance, A minimum sample size of 5 devices with zero rejects shall be reuired.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1,2,3,7,8,9, 10,11 1/	1,2,3,7,8, 9,10,11 1/	1,2,3,7,8 9,10,11 2/ 3/
Group A test requirements (see 4.4)	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8 9,10,11	1,2,3,4,7,8 9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,7,8,9 10,11	1,2,3,7,8,9 10,11	1,2,3,7,8,9 10,11
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1and 7.
2/ PDA applies to subgroups 1,7 and deltas.
3/ Delta limits as specified in Tabel IIB herein shall be required when specified and the delta values shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in delta parameters (+25°).

Parameter	Symbol	Delta limits
Standby power supply current	I_{DDSB}	±100 µA
Output leakage current	I_{OZL}, I_{OZH}	±2 µA
Input leakage current	I_{IH}, I_{IL}	±200 nA
Low level output voltage	V_{OL}	±80 mV
TTL high level output voltage	V_{OH1}	±600 mV
CMOS high level output voltage	V_{OH2}	±150 mV

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-I-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). SEP testing shall be required on class V devices (See 1.4). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^6 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331 and as follows:

Pin symbol	Type	Description
AD15-AD0	I/O	ADDRESS DATA BUS: These lines constitute the time multiplexed memory/IO address (T1) and data (T2, T3, TW, T4) bus. A0 is analogous to BHE for the lower byte of the data bus, pins D7-D0. It is LOW during T1 when a byte is to be transferred on the lower portion of the bus in memory or I/O opoerations. Eight bit oriented devices tied to the lower half would normally use AD0 to condition chip select functions (see BHE). These lines are active HIGH and are held at high impedance to the last valid logic level during interrupt acknowledge and local bus "hold acknowledge" or "grant sequence".
A19/S6 A18/S5 A17/S4 A16/S3	O	ADDRESS/STATUS: During T1, these are the four most significant address lines for memory operations. During I/O operations these lines are low. During memory and I/O operations, status information is available on these lines during T2, T3, TW, T4 ⊛ S6 is always zero. The status of the interrupt enable FLAG bit (S5) is updated at the beginning of each clock cycle. S4 and S3 are encoded. This information indicates which segment register is presently being used for data accessing. These lines are held at high impedance to the last valid logic level during local bus "hold acknowledge" or "grant sequence".

S4	S3	Characteristics
0	0	Extra data
0	1	Stack
1	0	Code or none
1	1	Data

Pin symbol	Type	Description - Continued.
$\overline{BHE}$/S7	O	BUS HIGH ENABLE/STATUS: During T1 the bus high enable signal ($\overline{BHE}$) should be used to enable data onto the most significant half of the data bus, pins D15-D8. Eight bit oriented devices tied to the upper half of the bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is LOW during T1 for read, write, and interrupt acknowledge cycles when a bytes is to be transferred on the high portion of the bus. The S7 status information is available during T2, T3, and T4. The signal is active LOW, and is held at high impedance to the last valid logic level during interrupt acknowledge and local bus "hold acknowledge" or "grant sequence"; it is LOW during T1 for the first interrupt acknowledge cycle.

$\overline{BHE}$	A0	Characteristics
0	0	Whole word
0	1	Upper byte from/to odd address
1	0	Lower byte from/to odd address
1	1	None

$\overline{RD}$	O	READ: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the M/IO or S2 pin. This signal is used to read devices which reside on the device local bus. RD is active LOW during T2, T3, and TW of any read cycle, and is guaranteed to remain HIGH in T2 until the device local bus has floated. This line is held at a high impedance logic one state during "hold acknowledge" or "grant sequence".
READY	I	READY: Is the acknowledgment from the addressed memory or I/O device that will complete the data transfer. The RDY signal from memory or I/O is synchronized by the 82C85 clock generator to form READY. This signal is active HIGH. The device READY input is not synchronized. Correct operation is not guaranteed if the setup and hold times are not met.
INTR	I	INTERRUPT REQUEST: Is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. If so, an interrupt service routine is called via an interrupt vector lookup table located in system memory. INTR is internally synchronized and it can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.
$\overline{TEST}$	I	TEST: Input is examined by the "Wait" instruction. If the $\overline{TEST}$ input is LOW execution continues, otherwise the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
NMI	I	NON-MASKABLE INTERRUPT: Is an edge triggered input which causes a type 2 interrupt. An interrupt service routine is called via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	I	RESET: Causes the processor to immediately terminate its present activity. The signal must change from LOW to HIGH and remain active HIGH for at least four clock cycles. It restarts execution, as described in the instruction set description, when RESET returns LOW. RESET is internally synchronized.
CLK	I	CLOCK: Provides the basic timing for the processor and bus controller. It is asymmetric with a 33 percent duty cycle to provide optimized internal timing.
V_{DD}		V_{DD}: +5 V power supply pin. A 0.1 µF capacitor between pin 20 and pin 40 is recommended for decoupling.
GND		GND: Ground. Note: Both must be connected. A 0.1 µF capacitor between pin 1 and pin 20 is recommended for decoupling.
MN/$\overline{MX}$	I	MINIMUM/MAXIMUM: Indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

The following pin descriptions are for the 80C86RH in Min mode (ie MN/$\overline{MX}$ = V_{DD}. Only the pin functions which are unique to the minimum mode are described below.

Pin symbol | Type | Description - Continued.

Pin symbol	Type	Description - Continued.
M/$\overline{IO}$	O	STATUS LINE: Logically equivalent to $\overline{S2}$ in the maximum mode. It is used to distinguish a memory access from an I/O access. M/IO becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (M = HIGH, I/O = LOW). M/IO is held to a high impedance logic zero during local bus "hold acknowledge".
$\overline{WR}$	O	WRITE: Indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/IO signal. WR is active for T2, T3, and TW of any write cycle. It is active LOW, and is held to high impedance logic one during local bus "hold acknowledge".
$\overline{INTA}$	O	INTERRUPT ACKNOWLEDGE: Is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T2, T3, and TW of each interrupt acknowledge cycle. Note that INTA is never floated.
ALE	O	ADDRESS LATCH ENABLE: Is provided by the processor to latch the address into the 82C82 address latch. It is a HIGH pulse active during clock LOW of T1 of any bus cycle. Note that ALE is never floated.
DT/$\overline{R}$	O	DATA TRANSMIT/RECEIVE: Is needed in a minimum system that desires to use a data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/$\overline{R}$ is equivalent to S1 in maximum mode, and its timing is the same as for M/IO (T = HIGH, R = LOW). DT/$\overline{R}$ is held to a high impedance logic one during local bus "hold acknowledge".
$\overline{DEN}$	O	DATA ENABLE: Provided as an output enable for a bus transceiver in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access and for INTA cycles. For a read or INTA cycle it is active from the middle of T2 until the middle of T4, while for a write cycle it is active from the beginning of T2 until the middle of T4 . $\overline{DEN}$ is held to a high impedance logic one during local bus "hold acknowledge".
HOLD	I	HOLD: Indicates that another master is requesting a local bus "hold". To be a acknowledged, HOLD must be active HIGH. The processor receiving the "hold" will issue a "hold acknowledge" (HLDA) in the middle of a T4 or T1 clock cycle. Simultaneously with the issuance of HLDA, the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will lower HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines.
HLDA	O	

HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time.

The following pin functions are for the device system in maximum mode (ie. Min/MX = GND). Only the pin functions which are unique to maximum mode are described below.

$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	O	STATUS: Is active during T4, T1, and T2 and is returned to the passive state (1,1,1) during T3 or during TW when READY is HIGH. This status is used by the 82C88 bus controller to generate all memory and I/O access control signals. Any change by S2, S1, or S0 during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 or TW is used to indicate the end of a 8 μs cycle. These status lines are encoded.

These signals are held at a high impedance logic one state during "grant sequence".

S2	S1	$\overline{S0}$	Characteristics
0	0	0	Interrupt acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1	0	0	Code access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive

Pin symbol	Type	Description - Continued.
$\overline{RQ}/GT0$ $\overline{RQ}/GT1$	I/O	REQUEST/GRANT: Pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bi-directional with RQ/GT0 having higher priority that RQ/GT1. RQ/GT has an internal pull-up bus hold device so it may be left unconnected. The request/grant sequence is as follows (see RQ/GT sequence timing). 1. A pulse of 1 CLK wide from another local bus master indicates a local bus request ("hold") to the device (pulse 1). 2. During a T4 or T1 clock cycle, a pulse 1 CLK wide from the device to the requesting master (pulse 2) indicates that the device has allowed the bus to float and that it will enter the "grant sequence" state at next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "grant sequence". 3. A pulse 1 CLK wide from the requesting master indicates to the device (pulse 3) that the "hold" request is about to end and that the device can reclaim the local bus at the next CLK. The CPU then enters T4 (or T1 if no bus cycles pending). Each master-master exchange of the local bus is a sequence of 3 pulses. There must be one idle CLK cycle after each bus exchange. Pulses are active low. If the request is made while the CPU is performing a memory cycle, it will release the local bus during T4 of the cycle when all the following conditions are met: 1. Request occurs on or before T2. 2. Current cycle is not the low byte of a word (on an odd address). 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently executing. If the local bus is idle when the request is made the two possible events will follow: 1. Local bus will be released during the next cycle. 2. A memory cycle will start within three clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.
$\overline{LOCK}$	O	LOCK: Output indicates that other system bus masters are not to gain control of the system bus while LOCK is active LOW. The LOCK signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and is held at a HIGH impedance logic one state during "grant sequence". In MAX mode, LOCK is automatically generated during T2 of the first INTA cycle and removed during T2 of the second INTA cycle.
QS1,QS0	O	QUEUE STATUS: The queue status is valid during the CLK cycle after which the queue operation is performed. QS1 and QS2 provide status to allow external tracking of the internal device instruction queue. Note that QS1, QS0 never become high impedance. QS1 QS0 0 0 No operation 0 1 First byte of Op code from queue 1 0 Empty the queue 1 1 Subsequent byte from queue

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and aDDepted by DESC-EC.

6.8 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latchup (SEP).