

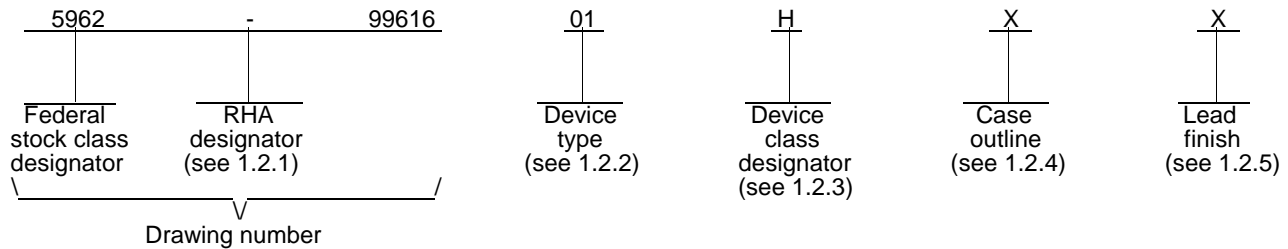
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PMIC N/A					PREPARED BY Gary Zahn					DEFENSE SUPPLY CENTER COLUMBUS POST OFFICE BOX 3990 COLUMBUS, OHIO 43216-5000 http://www.dsccl.dla.mil								
STANDARD MICROCIRCUIT DRAWING					CHECKED BY Michael C. Jones													
THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A					APPROVED BY Raymond Monnin					MICROCIRCUIT, HYBRID, DIGITAL-LINEAR, 14-BIT, DUAL CHANNEL, ANALOG TO DIGITAL CONVERTER								
					DRAWING APPROVAL DATE 01-02-02													
										REVISION LEVEL					SIZE A		CAGE CODE 67268	
										SHEET 1 OF 11								

1. SCOPE

查询"5962-9961601HXA"供应商

1.1 Scope. This drawing documents five product assurance classes, class D (lowest reliability), class E, (exceptions), class G (lowered high reliability), class H (high reliability), and class K, (highest reliability) and a choice of case outlines and lead finishes which are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	AD10465BZ	Dual channel, 14-bit, 65 MSPS, MCM, analog to digital converter

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device performance documentation</u>
D, E, G, H, or K	Certification and qualification to MIL-PRF-38534

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	68	Leaded ceramic chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Positive supply voltage (V_{CC})	0 V dc to +7.0 V dc
Digital positive supply voltage (DV_{CC})	0 V dc to +7.0 V dc
Negative supply voltage (V_{EE})	0 V dc to -7.0 V dc
Analog input voltage	-7.0 V dc to +7.0 V dc
Analog input current	-10 mA to +10 mA
Digital input voltage (ENCODE)	0 V dc to +7.0 V dc
ENCODE, ENCODE differential voltage	4 V dc
Digital output current	-10 mA to +10 mA
Gain and offset adjust voltage range	$-V_{EE}$ to $+V_{CC}$
Digital input voltage range	+0.5 V to $-V_{EE}$
Power dissipation (P_D)	3.8 W
Thermal resistance junction-to-case (θ_{JC})	2.22°C/W
Thermal resistance junction-to-ambient (θ_{JA})	24.3°C/W
Junction temperature (T_J)	+175°C
Storage temperature	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-99616
		REVISION LEVEL	SHEET 2

1.4 Recommended operating conditions.

[查询"5962-9961601HXA"供应商](#)

Positive supply voltage (AV _{CC})	+4.85 V dc to +5.25 V dc
Digital positive supply voltage (DV _{CC})	+3.14 V dc to +3.47 V dc
Negative supply voltage (AV _{EE})	-5.25 V dc to -4.75 V dc
Case operating temperature range (T _C)	-40°C to +85°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. Therefore, the tests and inspections herein may not be performed for the applicable device class (see MIL-PRF-38534). Furthermore, the manufacturer may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-99616
		REVISION LEVEL	SHEET 3

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein. [查询 5962-99616-1HXA"供应商](#)

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked in MIL-HDBK-103 and QML-38534.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-99616
		REVISION LEVEL	SHEET 4

TABLE I. Electrical performance characteristics.

[查询"5962-9961601HXA"供应商](#)

Test	Symbol	Conditions <u>1</u> / -40°C ≤ T _C ≤ +85°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Offset error	OFF _{ERROR}		1,2,3	01	-2.2	+2.2	%FS
Offset error channel match	OFF _{ECM}		1,2,3	01	-1.0	+1.0	%FS
Gain error	AV _{ERROR}	<u>2</u> /	1	01	-3	+1	%FS
			2,3		-5	+5	
Gain error channel match	AV _{ECM}		1	01	-1.5	+1.5	%FS
			2		-3.0	+3.0	
			3		-5.0	+5.0	
Analog input resistance	AR _{IN1}	<u>3</u> /	1,2,3	01	99	101	Ω
	AR _{IN2}				198	202	
	AR _{IN3}				396	404	
ENCODE input (differential input voltage)	V _{IN}	<u>3</u> / <u>4</u> /	1,2,3	01	0.4		Vp-p
Supply currents	I _{CC} TOTAL		1,2,3	01		403	mA
Digital output voltage (logic "1" voltage)	V _{OH}	DV _{CC} = +3.3 V <u>5</u> /	1,2,3	01	2.5		V
Digital output voltage (logic "0" voltage)	V _{OL}	DV _{CC} = +3.3 V <u>5</u> /	1,2,3	01		0.5	V
Input capacitance	C _{IN}	T _A = +25°C <u>3</u> / <u>6</u> /	4	01		7.0	pF
ENCODE pulse width high	ENC _{HI}	<u>3</u> /	4,5,6	01	6.2	9.2	ns
ENCODE pulse width low	ENC _{LO}	<u>3</u> /	4,5,6	01	6.2	9.2	ns
Aperture delay matching	t _{ADM}	T _A = +25°C <u>3</u> /	4	01		500	ps
Maximum conversion rate	CNV _{MAX}	<u>7</u> /	4,5,6	01	65		MSPS

See footnotes at end of table.

**STANDARD
MICROCIRCUIT DRAWING**

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

SIZE
A

REVISION LEVEL

5962-99616

SHEET
5

TABLE I. Electrical performance characteristics - Continued.

[查询"5962-9961601HXA"供应商](#)

Test	Symbol	Conditions <u>1/</u> -40°C ≤ T _C ≤ +85°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Spurious free dynamic range <u>8/</u>	SFDR	Analog input at 9.9 MHz	4	01	73		dBFS
			5,6		70		
		Analog input at 19.5 MHz	4		72		
			5,6		70		
		Analog input at 32.1 MHz	4		62		
			5,6		60		
Signal-to-noise ratio <u>9/</u>	SNR	Analog input at 9.9 MHz	4	01	69		dBFS
			5,6		68		
		Analog input at 19.5 MHz	4		68		
			5,6		67		
		Analog input at 32.1 MHz	4,5,6		67		
Signal-to-noise and distortion <u>10/</u>	SINAD	Analog input at 9.9 MHz	4,5,6	01	67.5		dB
		Analog input at 19.5 MHz	4,5,6		65		
		Analog input at 32.1 MHz	4		60		
			5,6		58		
Two tone intermodulation distortion rejection <u>11/</u>	IMD	f _{IN} = 10 MHz and 11 MHz, f1 and f2 are -7 dB	4	01	78		dBFS
			5,6		78		
		f _{IN} = 31 MHz and 32 MHz, f1 and f2 are -7 dB	4		68		
			5,6		60		

See footnotes at end of table.

**STANDARD
MICROCIRCUIT DRAWING**

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

SIZE
A

REVISION LEVEL

5962-99616

SHEET

6

TABLE I. Electrical performance characteristics - Continued.

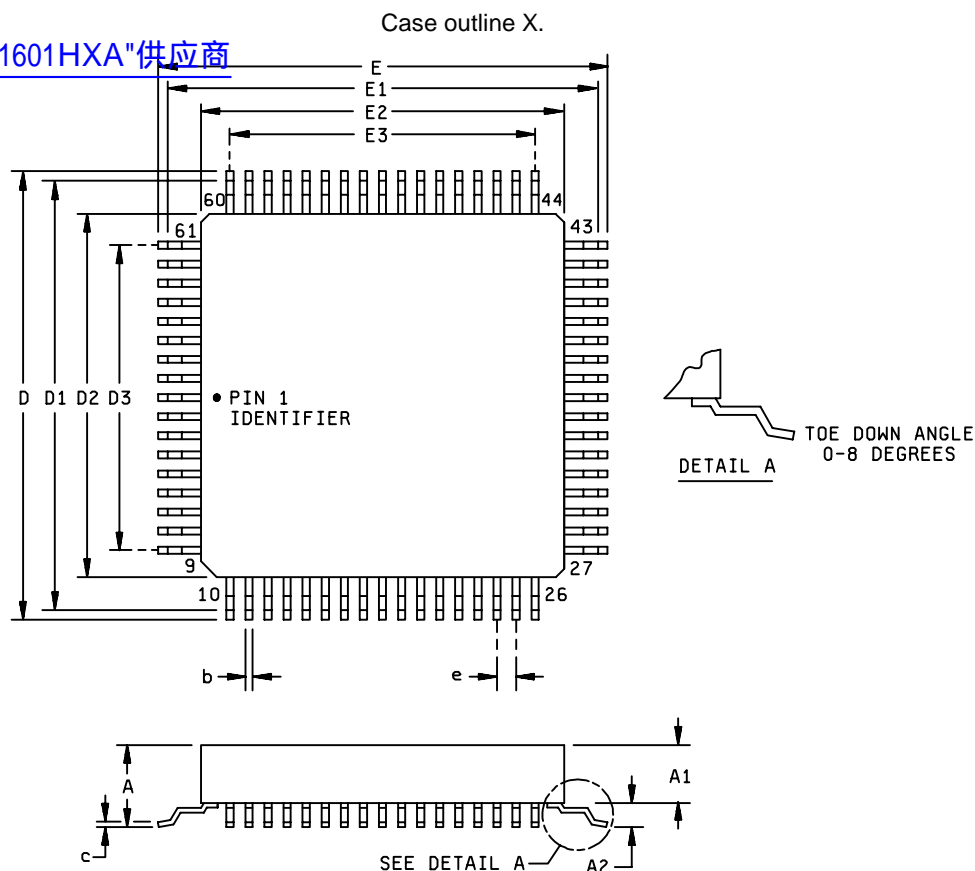
[查询"5962-9961601HXA"供应商](#)

Test	Symbol	Conditions 1/ $-40^{\circ}\text{C} \leq T_C \leq +85^{\circ}$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Channel to channel isolation 3/ 12/	ISO	$T_A = +25^{\circ}\text{C}$	4	01	90		dB

- 1/ $AV_{CC}(\text{analog}) = +5\text{ V dc}$, $AV_{EE}(\text{analog}) = -5\text{ V dc}$, and $DV_{CC}(\text{digital}) = +3.3\text{ V dc}$, unless otherwise specified. AV_{CC} may be varied from $+4.85\text{ V}$ to $+5.25\text{ V}$. However, rated AC (harmonics) performance is valid only over the range; $AV_{CC} = 5.0\text{ V}$ to 5.25 V .
- 2/ Gain tests are preformed on A_{IN1} input voltage range.
- 3/ Parameter shall be tested as part of device initial characterization and after design and process changes. Parameter shall be guaranteed to the limits specified in table I for all lots not specifically tested.
- 4/ All AC specifications tested by driving ENCODE and ENCODE differentially.
- 5/ Digital output logic levels: $V_{CC}(\text{digital}) = +3.3\text{ V dc}$, $C_{LOAD} = 10\text{ pF}$. Capacitive loads $> 10\text{ pF}$ will degrade performance.
- 6/ Input capacitance combines die and package capacitance.
- 7/ Maximum conversion rate allows for variation in ENCODE DUTY CYCLE of 50%, $\pm 5\%$.
- 8/ Analog input signal equals -1 dBFS; SFDR is the ratio of converter full scale to worst spur.
- 9/ Analog input signal power at -1 dBFS; signal-to-noise ratio (SNR) is the ratio of signal level to total noise (first 5 harmonics removed). ENCODE = 65 MSPS. SNR is reported in dBFS, related back to converter full scale.
- 10/ Analog input signal power at -1 dBFS; signal-to-noise and distortion (SINAD) is the ratio of signal level to total noise plus harmonics. ENCODE = 65 MSPS.
- 11/ Two tone intermodulation distortion rejection is the ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBFS.
- 12/ Channel to channel isolation tested with A channel grounded and a full scale signal applied to B channel.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-99616
		REVISION LEVEL	SHEET 7

[查询"5962-9961601HXA"供应商](#)



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		5.97		0.235
A1		4.45		0.175
A2	0.18	1.02	0.040	0.060
b	0.36	0.51	0.014	0.020
c	0.18	0.25	0.007	0.010
e	1.14	1.40	0.045	0.055
D/E	29.72	30.23	1.170	1.190
D1/E1	27.18		1.070	
D2/E2	23.88	24.38	0.940	0.960
D3/E3	20.32 BSC		0.800 BSC	

NOTES:

1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin 1 dot and pin numbers are for reference only.

FIGURE 1. Case outline(s).

**STANDARD
MICROCIRCUIT DRAWING**

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

SIZE
A

5962-99616

REVISION LEVEL

SHEET

8

[查询"5962-9961601HXA"供应商](#)

Device type	01	Device type	01	Device type	01
Case outline	X	Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	Shield	24	D9A	47	D11B
2	Channel A analog ground	25	D10A	48	D12B
3	VREF_ A	26	Channel A digital ground	49	D13B (MSB)
4	Channel A analog ground	27	Channel A digital ground	50	DV _{CC}
5	Channel A analog ground	28	<u>Encode A</u>	51	Encode B
6	Analog input A1	29	Encode A	52	<u>Encode B</u>
7	Analog input A2	30	DV _{CC}	53	Channel B analog ground
8	Analog input A3	31	D11A	54	Channel B analog ground
9	Channel A analog ground	32	D12A	55	Data ready B output
10	Channel A analog ground	33	D13A (MSB)	56	VREF_ B
11	Channel A analog ground	34	D0B (LSB)	57	Channel B analog ground
12	Data ready A output	35	D1B	58	Channel B analog ground
13	AV _{EE}	36	D2B	59	Channel B analog ground
14	AV _{CC}	37	D3B	60	Channel B analog ground
15	DOA (LSB)	38	D4B	61	Channel B analog ground
16	D1A	39	D5B	62	Analog input B1
17	D2A	40	D6B	63	Analog input B2
18	D3A	41	D7B	64	Analog input B3
19	D4A	42	D8B	65	Channel B analog ground
20	D5A	43	Channel B digital ground	66	AV _{CC}
21	D6A	44	Channel B digital ground	67	AV _{EE}
22	D7A	45	D9B	68	Channel B analog ground
23	D8A	46	D10B		

FIGURE 2. Terminal connections.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-99616
		REVISION LEVEL	SHEET 9

TABLE II. Electrical test requirements.

[查询"5962-9961601HXA"供应商](#)

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1
Final electrical parameters	1*,2,3,4,5,6,7,8
Group A test requirements	1,2,3,4,5,6,7,8
Group C end-point electrical parameters	1
End-point electrical parameters for radiation hardness assurance (RHA) devices	Not applicable

* PDA applies to subgroup 1.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 9, 10, and 11 shall be omitted.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - (2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Radiation Hardness Assurance (RHA) inspection. RHA inspection is not currently applicable to this drawing.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-99616
		REVISION LEVEL	SHEET 10

5. PACKAGING

[查询"5962-9961601HXA"供应商](#)

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-PRF-38534.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Post Office Box 3990, Columbus, Ohio 43216-5000, or telephone (614) 692-0512.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-99616
		REVISION LEVEL	SHEET 11

[查询"5962-9961601HXA"供应商](#) STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-02-02

Approved sources of supply for SMD 5962-99616 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-9961601HXA	34031	AD10465BZ/QMLH

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

34031

Vendor name
and address

Analog Devices Incorporated
7910 Triad Center Drive
Greensboro, NC 27409-9605

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.