



November 2001
Revised November 2001

74ALVC162240

Low Voltage 16-Bit Inverting Buffer/Line Driver with 3.6V Tolerant Inputs and Outputs and 26Ω Series Resistors in Outputs

General Description

The ALVC162240 contains sixteen inverting buffers with 3-STATE outputs to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble (4-bit) controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

The 74ALVC162240 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O capability up to 3.6V. The 74ALVC162240 is also designed with 26Ω series resistors in the outputs. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The 74ALVC162240 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.65V to 3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- 26Ω series resistors in outputs
- t_{PD}
 - 3.8 ns max for 3.0V to 3.6V V_{CC}
 - 4.3 ns max for 2.3V to 2.7V V_{CC}
 - 7.6 ns max for 1.65V to 1.95V V_{CC}
- Power-off high impedance inputs and outputs
- Supports live insertion and withdrawal (Note 1)
- Uses patented noise/EMI reduction circuitry
- Latchup conforms to JEDEC JED78
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V

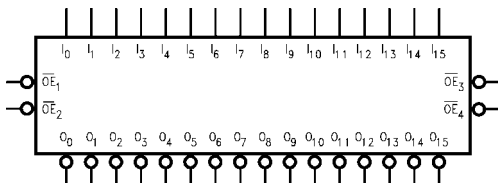
Note 1: To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Descriptions
74ALVC162240T	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



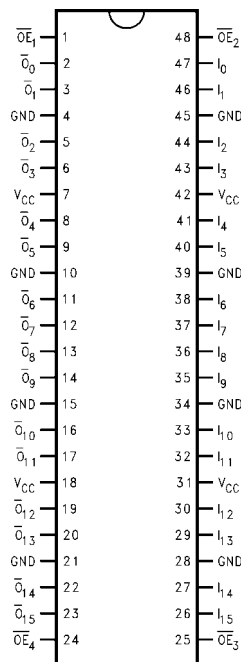
Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
I_0-I_{15}	Inputs
$\overline{O}_0-\overline{O}_{15}$	Outputs

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Connection Diagram



Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0-I_3	$\overline{O}_0-\overline{O}_3$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{O}E_2$	I_4-I_7	$\overline{O}_4-\overline{O}_7$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8-I_{11}	$\overline{O}_8-\overline{O}_{11}$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	$I_{12}-I_{15}$	$\overline{O}_{12}-\overline{O}_{15}$
L	L	H
L	H	L
H	X	Z

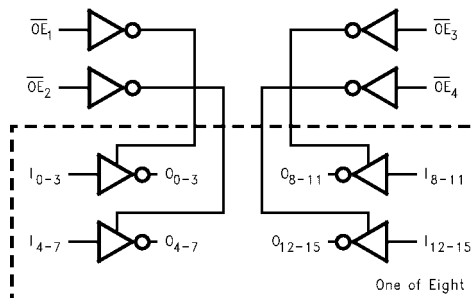
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)
Z = High Impedance

Functional Description

The 74ALVC162240 contains sixteen inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of each other. The control pins may be shorted together to obtain full 16-bit operation. The 3-STATE outputs are con-

trolled by an Output Enable ($\overline{\text{OE}}_n$) input. When $\overline{\text{OE}}_n$ is LOW, the outputs are in the 2-state mode. When $\overline{\text{OE}}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the inputs.

Logic Diagram



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AC Electrical Characteristics

Symbol	Parameter	T _A = -40°C to +85°C, R _L = 500Ω								Units
		C _L = 50 pF				C _L = 30 pF				
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		V _{CC} = 2.5V ± 0.2V		V _{CC} = 1.8V ± 0.15V		
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{PHL} , t _{PL}	Propagation Delay Bus to Bus	1.3	3.8	1.5	4.3	1.0	3.8	1.5	7.6	ns
t _{PZL} , t _{PZH}	Output Enable Time	1.3	4.3	1.5	5.6	1.0	5.1	1.5	9.8	ns
t _{PLZ} , t _{PHZ}	Output Disable Time	1.3	4.1	1.5	4.5	1.0	4.0	1.5	7.2	ns

Capacitance

Symbol	Parameter		Conditions	$T_A = +25^{\circ}\text{C}$		Units
				V_{CC}	Typical	
C_{IN}	Input Capacitance		$V_I = 0\text{V or } V_{CC}$	3.3	6	pF
C_{OUT}	Output Capacitance		$V_I = 0\text{V or } V_{CC}$	3.3	7	pF
C_{PD}	Power Dissipation Capacitance	Outputs Enabled	$f = 10\text{ MHz}, C_L = 50\text{ pF}$	3.3	20	pF
				2.5	20	

AC Loading and Waveforms

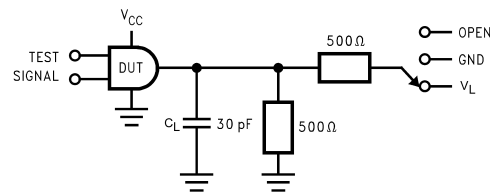


FIGURE 1. AC Test Circuit

TABLE 1. Values for Figure 1

TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	V_L
t_{PZH} , t_{PHZ}	GND

TABLE 2. Variable Matrix
(Input Characteristics: $f = 1\text{MHz}$; $t_r = t_f = 2\text{ns}$; $Z_0 = 50\Omega$)

Symbol	V_{CC}			
	$3.3\text{V} \pm 0.3\text{V}$	2.7V	$2.5\text{V} \pm 0.2\text{V}$	$1.8\text{V} \pm 0.15\text{V}$
V_{mi}	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.15\text{V}$	$V_{OL} + 0.15\text{V}$
V_Y	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.15\text{V}$	$V_{OH} - 0.15\text{V}$
V_L	6V	6V	$V_{CC} \times 2$	$V_{CC} \times 2$

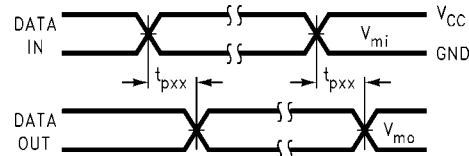


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

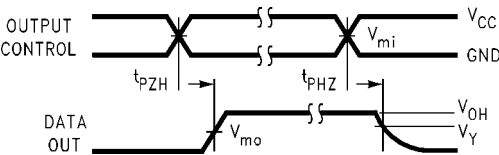


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

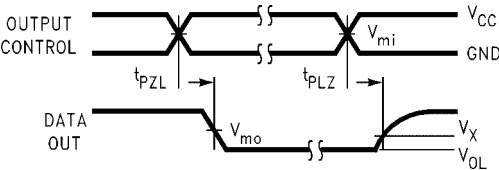
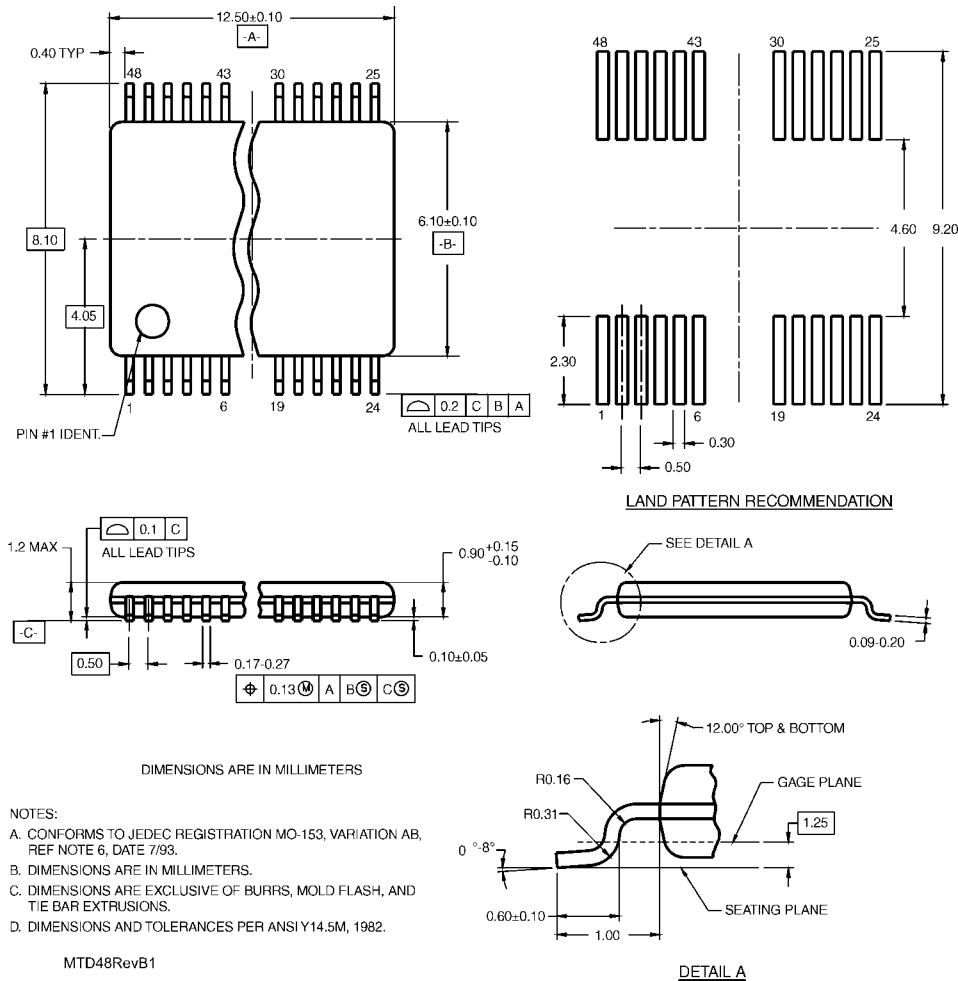


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

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Physical Dimensions inches (millimeters) unless otherwise noted



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